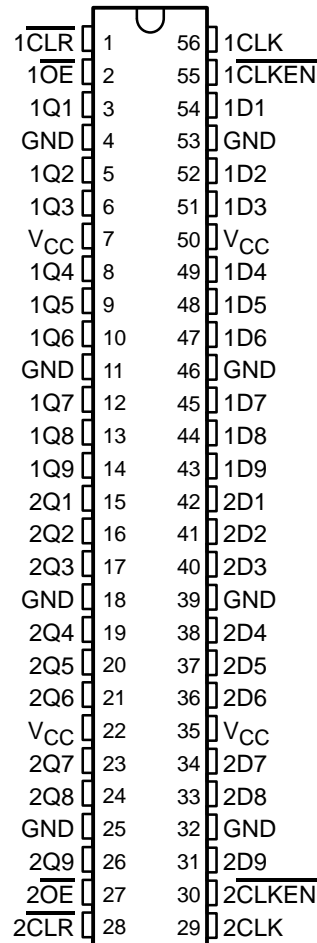


54AC16823, 74AC16823 18-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCAS243A – APRIL 1991 – REVISED APRIL 1996

- **Members of the Texas Instruments Widebus™ Family**
- **Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses With Parity**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Package Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Pin Spacings**

54AC16823 . . . WD PACKAGE
74AC16823 . . . DL PACKAGE
(TOP VIEW)



description

These 18-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, parity bus interfacing, and working registers.

The 'AC16823 can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable ($\overline{\text{CLKEN}}$) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{\text{CLKEN}}$ high disables the clock buffer, thus latching the outputs. Taking the clear ($\overline{\text{CLR}}$) input low causes the Q outputs to go low independently of the clock.

The output enable ($\overline{\text{OE}}$) input can be used to place the outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

$\overline{\text{OE}}$ does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74AC16823 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54AC16823 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74AC16823 is characterized for operation from -40°C to 85°C .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1996, Texas Instruments Incorporated

54AC16823, 74AC16823

18-BIT BUS INTERFACE FLIP-FLOPS

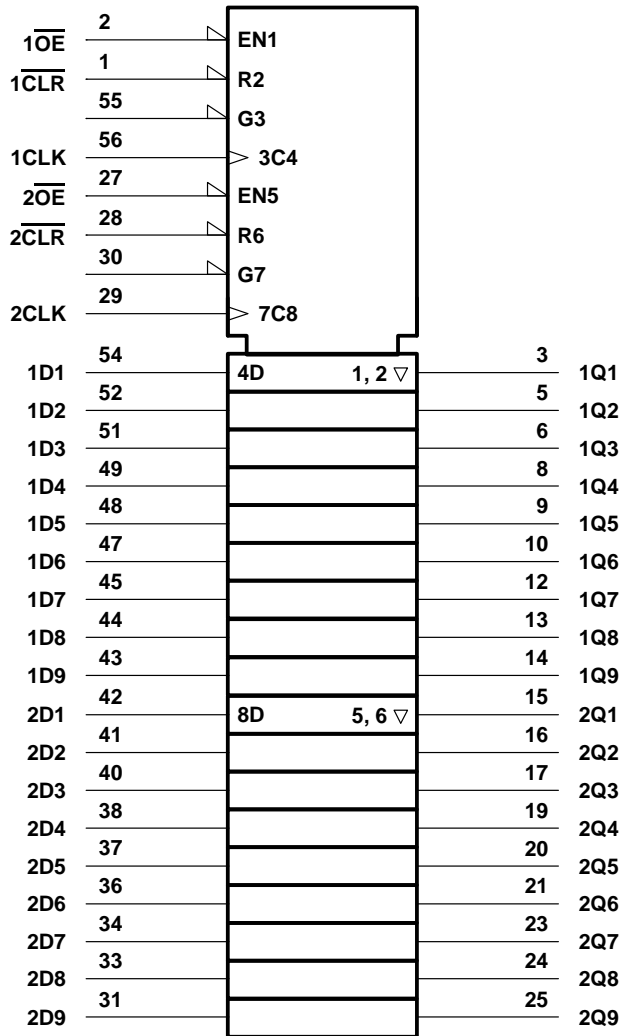
WITH 3-STATE OUTPUTS

SCAS243A – APRIL 1991 – REVISED APRIL 1996

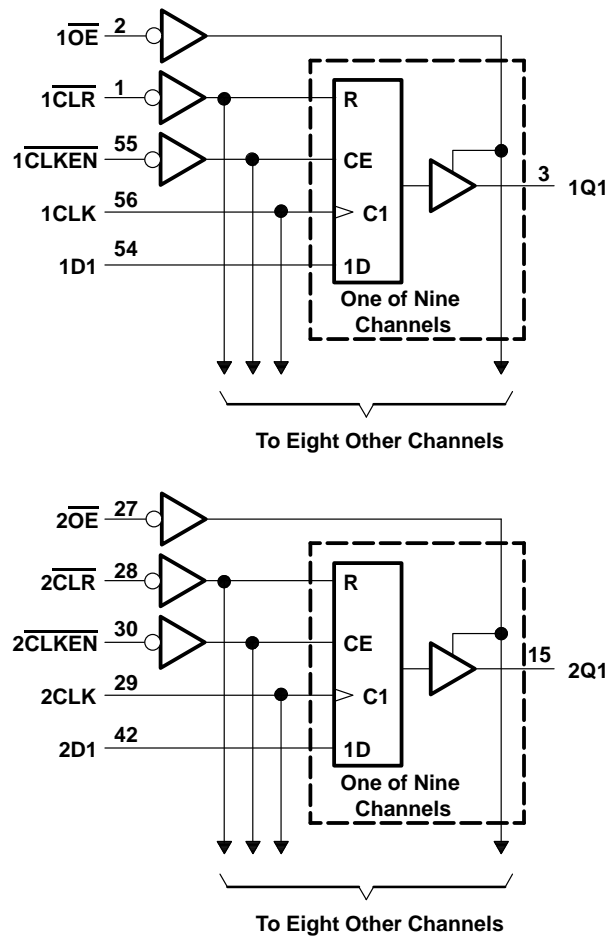
FUNCTION TABLE
(each 9-bit stage)

INPUTS					OUTPUT
\overline{OE}	\overline{CLR}	\overline{CLKEN}	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	L	L	X	Q_0
L	H	H	X	X	Q_0
H	X	X	X	X	Z

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

54AC16823, 74AC16823
18-BIT BUS INTERFACE FLIP-FLOPS
WITH 3-STATE OUTPUTS

SCAS243A – APRIL 1991 – REVISED APRIL 1996

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±450 mA
Maximum power package dissipation at $T_A = 55^\circ\text{C}$ (in still air)(see Note 2): DL package	1.4 W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

		54AC16823			74AC16823			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 3$ V		2.1	$V_{CC} = 3$ V		2.1	V
		$V_{CC} = 4.5$ V		3.15	$V_{CC} = 4.5$ V		3.15	
		$V_{CC} = 5.5$ V		3.85	$V_{CC} = 5.5$ V		3.85	
V_{IL}	Low-level input voltage	$V_{CC} = 3$ V			$V_{CC} = 3$ V		0.9	V
		$V_{CC} = 4.5$ V			$V_{CC} = 4.5$ V		1.35	
		$V_{CC} = 5.5$ V			$V_{CC} = 5.5$ V		1.65	
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 3$ V			$V_{CC} = 3$ V		–4	mA
		$V_{CC} = 4.5$ V			$V_{CC} = 4.5$ V		–24	
		$V_{CC} = 5.5$ V			$V_{CC} = 5.5$ V		–24	
I_{OL}	Low-level output current	$V_{CC} = 3$ V			$V_{CC} = 3$ V		12	mA
		$V_{CC} = 4.5$ V			$V_{CC} = 4.5$ V		24	
		$V_{CC} = 5.5$ V			$V_{CC} = 5.5$ V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	–55		125	–40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

54AC16823, 74AC16823 18-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCAS243A – APRIL 1991 – REVISED APRIL 1996

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC16823		74AC16823		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	3 V	2.9			2.9		2.9	V	
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		2.48		
		4.5 V	3.94			3.8		3.8		
		5.5 V	4.94			4.8		4.8		
I _{OH} = -75 mA [†]	5.5 V				3.85		3.85			
V _{OL}	I _{OL} = 50 μA	3 V			0.1		0.1	0.1	V	
		4.5 V			0.1		0.1	0.1		
		5.5 V			0.1		0.1	0.1		
	I _{OL} = 12 mA	3 V			0.36		0.44	0.44		
		4.5 V			0.36		0.44	0.44		
	I _{OL} = 24 mA	3 V			0.36		0.44	0.44		
		5.5 V			0.36		0.44	0.44		
I _{OL} = 75 mA [†]	5.5 V					1.65	1.65			
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1	±1	μA	
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.5		±5	±5	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		80	80	μA	
C _i	V _I = V _{CC} or GND	5 V			3				pF	
C _o	V _O = V _{CC} or GND	5 V			11				pF	

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range,
V_{CC} = 3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		54AC16823		74AC16823		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	0	60	0	60	0	60	MHz
t _w	Pulse duration	CLR low	3.3		3.3		3.3	ns
		CLK high or low	8.4		8.4		8.4	
t _{su}	Setup time before CLK [↑]	CLR inactive	0.5		0.5		0.5	ns
		Data	7.2		7.2		7.2	
		CLKEN low	5.8		5.8		5.8	
t _h	Hold time after CLK [↑]	Data	0		0		0	ns
		CLKEN high or low	1		1		1	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

54AC16823, 74AC16823 18-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCAS243A – APRIL 1991 – REVISED APRIL 1996

**timing requirements over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

		T _A = 25°C		54AC16823		74AC16823		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	0	115	0	115	0	115	MHz
t _w	Pulse duration	CLR low		3.3	3.3	3.3	3.3	ns
		CLK high or low		4.4	4.4	4.4	4.4	
t _{su}	Setup time before CLK↑	CLR inactive		0.6	0.6	0.6	0.6	ns
		Data		5	5	5	5	
		CLKEN low		4.2	4.2	4.2	4.2	
t _h	Hold time after CLK↑	Data		1.3	1.3	1.3	1.3	ns
		CLKEN high or low		1.4	1.4	1.4	1.4	

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			54AC16823		74AC16823		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			60			60		60	MHz	
t _{PLH}	CLK	Q	3.9	13.8	16.8	3.9	18.8	3.9	18.8	ns
t _{PHL}			4.7	14.5	17.3	4.7	18.9	4.7	18.9	
t _{PHL}	CLR	Q	4	12.4	14.9	4	16.2	4	16.2	ns
t _{PZH}	OE	Q	3	11.1	14	3	15.4	3	15.4	ns
t _{PZL}			4.3	15	18.7	4.3	20.8	4.3	20.8	
t _{PHZ}	OE	Q	4.5	8.5	10.4	4.5	11.2	4.5	11.2	ns
t _{PLZ}			3.9	7.7	9.3	3.9	10.3	3.9	10.3	

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			54AC16823		74AC16823		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			115			115		115	MHz	
t _{PLH}	CLK	Q	3.1	7.8	10.6	3.1	12	3.1	12	ns
t _{PHL}			3.9	8.6	11.4	3.9	12.7	3.9	12.7	
t _{PHL}	CLR	Q	3.2	7.4	9.9	3.2	11	3.2	11	ns
t _{PZH}	OE	Q	2.2	6.1	8.6	2.2	9.7	2.2	9.7	ns
t _{PZL}			3	7.4	10.6	3	11.8	3	11.8	
t _{PHZ}	OE	Q	4.2	6.8	8.7	4.2	9.3	4.2	9.3	ns
t _{PLZ}			3.7	6.2	7.8	3.7	8.6	3.7	8.6	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	36	pF
		Outputs disabled	18	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

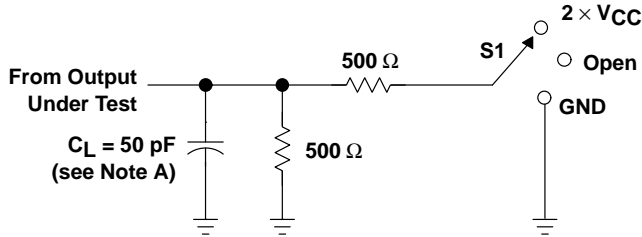


POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

54AC16823, 74AC16823
18-BIT BUS INTERFACE FLIP-FLOPS
WITH 3-STATE OUTPUTS

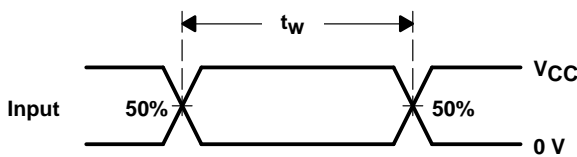
SCAS243A – APRIL 1991 – REVISED APRIL 1996

PARAMETER MEASUREMENT INFORMATION

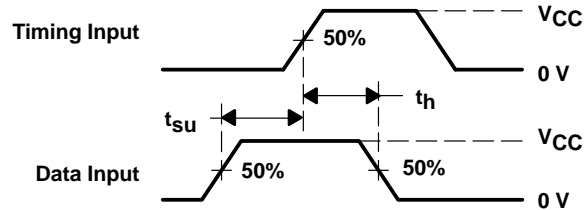


LOAD CIRCUIT

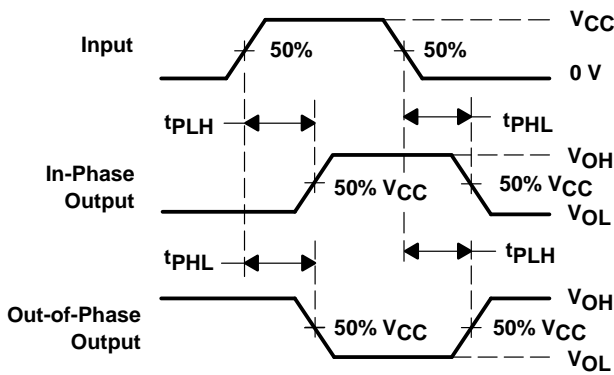
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



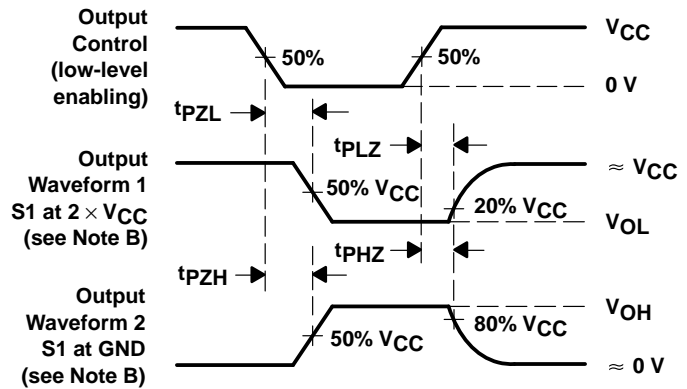
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 3$ ns, $t_f = 3$ ns.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.