

## 54AC175 • 54ACT175 Quad D Flip-Flop

Check for Samples: [54AC175](#), [54ACT175](#)

### FEATURES

- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Asynchronous Common Reset
- True and Complement Output
- Outputs Source/Sink 24 mA
- 'ACT175 has TTL-Compatible Inputs
- Standard Microcircuit Drawing (SMD)
  - 'AC175: 5962-89552
  - 'ACT175: 5962-89693

### DESCRIPTION

The 'AC/'ACT175 is a high-speed quad D flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

### Logic Symbols

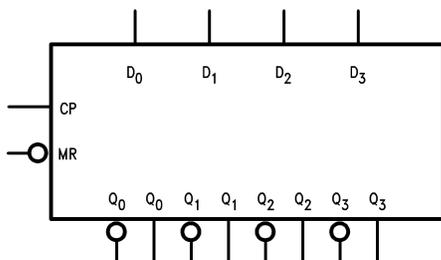


Figure 1. IEEE/IEC

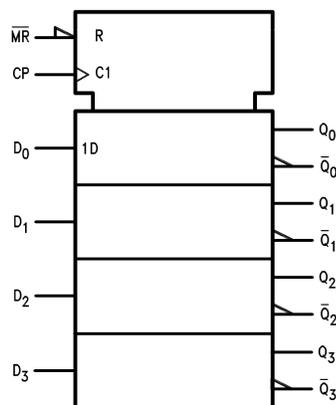


Figure 2. IEEE/IEC

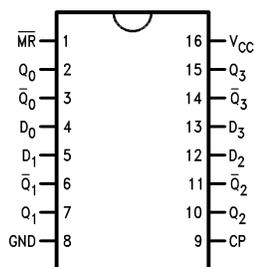
Pin Names	Description
D <sub>0</sub> –D <sub>3</sub>	Data Inputs
CP	Clock Pulse Input
$\overline{\text{MR}}$	Master Reset Input
Q <sub>0</sub> –Q <sub>3</sub>	True Outputs
$\overline{\text{Q}}_0$ – $\overline{\text{Q}}_3$	Complement Outputs



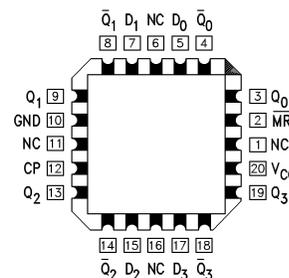
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## Connection Diagrams



**Figure 3. Pin Assignment for CDIP and CLGA**  
See Package Numbers NFE and NAD



**Figure 4. Pin Assignment for LCCC**  
See Package Number NAJ

## Functional Description

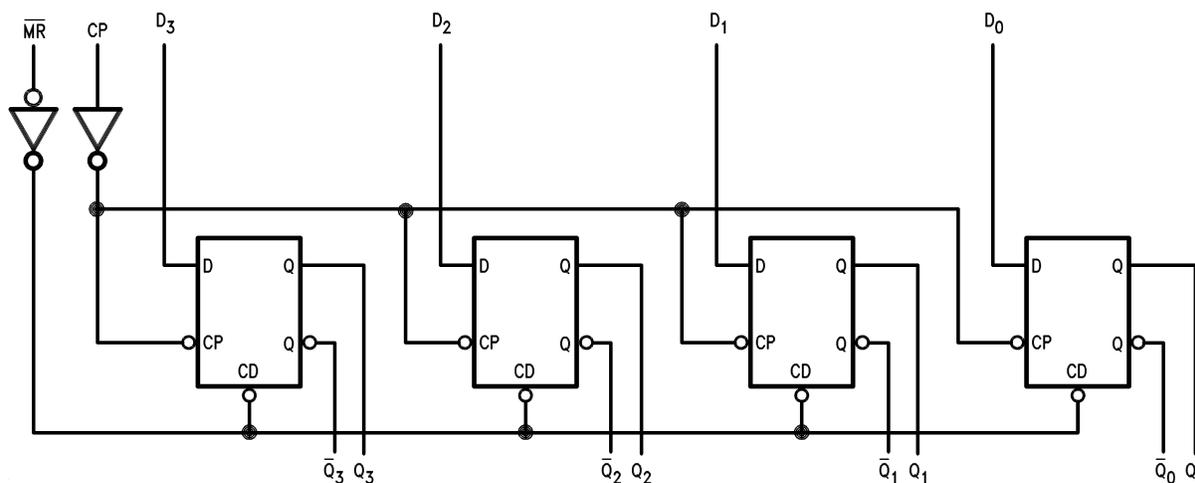
The 'AC/'ACT175 consists of four edge-triggered D flip-flops with individual D inputs and Q and  $\bar{Q}$  outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and  $\bar{Q}$  outputs to follow. A LOW input on the Master Reset ( $\overline{MR}$ ) will force all Q outputs LOW and  $\bar{Q}$  outputs HIGH independent of Clock or Data inputs. The 'AC/'ACT175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

### TRUTH TABLE<sup>(1)</sup>

Inputs		Outputs	
@ $t_n$ , $\overline{MR} = H$		@ $t_{n+1}$	
$D_n$		$Q_n$	$\bar{Q}_n$
L		L	H
H		H	L

- (1) H = HIGH Voltage Level  
L = LOW Voltage Level  
 $t_n$  = Bit Time before Clock Pulse  
 $t_{n+1}$  = Bit Time after Clock Pulse

### LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### ABSOLUTE MAXIMUM RATINGS<sup>(1)(2)</sup>

Supply Voltage ( $V_{CC}$ )		-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	$V_I = -0.5V$	-20 mA
	$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )		-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	$V_O = -0.5V$	-20 mA
	$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )		-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )		$\pm 50$ mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )		$\pm 50$ mA
Storage Temperature ( $T_{STG}$ )		-65°C to +150°C
Junction Temperature ( $T_J$ )	CDIP	175°C

- (1) Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Texas Instruments does not recommend operation of FACT<sup>®</sup> circuits outside databook specifications.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

### RECOMMENDED OPERATING CONDITIONS

Supply Voltage ( $V_{CC}$ )	'AC	2.0V to 6.0V
	'ACT	4.5V to 5.5V
Input Voltage ( $V_I$ )		0V to $V_{CC}$
Output Voltage ( $V_O$ )		0V to $V_{CC}$
Operating Temperature ( $T_A$ )	54AC/ACT	-55°C to +125°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	'AC Devices	
	$V_{IN}$ from 30% to 70% of $V_{CC}$	
	$V_{CC}$ @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	'ACT Devices	
	$V_{IN}$ from 0.8V to 2.0V	
	$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

**DC CHARACTERISTICS FOR 'AC FAMILY DEVICES**

Symbol	Parameter	V <sub>CC</sub> (V)	54AC		Units	Conditions	
			T <sub>A</sub> = -55°C to +125°C				
			Specified Limits				
V <sub>IH</sub>	Minimum High Level Input Voltage	3.0	2.1		V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	
		4.5	3.15				
		5.5	3.85				
V <sub>IL</sub>	Maximum Low Level Input Voltage	3.0	0.9		V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	
		4.5	1.35				
		5.5	1.65				
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0	2.9		V	I <sub>OUT</sub> = -50 μA	
		4.5	4.4				
		5.5	5.4				
			3.0	2.4		V	See <sup>(1)</sup> V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -12 mA I <sub>OH</sub> = -24 mA I <sub>OH</sub> = -24 mA
			4.5	3.7			
			5.5	4.7			
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	0.1		V	I <sub>OUT</sub> = 50 μA	
		4.5	0.1				
		5.5	0.1				
			3.0	0.50		V	See <sup>(1)</sup> V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 12 mA I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 24 mA
			4.5	0.50			
			5.5	0.50			
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	±1.0		μA	V <sub>I</sub> = V <sub>CC</sub> , GND	
I <sub>OLD</sub>	Minimum Dynamic <sup>(2)</sup>	5.5	50		mA	V <sub>OLD</sub> = 1.65V Max	
I <sub>OHD</sub>	Output Current	5.5	-50		mA	V <sub>OHD</sub> = 3.85V Min	
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	160.0		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	

(1) All outputs loaded; thresholds on input associated with output under test.

(2) Maximum test duration 2.0 ms, one output loaded at a time.

**DC CHARACTERISTICS FOR 'ACT FAMILY DEVICES**

Symbol	Parameter	V <sub>CC</sub> (V)	54ACT		Units	Conditions
			T <sub>A</sub> = -55°C to +125°C			
			Specified Limits			
V <sub>IH</sub>	Minimum High Level Input Voltage	4.5	2.0		V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
		5.5	2.0			
V <sub>IL</sub>	Maximum Low Level Input Voltage	4.5	0.8		V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
		5.5	0.8			
V <sub>OH</sub>	Minimum High Level Output Voltage	4.5	4.4		V	I <sub>OUT</sub> = -50 μA
		5.5	5.4			
			4.5	3.70		V
5.5			4.70			

(1) All outputs loaded; thresholds on input associated with output under test.

**DC CHARACTERISTICS FOR 'ACT FAMILY DEVICES (continued)**

Symbol	Parameter	V <sub>CC</sub> (V)	54ACT		Units	Conditions
			T <sub>A</sub> = -55°C to +125°C			
			Specified Limits			
V <sub>OL</sub>	Maximum Low Level Output Voltage	4.5	0.1		V	I <sub>OUT</sub> = 50 μA
		5.5	0.1			
		4.5	0.50		V	See <sup>(1)</sup> V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 24 mA
		5.5	0.50			
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	±1.0		μA	V <sub>I</sub> = V <sub>CC</sub> , GND
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	1.6		mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1V
I <sub>OLD</sub>	See <sup>(2)</sup> Minimum Dynamic	5.5	50		mA	V <sub>OLD</sub> = 1.65V Max
I <sub>OHD</sub>	Output Current	5.5	-50		mA	V <sub>OHD</sub> = 3.85V Min
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	160.0		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND

(2) Maximum test duration 2.0 ms, one output loaded at a time.

**AC ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	V <sub>CC</sub> (V) <sup>(1)</sup>	54AC		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C			
			C <sub>L</sub> = 50 pF			
			Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	3.3	95		MHz	
		5.0	95			
t <sub>PLH</sub>	Propagation Delay CP to Q <sub>n</sub> or $\bar{Q}_n$	3.3	1.0	14.5	ns	
		5.0	1.5	10.5		
t <sub>PHL</sub>	Propagation Delay CP to Q <sub>n</sub> or $\bar{Q}_n$	3.3	1.0	15.0	ns	
		5.0	1.5	11.5		
t <sub>PLH</sub>	Propagation Delay $\overline{MR}$ to $\bar{Q}_n$	3.3	1.0	15.0	ns	
		5.0	1.5	11.0		
t <sub>PHL</sub>	Propagation Delay $\overline{MR}$ to Q <sub>n</sub>	3.3	1.0	13.5	ns	
		5.0	1.5	10.5		

(1) Voltage Range 3.3 is 3.3V ±0.3V  
Voltage Range 5.0 is 5.0V ±0.5V.

**AC OPERATING REQUIREMENTS**

Symbol	Parameter	V <sub>CC</sub> (V) <sup>(1)</sup>	54AC		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C			
			C <sub>L</sub> = 50 pF			
			Specified Minimum			
t <sub>s</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to CP	3.3	5.0		ns	
		5.0	3.5			
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP	3.3	2.0		ns	
		5.0	2.5			

(1) Voltage Range 3.3 is 3.3V ±0.3V  
Voltage Range 5.0 is 5.0V ±0.5V.

**AC OPERATING REQUIREMENTS (continued)**

Symbol	Parameter	V <sub>CC</sub> (V) <sup>(1)</sup>	54AC		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF			
			Specified Minimum			
t <sub>w</sub>	CP Pulse Width HIGH or LOW	3.3	6.0		ns	
		5.0	5.0			
t <sub>w</sub>	$\overline{\text{MR}}$ Pulse Width, LOW	3.3	5.5		ns	
		5.0	5.0			
t <sub>rec</sub>	Recovery Time $\overline{\text{MR}}$ to CP	3.3	1.5		ns	
		5.0	1.5			

**AC ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	V <sub>CC</sub> (V) <sup>(1)</sup>	54ACT		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF			
			Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	5.0	95		MHz	
t <sub>PLH</sub>	Propagation Delay CP to Q <sub>n</sub> or $\overline{\text{Q}}_n$	5.0	1.5	11.5	ns	
t <sub>PHL</sub>	Propagation Delay CP to Q <sub>n</sub> or $\overline{\text{Q}}_n$	5.0	1.5	12.5	ns	
t <sub>PLH</sub>	Propagation Delay $\overline{\text{MR}}$ to $\overline{\text{Q}}_n$	5.0	1.5	11.5	ns	
t <sub>PHL</sub>	Propagation Delay $\overline{\text{MR}}$ to Q <sub>n</sub>	5.0	1.5	11.0	ns	

(1) Voltage Range 5.0 is 5.0V ±0.5V.

**AC OPERATING REQUIREMENTS**

Symbol	Parameter	V <sub>CC</sub> (V) <sup>(1)</sup>	54ACT		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF			
			Specified Minimum			
t <sub>s</sub> (H)	Setup Time	5.0	3.5		ns	
t <sub>s</sub> (L)	D <sub>n</sub> to CP		3.5			
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP	5.0	1.5		ns	
t <sub>w</sub>	CP Pulse Width HIGH or LOW	5.0	5.0		ns	
t <sub>w</sub>	$\overline{\text{MR}}$ Pulse Width, LOW	5.0	5.0		ns	
t <sub>rec</sub>	Recovery Time, $\overline{\text{MR}}$ to CP	5.0	1.5		ns	

(1) Voltage Range 5.0 is 5.0V ±0.5V.

**CAPACITANCE**

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
C <sub>PD</sub>	Power Dissipation Capacitance	45.0	pF	V <sub>CC</sub> = 5.0V

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**REVISION HISTORY**

<b>Changes from Revision A (April 2013) to Revision B</b>	<b>Page</b>
• Changed layout of National Data Sheet to TI format .....	<a href="#">6</a>

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