

# UT54ACS164245S

## RadHard Schmitt CMOS 16-bit Bidirectional MultiPurpose Transceiver Datasheet



April, 2002

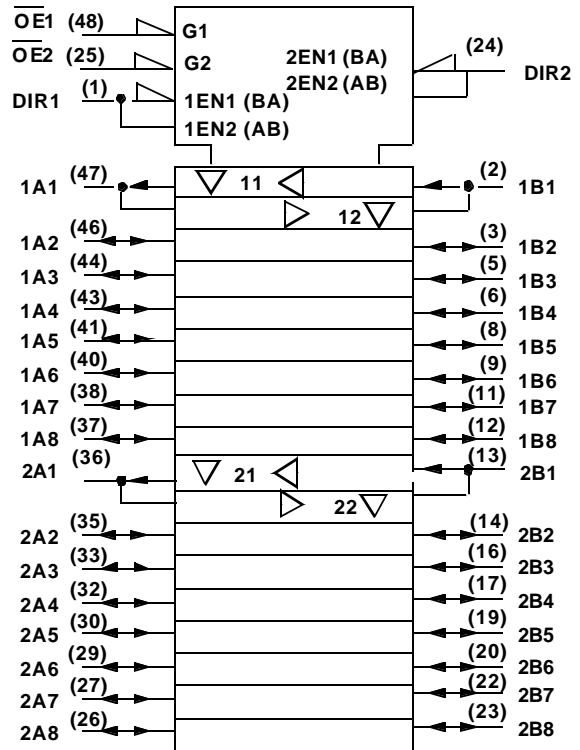
### FEATURES

- Voltage translation
  - 5V bus to 3.3V bus
  - 3.3V bus to 5V bus
- Cold sparing
  - 1MΩ minimum input impedance power-off
- 0.6μm Commercial RadHard™ CMOS
  - Total dose: 100K rad(Si)
  - Single Event Latchup immune
- High speed, low power consumption
- Schmitt trigger inputs to filter noisy signals
- Available QML Q or V processes
- Standard Microcircuit Drawing 5962-98580
- Package:
  - 48-lead flatpack, 25 mil pitch (.390 x .640)

### DESCRIPTION

The 16-bit wide UT54ACS164245S MultiPurpose transceiver is built using UTMC's Commercial RadHard™ epitaxial CMOS technology and is ideal for space applications. This high speed, low power UT54ACS164245S transceiver is designed to perform multiple functions including: asynchronous two-way communication, signal buffering, voltage translation, and cold sparing. With  $V_{DD}$  equal to zero volts, the UT54ACS164245S outputs and inputs present a minimum impedance of 1MΩ making it ideal for "cold spare" applications. Balanced outputs and low "on" output impedance make the UT54ACS164245S well suited for driving high capacitance loads and low impedance backplanes. The UT54ACS164245S enables system designers to interface 3.3 volt CMOS compatible components with 5 volt CMOS components. For voltage translation, the A port interfaces with the 3.3 volt bus; the B port interfaces with the 5 volt bus. The direction control ( $DIR_x$ ) controls the direction of data flow. The output enable ( $\overline{OEx}$ ) overrides the direction control and disables both ports. These signals can be driven from either port A or B. The direction and output enable controls operate these devices as either two independent 8-bit transceivers or one 16-bit transceiver.

### LOGIC SYMBOL



### PIN DESCRIPTION

Pin Names	Description
$\overline{OEx}$	Output Enable Input (Active Low)
$DIR_x$	Direction Control Inputs
$xAx$	Side A Inputs or 3-State Outputs (3.3V Port)
$xBx$	Side B Inputs or 3-State Outputs (5V Port)

### FUNCTION TABLE

ENABLE $\overline{OEx}$	DIRECTION $DIR_x$	OPERATION
L	L	B Data To A Bus
L	H	A Data To B Bus
H	X	Isolation

## PINOUTS

**48-Lead Flatpack  
Top View**

DIR1	1	48	$\overline{\text{OE}}1$
1B1	2	47	1A1
1B2	3	46	1A2
V <sub>SS</sub>	4	45	V <sub>SS</sub>
1B3	5	44	1A3
1B4	6	43	1A4
VDD1	7	42	VDD2
1B5	8	41	1A5
1B6	9	40	1A6
V <sub>SS</sub>	10	39	V <sub>SS</sub>
1B7	11	38	1A7
1B8	12	37	1A8
2B1	13	36	2A1
2B2	14	35	2A2
V <sub>SS</sub>	15	34	V <sub>SS</sub>
2B3	16	33	2A3
2B4	17	32	2A4
VDD1	18	31	VDD2
2B5	19	30	2A5
2B6	20	29	2A6
V <sub>SS</sub>	21	28	V <sub>SS</sub>
2B7	22	27	2A7
2B8	23	26	2A8
DIR2	24	25	$\overline{\text{OE}}2$

**POWER TABLE<sup>1</sup>**

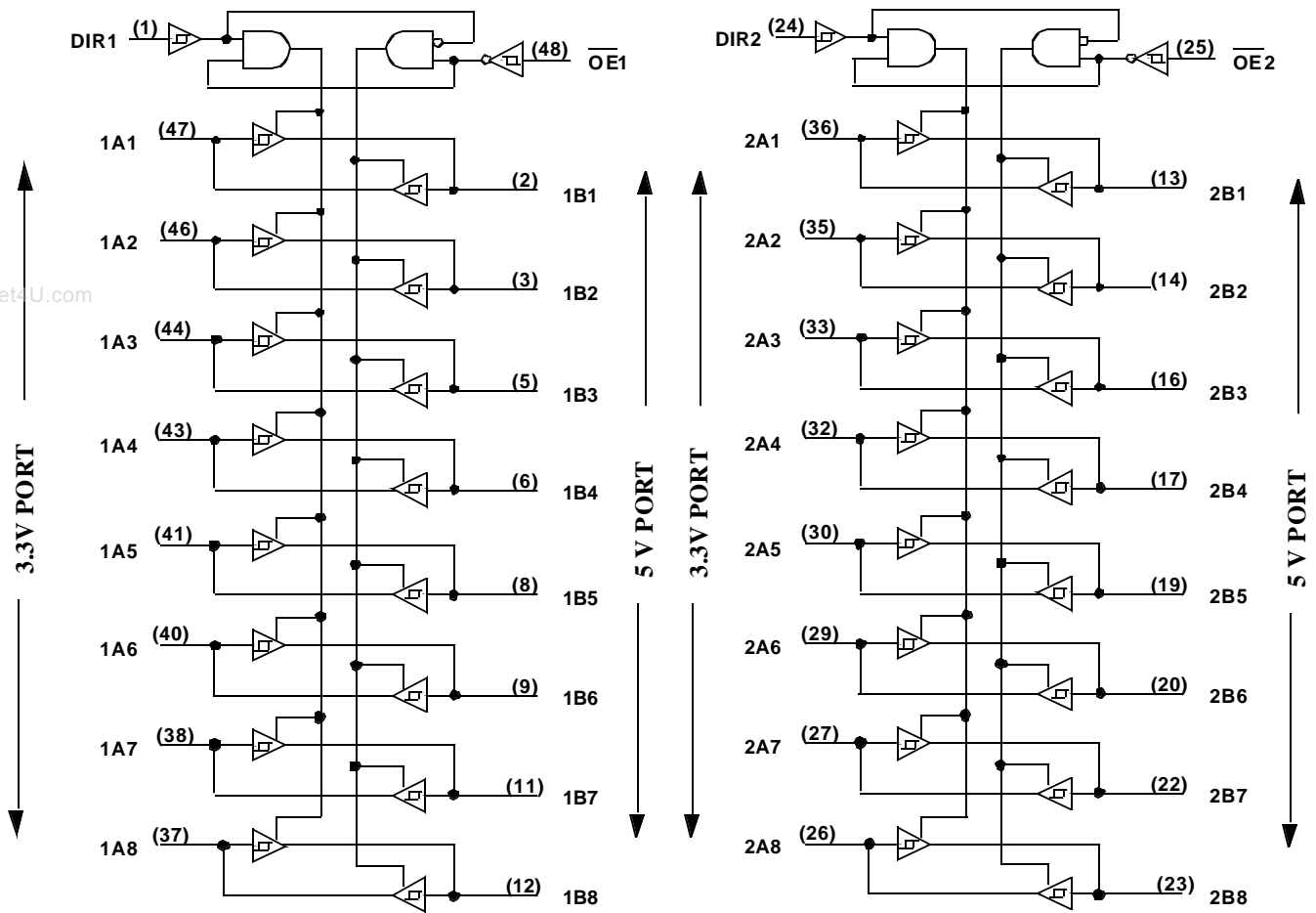
Port B	Port A	OPERATION
5 Volts	3.3 Volts	Voltage Translator
5 Volts	5 Volts	Non Translating
3.3 Volts	3.3 Volts	Non Translating
V <sub>SS</sub>	V <sub>SS</sub>	Cold Spare
V <sub>SS</sub>	3.3V or 5V	Port B Cold Spare

**NOTE:**

1. V<sub>DD2</sub> cannot be tied to V<sub>SS</sub> while power is applied to V<sub>DD1</sub>.

Control signals DIRx and  $\overline{\text{OE}}x$  are 5 volt tolerant inputs. When V<sub>DD2</sub> is at 3.3 volts, either 3.3 or 5 volt CMOS logic levels can be applied to all control inputs. For proper operation connect power to all V<sub>DD</sub> and ground all V<sub>SS</sub> pins (i.e., no floating V<sub>DD</sub> or V<sub>SS</sub> input pins). Tie unused inputs to V<sub>SS</sub>. If V<sub>DD1</sub> and V<sub>DD2</sub> are not powered up together, then V<sub>DD2</sub> should be powered up first for proper control of  $\overline{\text{OE}}$  and DIR. Until V<sub>DD2</sub> reaches 2.75V ± 5%, control of the outputs by  $\overline{\text{OE}}$  and DIR cannot be guaranteed. During operation of the part, after power up, insure V<sub>DD1</sub> ≥ V<sub>DD2</sub>. Tie unused inputs to V<sub>SS</sub>.

# LOGIC DIAGRAM



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## RADIATION HARDNESS SPECIFICATIONS <sup>1</sup>

PARAMETER	LIMIT	UNITS
Total Dose	1.0E5	rad(Si)
SEL Latchup	>120	MeV-cm <sup>2</sup> /mg
Neutron Fluence <sup>2</sup>	1.0E14	n/cm <sup>2</sup>

**Notes:**

1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Not tested, inherent of CMOS technology.

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

SYMBOL	PARAMETER	LIMIT (Mil only)	UNITS
V <sub>IO</sub>	Voltage any pin	-3 to V <sub>DD1</sub> +.3	V
V <sub>DD1</sub>	Supply voltage	-0.3 to 6.0	V
V <sub>DD2</sub>	Supply voltage	-0.3 to 6.0	V
T <sub>STG</sub>	Storage Temperature range	-65 to +150	°C
T <sub>J</sub>	Maximum junction temperature	+175	°C
Θ <sub>JC</sub>	Thermal resistance junction to case	20	°C/W
I <sub>I</sub>	DC input current	±10	mA
P <sub>D</sub>	Maximum power dissipation	1	W

**Note:**

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

## DUAL SUPPLY OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V <sub>DD1</sub>	Supply voltage	3.0 to 3.6 or 4.5 to 5.5	V
V <sub>DD2</sub>	Supply voltage	3.0 to 3.6 or 4.5 to 5.5	V
V <sub>IN</sub>	Input voltage any pin	0 to V <sub>DD1</sub>	V
T <sub>C</sub>	Temperature range	-55 to + 125	°C

## DC ELECTRICAL CHARACTERISTICS <sup>1</sup>

( $-55^{\circ}\text{C} < T_C < +125^{\circ}\text{C}$ ) ( $T_C = -55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  for "C" screening and  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  for "W" screening)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
$V_{T+}$	Schmitt Trigger, positive going threshold <sup>2</sup>	$V_{DD}$ from 3.00 to 5.5		$.7V_{DD}$	V
$V_{T-}$	Schmitt Trigger, negative going threshold <sup>2</sup>	$V_{DD}$ from 3.00 to 5.5	$.3V_{DD}$		V
$V_{H1}$	Schmitt Trigger range of hysteresis <sup>10</sup>	$V_{DD}$ from 4.5 to 5.5	0.6		V
$V_{H2}$	Schmitt Trigger range of hysteresis <sup>10</sup>	$V_{DD}$ from 3.00 to 3.6	0.4		V
$I_{IN}$	Input leakage current <sup>10</sup>	$V_{DD}$ from 3.6 to 5.5 $V_{IN} = V_{DD}$ or $V_{SS}$	-1	3	$\mu\text{A}$
$I_{OZ}$	Three-state output leakage current <sup>10</sup>	$V_{DD}$ from 3.6 to 5.5 $V_{IN} = V_{DD}$ or $V_{SS}$	-1	3	$\mu\text{A}$
$I_{CS}$	Cold sparing leakage current <sup>3</sup>	$V_{IN} = 5.5$ $V_{DD} = V_{SS}$	-1	5	$\mu\text{A}$
$I_{OS1}$	Short-circuit output current <sup>6, 11</sup>	$V_O = V_{DD}$ or $V_{SS}$ $V_{DD}$ from 4.5 to 5.5	-200	200	mA
$I_{OS2}$	Short-circuit output current <sup>6, 11</sup>	$V_O = V_{DD}$ or $V_{SS}$ $V_{DD}$ from 3.00 to 3.6	-100	100	mA
$V_{OL1}$	Low-level output voltage <sup>4, 10</sup>	$I_{OL} = 8\text{mA}$ $I_{OL} = 100\mu\text{A}$ $V_{DD} = 4.5$		0.4 0.2	V
$V_{OL2}$	Low-level output voltage <sup>4, 10</sup>	$I_{OL} = 8\text{mA}$ $I_{OL} = 100\mu\text{A}$ $V_{DD} = 3.00$		0.5 0.2	V
$V_{OH1}$	High-level output voltage <sup>4, 10</sup>	$I_{OH} = -8\text{mA}$ $I_{OH} = -100\mu\text{A}$ $V_{DD} = 4.5$	$V_{DD} - 0.7$ $V_{DD} - 0.2$		V
$V_{OH2}$	High-level output voltage <sup>4, 10</sup>	$I_{OH} = -8\text{mA}$ $I_{OH} = -100\mu\text{A}$ $V_{DD} = 3.00$	$V_{DD} - 0.9$ $V_{DD} - 0.2$		V

$P_{total1}$	Power dissipation <sup>5,7,8</sup>	$C_L = 50\text{pF}$ $V_{DD}$ from 4.5 to 5.5		2.0	mW/ MHz
$P_{total2}$	Power dissipation <sup>5,7,8</sup>	$C_L = 50\text{pF}$ $V_{DD}$ from 3.00 to 3.6		1.5	mW/ MHz
$I_{DD}$	Standby Supply Current $V_{DD1}$ or $V_{DD2}$  Pre-Rad 25°C Pre-Rad -55°C to +125°C Post-Rad 25°C	$V_{IN} = V_{DD}$ or $V_{SS}$ $V_{DD} = 5.5$ $\overline{OE} = V_{DD}$ $\overline{OE} = V_{DD}$ $\overline{OE} = V_{DD}$		10 100 500	$\mu\text{A}$ $\mu\text{A}$ $\mu\text{A}$
$C_{IN}$	Input capacitance <sup>9</sup>	$f = 1\text{MHz @ } 0\text{V}$ $V_{DD}$ from 3.00 to 5.5		15	pF
$C_{OUT}$	Output capacitance <sup>9</sup>	$f = 1\text{MHz @ } 0\text{V}$ $V_{DD}$ from 3.00 to 5.5		15	pF

**Notes:**

- All specifications valid for radiation dose  $\leq 1\text{E}5$  rad(Si) per MIL-STD-883, Method 1019.
- Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions:  $V_{IH} = V_{IH}(\text{min}) + 20\%$ ,  $- 0\%$ ;  $V_{IL} = V_{IL}(\text{max}) + 0\%$ ,  $- 50\%$ , as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$ .
- All combinations of OEx and DIRx
- Per MIL-PRF-38535, for current density  $\leq 5.0\text{E}5$  amps/cm<sup>2</sup>, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF-MHz.
- Guaranteed by characterization.
- Not more than one output may be shorted at a time for maximum duration of one second.
- Power does not include power contribution of any CMOS output sink current.
- Power dissipation specified per switching output.
- Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and  $V_{SS}$  at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
- Guaranteed; tested on a sample of pins per device.
- Supplied as a design limit, but not guaranteed or tested.

## AC ELECTRICAL CHARACTERISTICS<sup>1</sup> (Port B = 5 Volt, Port A = 3.3 Volt)

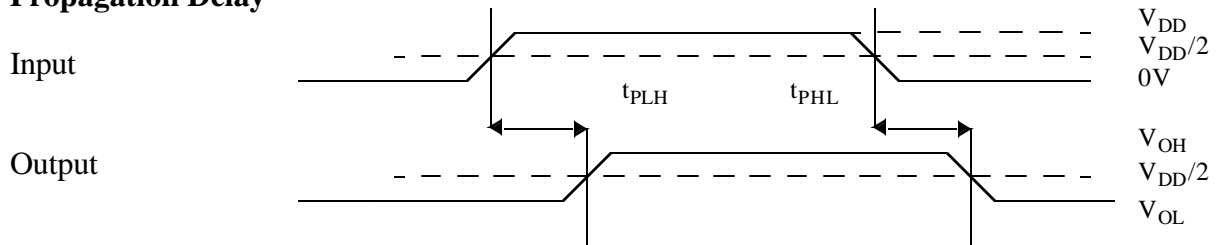
( $V_{DD1} = 5V \pm 10\%$ ;  $V_{DD2} = 3.00V$  to  $3.6V$ ,  $-55^{\circ}C < T_C < +125^{\circ}C$ ) ( $T_C = -55^{\circ}C$  to  $+125^{\circ}C$  for "C" screening and  $-40^{\circ}C$  to  $+125^{\circ}C$  for "W" screening)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
$t_{PLH}$	Propagation delay Data to Bus	1	20	ns
$t_{PHL}$	Propagation delay Data to Bus	1	20	ns
$t_{PZL}$	Output enable time $\overline{OEx}$ to Bus	1	18	ns
$t_{PZH}$	Output enable time $\overline{OEx}$ to Bus	1	18	ns
$t_{PLZ}$	Output disable time $\overline{OEx}$ to Bus high impedance	1	20	ns
$t_{PHZ}$	Output disable time $\overline{OEx}$ to Bus high impedance	1	20	ns
$t_{PZL}^2$	Output enable time DIRx to Bus	1	18	ns
$t_{PZH}^2$	Output enable time DIRx to Bus	1	18	ns
$t_{PLZ}^2$	Output disable time DIRx to Bus high impedance	1	20	ns
$t_{PHZ}^2$	Output disable time DIRx to Bus high impedance	1	20	ns

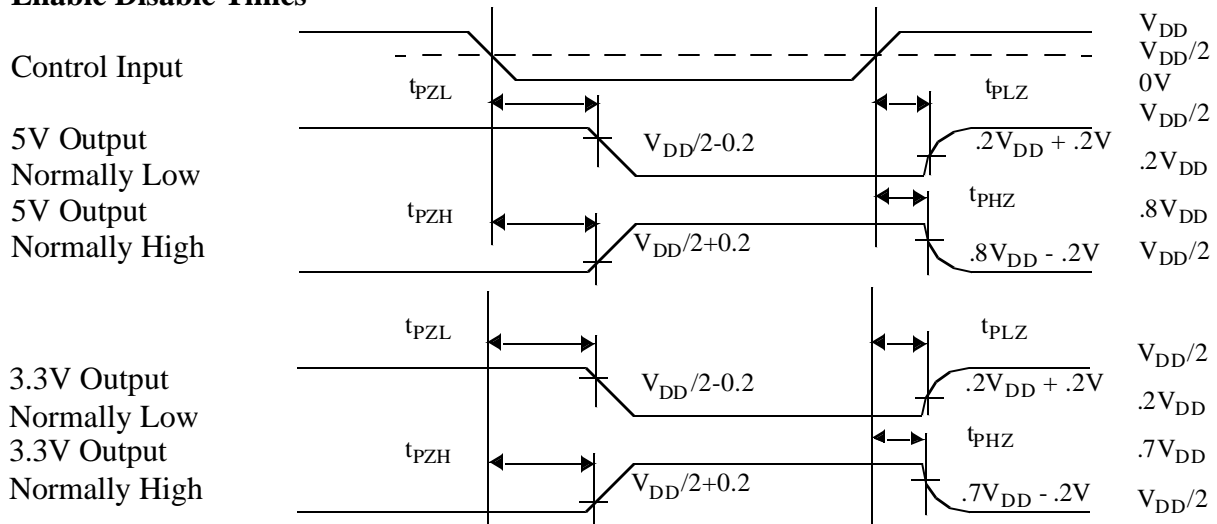
### Notes:

- All specifications valid for radiation dose  $\leq 1E5$  rad(Si) per MIL-STD-883, Method 1019.
- DIRx to bus times are guaranteed by design, but not tested. OEx to bus times are tested.

### Propagation Delay



### Enable Disable Times







### AC ELECTRICAL CHARACTERISTICS<sup>1</sup> (Port A = Port B, 5 Volt Operation)

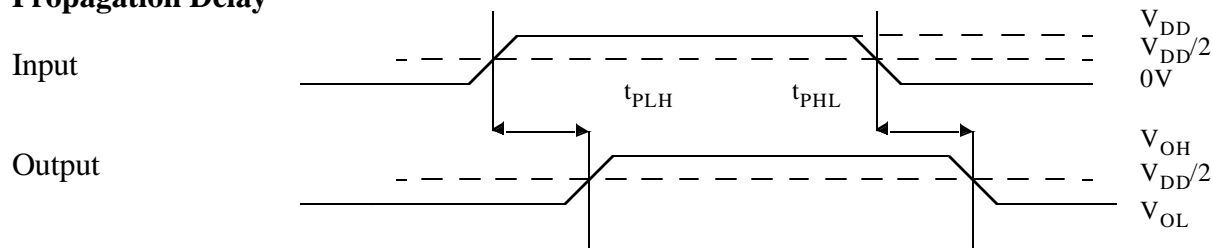
( $V_{DD1} = 5V \pm 10\%$ ;  $V_{DD2} = 5.0V \pm 10\%$ ,  $-55^{\circ}C < T_C < +125^{\circ}C$ )

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
$t_{PLH}$	Propagation delay Data to Bus	1	15	ns
$t_{PHL}$	Propagation delay Data to Bus	1	15	ns
$t_{PZL}$	Output enable time $\overline{OEx}$ to Bus	1	12	ns
$t_{PZH}$	Output enable time $\overline{OEx}$ to Bus	1	12	ns
$t_{PLZ}$	Output disable time $\overline{OEx}$ to Bus high impedance	1	15	ns
$t_{PHZ}$	Output disable time $\overline{OEx}$ to Bus high impedance	1	15	ns
$t_{PZL}^2$	Output enable time DIRx to Bus	1	12	ns
$t_{PZH}^2$	Output enable time DIRx to Bus	1	12	ns
$t_{PLZ}^2$	Output disable time DIRx to Bus high impedance	1	15	ns
$t_{PHZ}^2$	Output disable time DIRx to Bus high impedance	1	15	ns

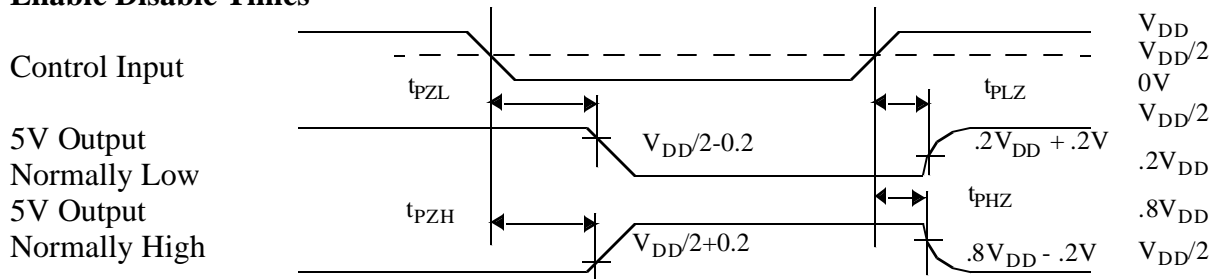
**Notes:**

1. All specifications valid for radiation dose  $\leq 1E5$  rad(Si) per MIL-STD-883, Method 1019.
2. DIRx to bus times are guaranteed by design, but not tested. OEx to bus times are tested

#### Propagation Delay



#### Enable Disable Times



### AC ELECTRICAL CHARACTERISTICS<sup>1</sup> (Port A = Port B, 3.3 Volt Operation)

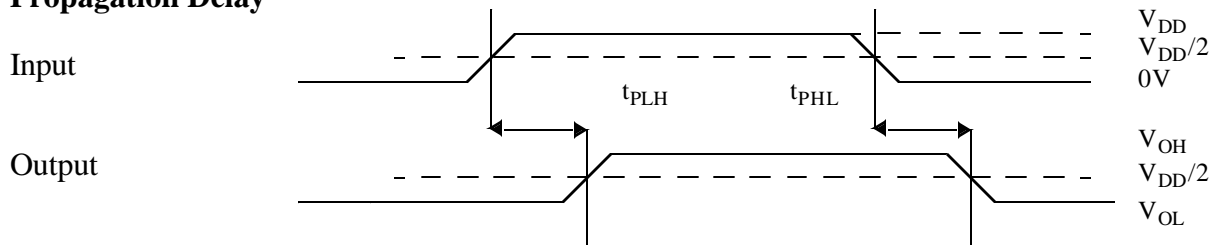
( $V_{DD1} = 3.00V$  to  $3.6V$ ;  $V_{DD2} = 3.00V$  to  $3.6V$ ,  $-55^{\circ}C < T_C < +125^{\circ}C$ )

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
$t_{PLH}$	Propagation delay Data to Bus	1	20	ns
$t_{PHL}$	Propagation delay Data to Bus	1	20	ns
$t_{PZL}$	Output enable time $\overline{OEx}$ to Bus	1	18	ns
$t_{PZH}$	Output enable time $\overline{OEx}$ to Bus	1	18	ns
$t_{PLZ}$	Output disable time $\overline{OEx}$ to Bus high impedance	1	20	ns
$t_{PHZ}$	Output disable time $\overline{OEx}$ to Bus high impedance	1	20	ns
$t_{PZL}^2$	Output enable time DIRx to Bus	1	18	ns
$t_{PZH}^2$	Output enable time DIRx to Bus	1	18	ns
$t_{PLZ}^2$	Output disable time DIRx to Bus high impedance	1	20	ns
$t_{PHZ}^2$	Output disable time DIRx to Bus high impedance	1	20	ns

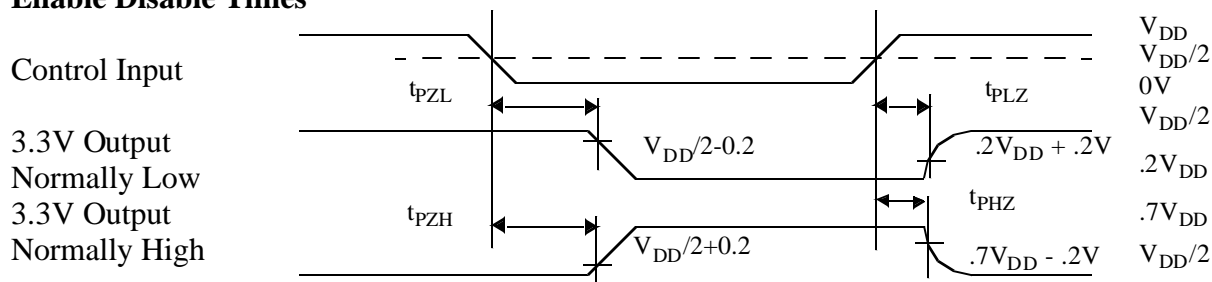
#### Notes:

1. All specifications valid for radiation dose  $\leq 1E5$  rad(Si) per MIL-STD-883, Method 1019.
2. DIRx to bus times are guaranteed by design, but not tested. OEx to bus times are tested.

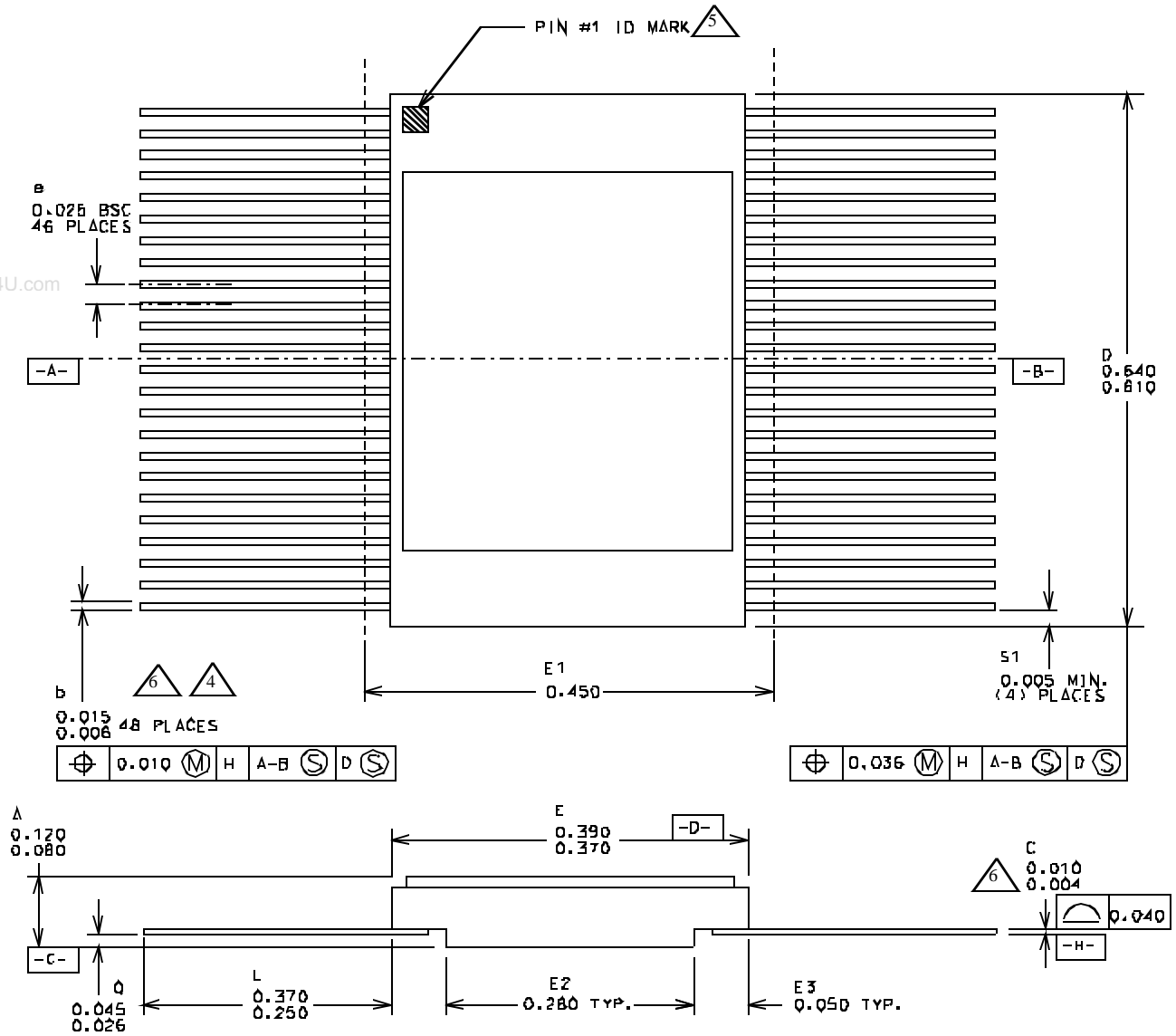
#### Propagation Delay



#### Enable Disable Times



# PACKAGE

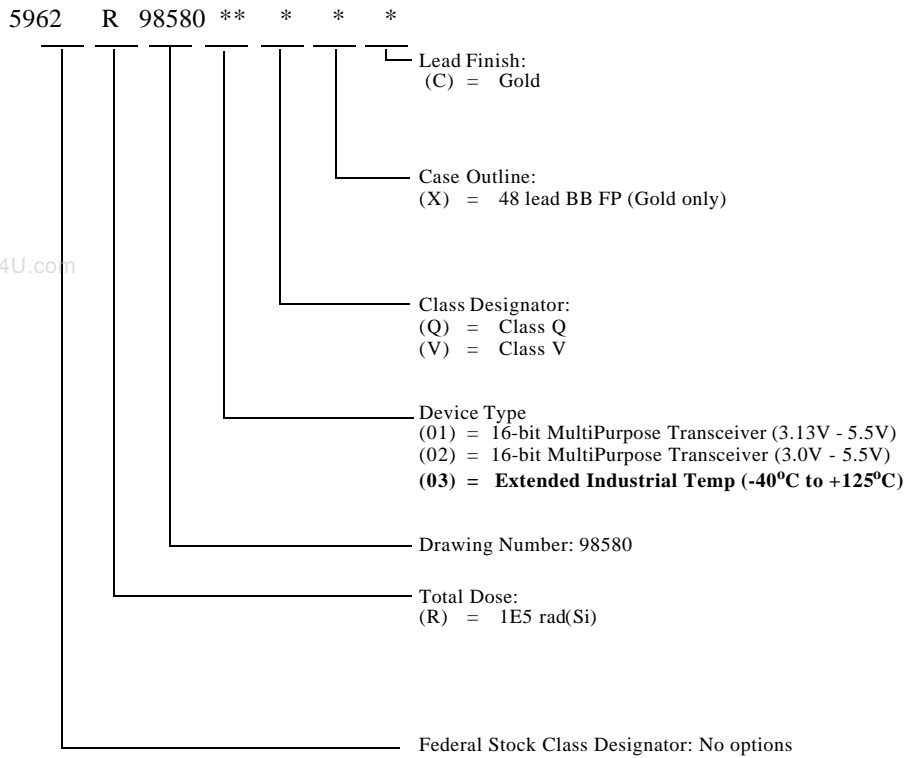


1. All exposed metallized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2. The lid is electrically connected to VSS.
3. Lead finishes are in accordance with MIL-PRF-38535.
4. Lead position and colanarity are not measured.
5. ID mark symbol is vendor option.
6. With solder, increase maximum by 0.003.

Figure 1. 48-Lead Flatpack

# ORDERING INFORMATION

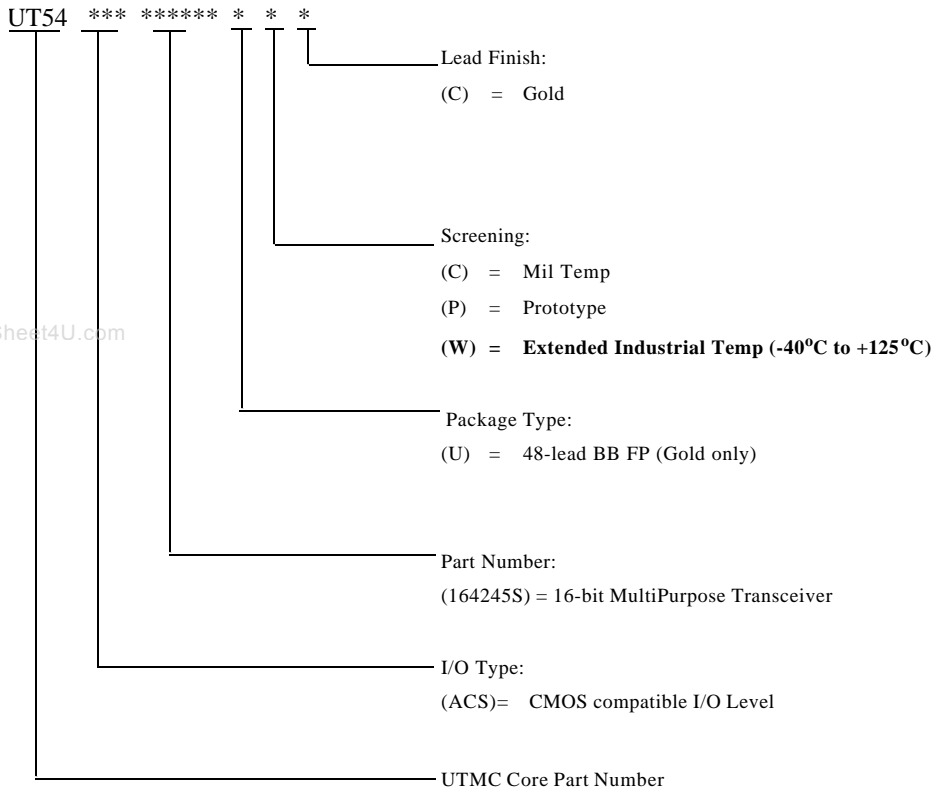
## UT54ACS164245S: SMD



### Notes:

1. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.

# UT54ACS164245S



### Notes:

1. Military Temperature Range flow per UTMC Manufacturing Flows Document. Devices are tested -55C, room temp, and 125C. Radiation n either tested nor guaranteed.
2. Prototype flow per UTMC Manufacturing Flows Document Tested at 25C only. Lead finish is gold only.
3. **Extended Industrial Temperature Range Flow per UTMC Manufacturing Flows Document. Devices are tested at -40°C, room temp, and +125°C. Radiation is neither tested nor guaranteed**

