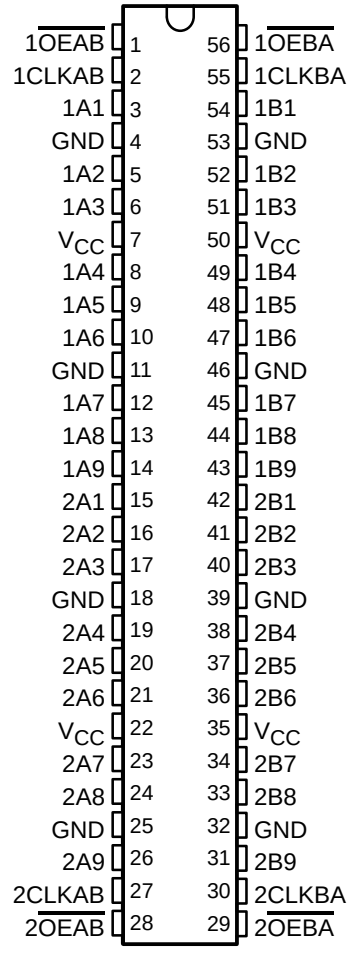
- **Members of the Texas Instruments *Widebus*™ Family**
- **Inputs Are TTL-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings**

54ACT16474 . . . WD PACKAGE
74ACT16474 . . . DL PACKAGE
(TOP VIEW)



description

The ’ACT16474 are noninverting 18-bit registered bus transceivers composed of two 9-bit sections with separate control signals. For either 9-bit transceiver section, data flow in the A-to-B mode is controlled by output-enable (1$\overline{\text{OEAB}}$ or 2$\overline{\text{OEAB}}$) and clock (1CLKAB or 2CLKAB) inputs. When 1$\overline{\text{OEAB}}$ or 2$\overline{\text{OEAB}}$ is low, the corresponding outputs are active (high or low) and take on either the current data on low-to-high transition of 1CLKAB or 2CLKAB or the previously stored data if 1CLKAB or 2CLKAB is low.

When 1$\overline{\text{OEAB}}$ or 2$\overline{\text{OEAB}}$ is high, the corresponding outputs are in the high-impedance state. 1$\overline{\text{OEAB}}$ or 2$\overline{\text{OEAB}}$ does not affect the operation on the internal registers. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

Data flow from B to A is similar, but uses 1$\overline{\text{OEBA}}$ and/or 2$\overline{\text{OEBA}}$ and 1CLKBA and/or 2CLKBA.

The 74ACT16474 is packaged in TI’s shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16474 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT16474 is characterized for operation from –40°C to 85°C.

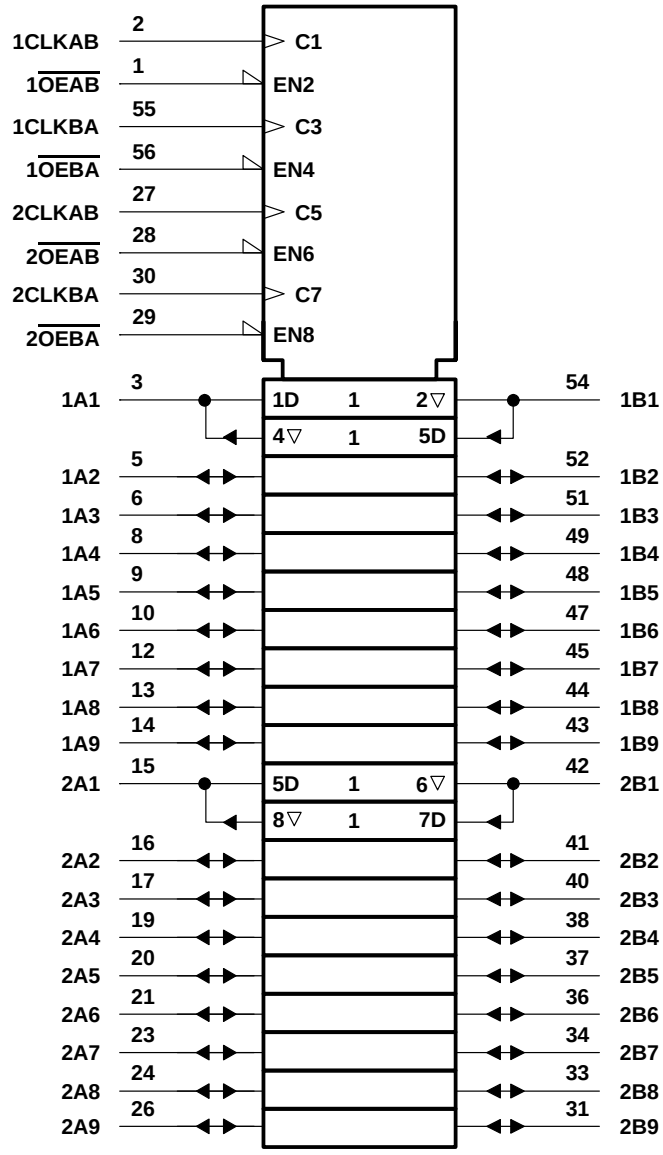
FUNCTION TABLE†

INPUTS			OUTPUT
CLKAB	OEAB	A	B
X	H	X	Z
L	L	X	B_0‡
↑	L	H	H
↑	L	L	L

† A-to-B data flow is shown: B-to-A flow is similar but uses CLKBA, and $\overline{\text{OEBA}}$.

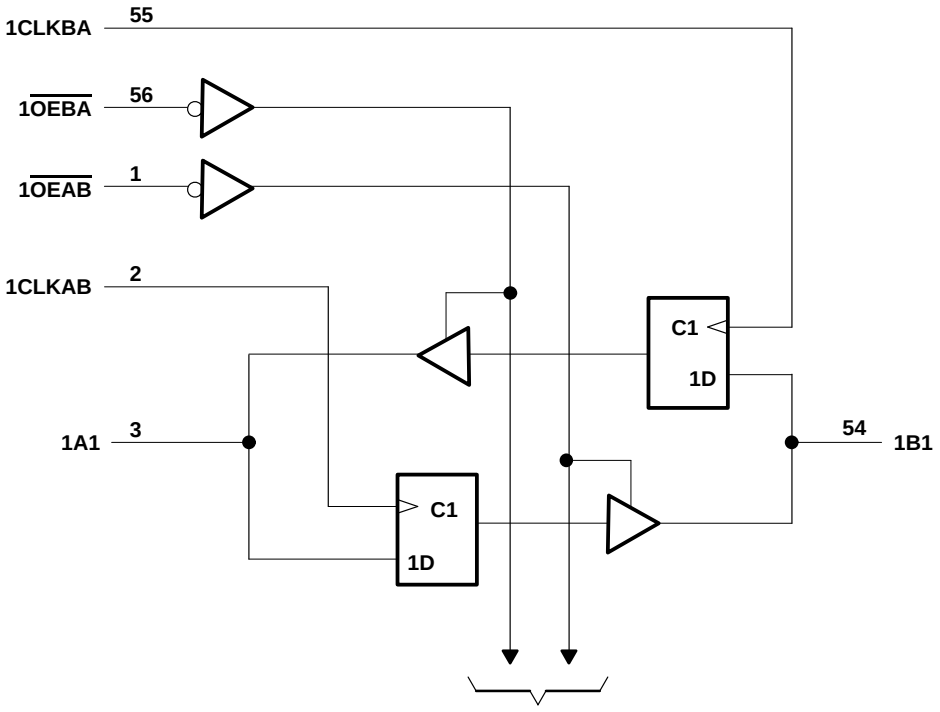
‡ Output level before the indicated steady-state input conditions were established

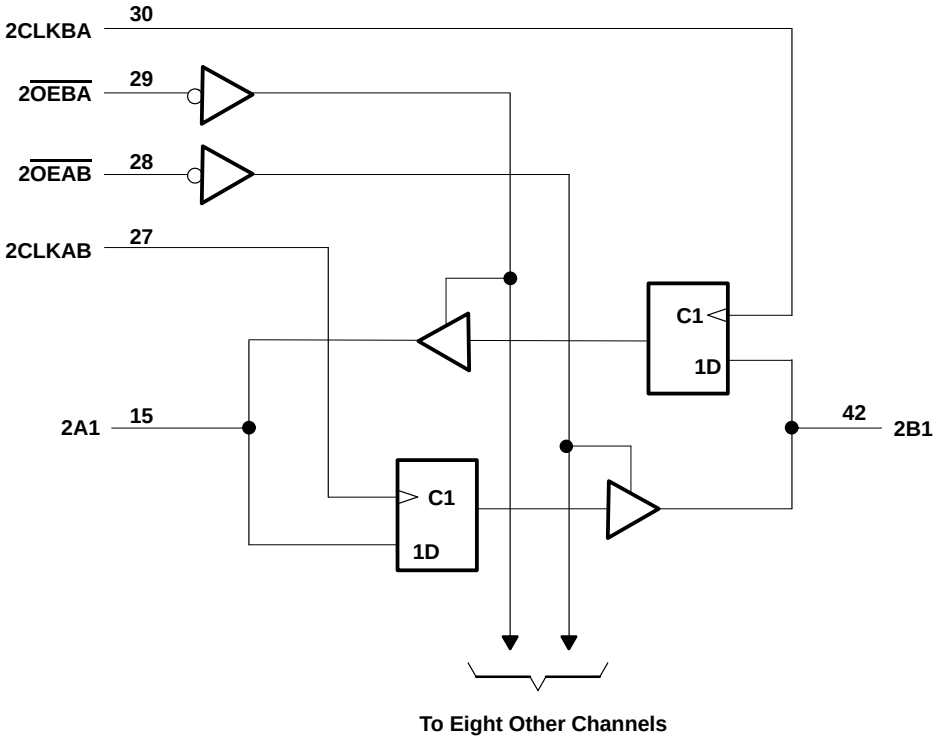
logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 to V_{CC} + 0.5 V
Input voltage range, V_O (see Note 1) . . . . . –0.5 to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±450 mA
Maximum package power dissipation at T_A = 55°C (in still air) (see Note 2): DL package . . . . . 1.4 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

		54ACT16474			74ACT16474			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			–24			–24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	–55		125	–40		85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT16474		74ACT16474		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 µA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_{OH} = –24 mA	4.5 V	3.94			3.8		3.8		
			5.5 V	4.94			4.8		4.8		
		I_{OH} = –75 mA†	5.5 V				3.85		3.85		
V_{OL}		I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.44		0.44	
			5.5 V			0.36		0.44		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65		1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	µA
I_{OZ}‡	A or B ports	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5		±5	µA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80		80	µA
ΔI_{CC}§		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		3						pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		11.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		54ACT16474		74ACT16474		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	75	0	75	0	75	MHz
t_w	Pulse duration	CLK high	4		4		4		ns
		CLK low	6.6		6.6		6.6		
t_{su}	Setup time	Data before CLK↑	5.5		5.5		5.5		ns
t_h	Hold time	Data after CLK↑	1		1		1		ns

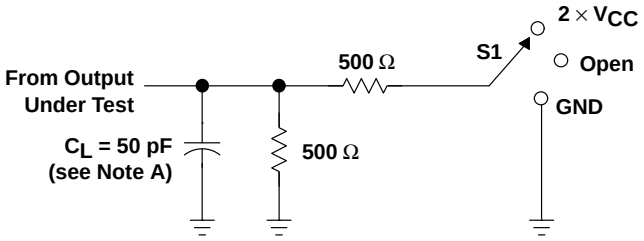
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT16474		74ACT16474		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			75			75		75		MHz
t_{PLH}	CLK	A or B	4	8	10.2	4	11.5	4	11.5	ns
t_{PHL}			4.2	8	10.2	4.2	11.4	4.2	11.4	
t_{PZH}	$\overline{OE}$	A or B	3	7.8	10.3	3	11.7	3	11.7	ns
t_{PZL}			3.7	9.2	11.6	3.7	13.1	3.7	13.1	
t_{PHZ}	$\overline{OE}$	A or B	4.8	7.1	8.8	4.8	9.5	4.8	9.5	ns
t_{PLZ}			4.4	6.6	8.4	4.4	9	4.4	9	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

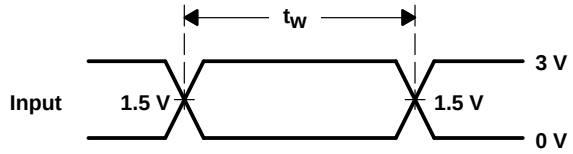
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	61	pF
		Outputs disabled		37	

PARAMETER MEASUREMENT INFORMATION

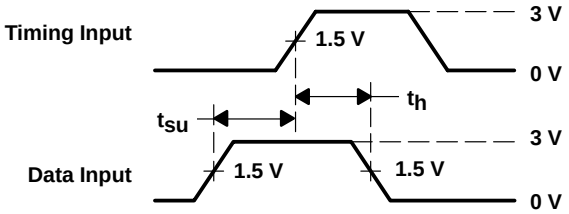


LOAD CIRCUIT

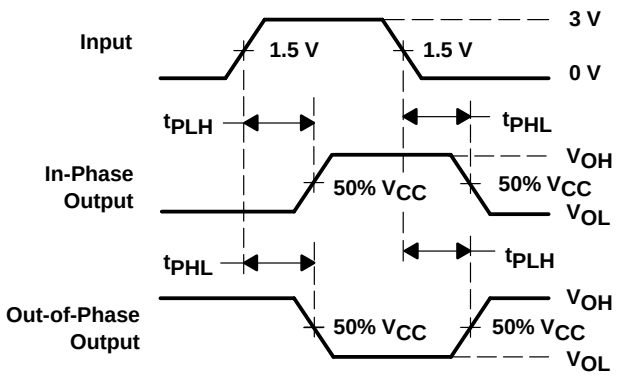
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



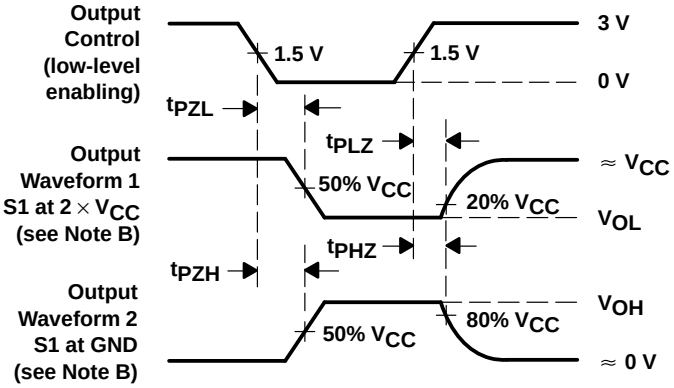
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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