- **Members of the Texas Instruments Widebus™ Family**
- **Inputs Are TTL-Voltage Compatible**
- **Provide Extra Data Width Necessary for Wider Address/Data Paths**
- **Provide Inverted Data**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-µm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Shrink Small-Outline 300-mil (DL) Package Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings**

54ACT16540 . . . WD PACKAGE
74ACT16540 . . . DL PACKAGE
(TOP VIEW)

$1\overline{OE1}$	1	48	$1\overline{OE2}$
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
V_{CC}	7	42	V_{CC}
1Y5	8	41	1A5
1Y6	9	40	1A6
GND	10	39	GND
1Y7	11	38	1A7
1Y8	12	37	1A8
2Y1	13	36	2A1
2Y2	14	35	2A2
GND	15	34	GND
2Y3	16	33	2A3
2Y4	17	32	2A4
V_{CC}	18	31	V_{CC}
2Y5	19	30	2A5
2Y6	20	29	2A6
GND	21	28	GND
2Y7	22	27	2A7
2Y8	23	26	2A8
$2\overline{OE1}$	24	25	$2\overline{OE2}$

description

These 16-bit buffers/bus drivers provide a high-performance bus interface for wide data paths.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state.

The 74ACT16540 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16540 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT16540 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

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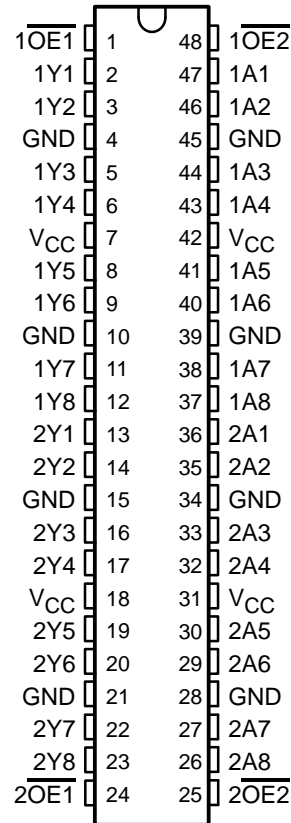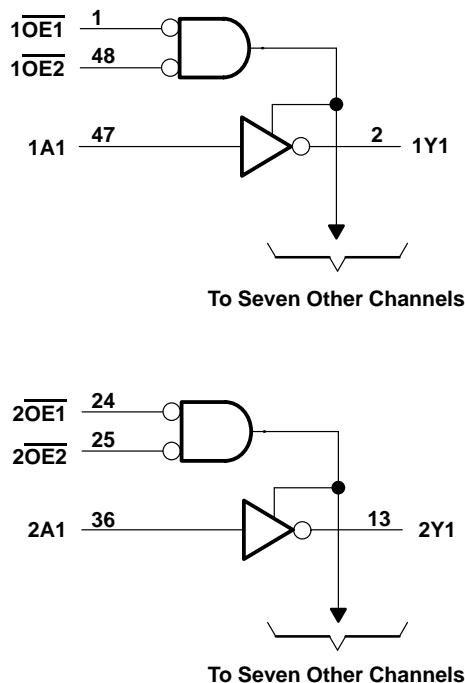EPIC and Widebus are trademarks of Texas Instruments Incorporated.

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54ACT16540, 74ACT16540
16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

SCAS186A – OCTOBER 1991 – REVISED APRIL 1996

logic symbol†

Pin	Signal				Signal	Pin
1	1$\overline{OE1}$	& EN1				
48	1$\overline{OE2}$					
24	2$\overline{OE1}$	& EN2				
25	2$\overline{OE2}$					
47	1A1	1 1▽		2	1Y1	
46	1A2			3	1Y2	
44	1A3			5	1Y3	
43	1A4			6	1Y4	
41	1A5			8	1Y5	
40	1A6			9	1Y6	
38	1A7			11	1Y7	
37	1A8			12	1Y8	
36	2A1	1 2▽		13	2Y1	
35	2A2			14	2Y2	
33	2A3			16	2Y3	
32	2A4			17	2Y4	
30	2A5			19	2Y5	
29	2A6			20	2Y6	
27	2A7			22	2Y7	
26	2A8			23	2Y8	
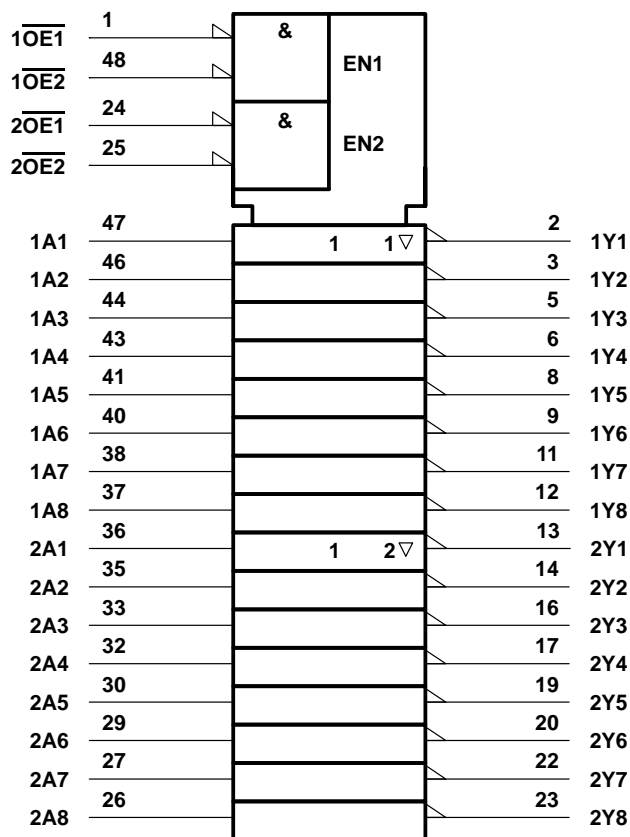
logic diagram (positive logic)

1$\overline{OE1}$ — 1
1$\overline{OE2}$ — 48
1A1 — 47
2 — 1Y1

To Seven Other Channels

2$\overline{OE1}$ — 24
2$\overline{OE2}$ — 25
2A1 — 36
13 — 2Y1

To Seven Other Channels

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) .... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) .... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) .... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±50 mA
Continuous current through V_{CC} or GND .... ±400 mA
Maximum power package dissipation at T_A = 55°C (in still air) (see Note 2): DL package .... 1.2 W
Storage temperature range, T_{stg} .... –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

		54ACT16540			74ACT16540			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	−55		125	−40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25°C$			54ACT16540		74ACT16540		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50\ \mu A$	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	$I_{OH} = -24\ mA$	4.5 V	3.94			3.8		3.8		
		5.5 V	4.94			4.8		4.8		
	$I_{OH} = -75\ mA$†	5.5 V				3.85		3.85		
V_{OL}	$I_{OL} = 50\ \mu A$	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	$I_{OL} = 24\ mA$	4.5 V			0.36		0.44		0.44	
		5.5 V			0.36		0.44		0.44	
	$I_{OL} = 75\ mA$†	5.5 V					1.65		1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5		±5	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		80		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4						pF
C_o	$V_O = V_{CC}$ or GND	5 V		13						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

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switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT16540		74ACT16540		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2.1	5.1	6.8	2.1	7.5	2.1	7.5	ns
t_{PHL}			3.9	6.8	8.5	3.9	9.5	3.9	9.5	
t_{PZH}	$\overline{OE}$	Y	2.7	6.2	8	2.7	8.9	2.7	8.9	ns
t_{PZL}			3.6	7.5	9.5	3.6	10.5	3.6	10.5	
t_{PHZ}	$\overline{OE}$	Y	5.4	9.2	10.9	5.4	11.9	5.4	11.9	ns
t_{PLZ}			5.4	8.6	10.3	5.4	11.1	5.4	11.1	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd} Power dissipation capacitance per buffer	Outputs enabled	C_L = 50 pF,	f = 1 MHz	42	pF
	Outputs disabled			8.5	

PARAMETER MEASUREMENT INFORMATION
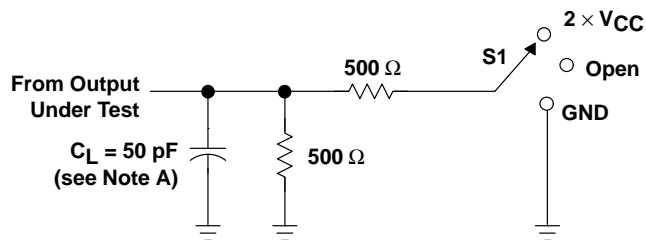
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT
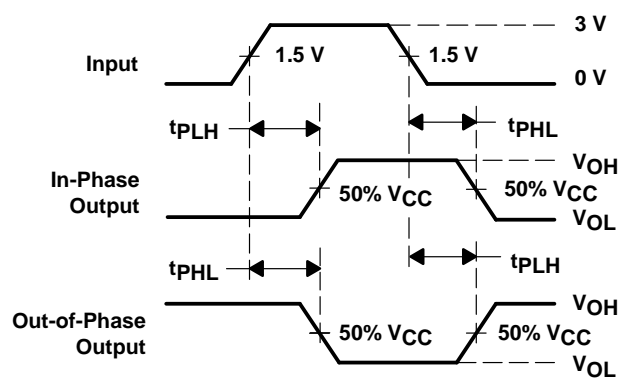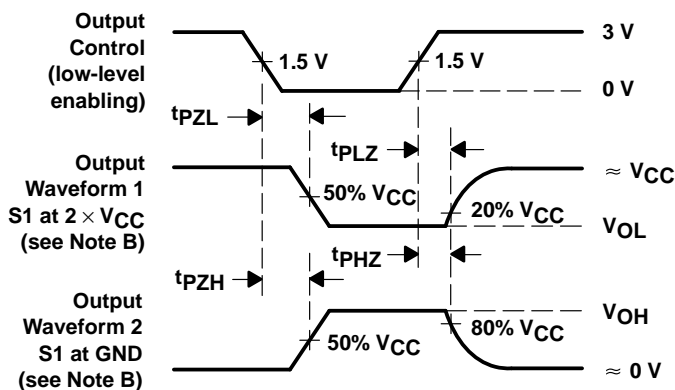
VOLTAGE WAVEFORMS

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
     B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
        Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
     C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
     D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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