- **Members of the Texas Instruments** *Widebus* ™ Family
- Inputs Are TTL-Voltage Compatible
- Flow-Through Architecture Optimizes **PCB Layout**
- Distributed V_{CC} and GND Pin Configuration **Minimizes High-Speed Switching Noise**
- **EPIC™** (Enhanced-Performance Implanted CMOS) 1-µm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Packages **Using 25-mil Center-to-Center Spacings**

description

The 'ACT16640 are inverting 16-bit transceivers designed for asynchronous communication between data buses.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (1DIR and 2DIR) inputs. The output-enable $(1\overline{OE} \text{ and } 2\overline{OE})$ inputs can be used to disable the device so that the buses are effectively isolated.

54ACT16640...WD PACKAGE 74ACT16640 . . . DL PACKAGE (TOP VIEW)

	- 1		П		
1DIR	q	1	\cup	48	10E
1B1	q	2		47] 1A1
1B2	9	3		46] 1A2
GND	q	4		45	GND
1B3	q	5		44] 1A3
1B4	q	6		43] 1A4
V_{CC}	q	7		42] v _{cc}
1B5	q	8		41] 1A5
1B6	q	9		40] 1A6
GND	q	10		39	GND
1B7	q	11		38] 1A7
1B8	q	12		37] 1A8
2B1	q	13		36	2A1
2B2	q	14		35] 2A2
GND	q	15		34	GND
2B3	q	16		33] 2A3
2B4	q	17		32] 2A4
V_{CC}	q	18		31] v _{cc}
2B5	9	19		30] 2A5
2B6	q	20		29] 2A6
GND	9	21		28	GND
2B7	9	22		27	2A7
2B8	\Box	23		26	2 <u>A8</u>
2DIR	9	24		25	2 <u>0E</u>

The 74ACT16640 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16640 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74ACT16640 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each section)

INP	UTS	OPERATION
OE	DIR	OFERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	Χ	Isolation

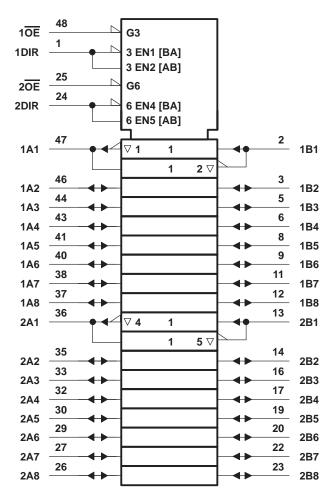


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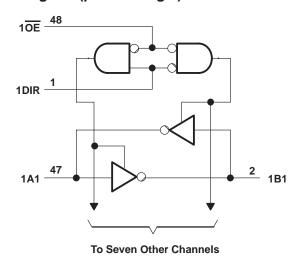


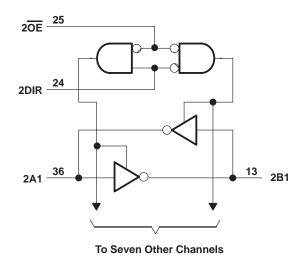
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)







absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	–0.5 V to 7 V
Input voltage range, V _I (see Note 1)($0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, V _O (see Note 1)	$0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND	±400 mA
Maximum package power dissipation at T _A = 55°C (in still air) (see Note 2): DL package	1.2 W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

		54ACT16640			74ACT16640			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2		7	2			V
V _{IL}	Low-level input voltage	0.8				0.8	V	
٧ _I	Input voltage	0	200	VCC	0		VCC	V
٧o	Output voltage	0	7	VCC	0		VCC	V
loh	High-level output current		3	-24			-24	mA
loL	Low-level output current	0	5	24			24	mA
Δt/Δν	Input transition rise or fall rate	90		10	0		10	ns/V
T _A	Operating free-air temperature	-55		125	-40		85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^{2.} The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V	T,	ղ = 25°C	;	54ACT16640		74ACT16640		UNIT
		TEST CONDITIONS	vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	ONT
		10.1 - 50.11A	4.5 V	4.4			4.4		4.4		
		I _{OH} = -50 μA	5.5 V	5.4			5.4		5.4		
Vон		1011 - 24 mA	4.5 V	3.94			3.8		3.8		V
		$I_{OH} = -24 \text{ mA}$	5.5 V	4.94			4.8		4.8		
		$I_{OH} = -75 \text{ mA}^{\dagger}$ 5					3.85	N.	3.85		
		10. – 50 uA	4.5 V			0.1		0.1		0.1	V
		I _{OL} = 50 μA	5.5 V			0.1		0.1		0.1	
VOL		la. 24 mA	4.5 V			0.36	, C)	0.44		0.44	
		I _{OL} = 24 mA	5.5 V			0.36	20	0.44		0.44	
		I _{OL} = 75 mA [†]	5.5 V				P _O	1.65		1.65	
II	Control inputs	V _I = V _{CC} or GND	5.5 V			±1	V	±1		±1	μΑ
loz‡	A or B ports	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5		±5	μΑ
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		80		80	μΑ
ΔICC§		One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			0.9		1		1	mA
Ci	Control inputs	V _I = V _{CC} or GND	5 V		4.5						pF
C _{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		16						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)	T _A = 25°C			54ACT16640		74ACT16640		UNIT
PARAMETER	(INPUT)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
^t PLH	A or B	B or A	2.2	6	8.3	2.2	9.1	2.2	9.1	ns
^t PHL			4.1	7.6	9.3	4.1	10.5	4.1	10.5	
^t PZH	ŌĒ	A or B	2.7	6.9	8.9	2.7	9.8	2.7	9.8	ns
t _{PZL}			3.5	8.2	10.4	3.5	11.5	3.5	11.5	
t _{PHZ}	ŌĒ	A or B	6.1	9.4	11.4	6.1	12.5	6.1	12.5	no
^t PLZ	OE		5.5	8.7	10.3	5.5	11	5.5	11	ns

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

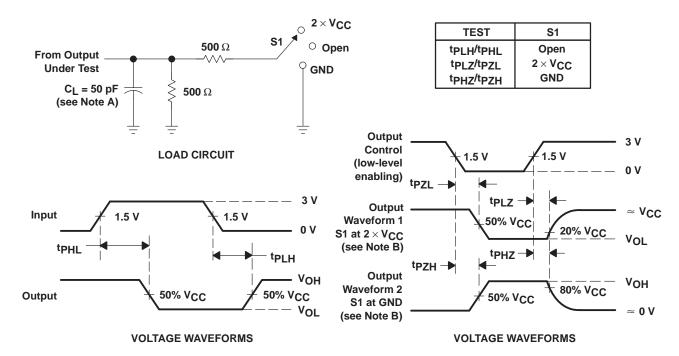
	PARAMETER				TEST CONDITIONS		
		Dower discipation conscitance per transceiver	Outputs enabled	C 50 pE	£ 4 NALI-	52	
Cpd	Power dissipation capacitance per transceiver	Outputs disabled	$C_L = 50 \text{ pF},$	f = 1 MHz	9	pF	



 $[\]mbox{\ensuremath{\mbox{\,^{\dag}}}}\xspace For I/O ports, the parameter I_{OZ} includes the input leakage current.$

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50~\Omega$, $t_f = 3~ns$, $t_f = 3~ns$.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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