National Semiconductor

April 1993

54ACTQ/74ACTQ16245 16-Bit Transceiver with TRI-STATE® Outputs

General Description

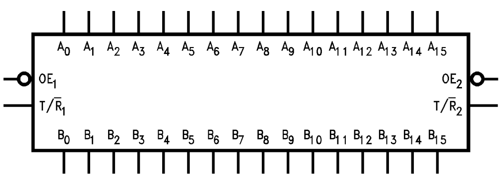
The 'ACTQ16245 contains sixteen non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus oriented applications. The device is byte controlled. Each has separate control inputs which can be shorted together for full 16-bit operation. The T/$\overline{R}$ inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable both the A and B ports by placing them in a high impedance state.

The 'ACTQ16245 utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control for superior performance.

Features

- Utilizes NSC FACT Quiet Series technology
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin output skew
- Bidirectional non-inverting buffers
- Separate control logic for each byte
- 16-bit version of the 'ACTQ245
- Outputs source/sink 24 mA
- Additional specs for multiple output switching
- Output loading specs for both 50 pF and 250 pF loads

Logic Symbol



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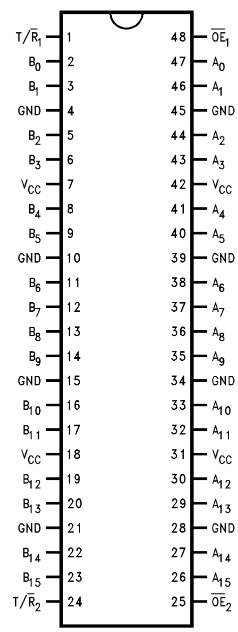
Pin Description

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
T/$\overline{R}$	Transmit/Receive Input
A_0–A_{15}	Side A Inputs/Outputs
B_0–B_{15}	Side B Outputs/Inputs

Connection Diagram

Pin Assignment for SSOP and CERPAK



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RRD-B30M75/Printed in U. S. A.

Functional Description

The 'ACTQ16245 contains sixteen non-inverting bidirectional buffers with TRI-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the $T/\overline{R}$ input is HIGH, then Bus A data is transmitted to Bus B. When the $T/\overline{R}$ input is LOW, Bus B data is transmitted to Bus A. The TRI-STATE outputs are controlled by an Output Enable ($\overline{OE}_n$) input for each byte. When $\overline{OE}_n$ is LOW, the outputs are in 2-state mode. When $\overline{OE}_n$ is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

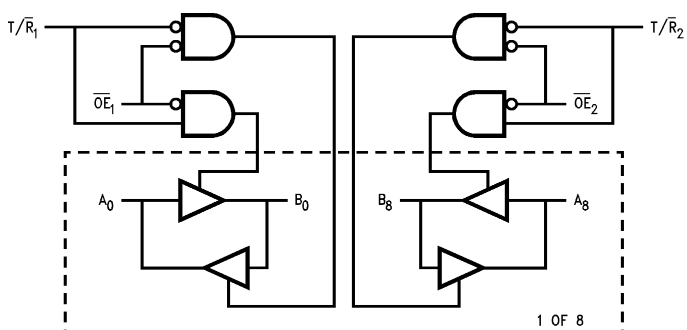
Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$T/\overline{R}_1$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH-Z State on A_0–A_7, B_0–B_7

Inputs		Outputs
$\overline{OE}_2$	$T/\overline{R}_2$	
L	L	Bus B_8–B_{15} Data to Bus A_8–A_{15}
L	H	Bus A_8–A_{15} Data to Bus B_8–B_{15}
H	X	HIGH-Z State on A_8–A_{15}, B_8–B_{15}

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	$-0.5V$ to $+7.0V$
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	$+20$ mA
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	$+20$ mA
DC Output Voltage (V_O)	$-0.5V$ to $V_{CC} + 0.5V$
DC Output Source/Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current per Output Pin	± 50 mA
Junction Temperature	
C-DIP	$+175°C$
PDIP/SOIC	$+140°C$
Storage Temperature	$-65°C$ to $+150°C$

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception to ensure that the system design is reliable over its power supply, temperature, and output/input loading varaibles. National does not recommend operation of FACT™ circuits outside databook specifications.

Note 2: For qualification information please refer to the NSC SSOP Qualification Handbook.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACTQ	$-40°C$ to $+85°C$
54ACTQ	$-55°C$ to $+125°C$
Minimum Input Edge Rate (dV/dt)	
'ACTQ Devices	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

DC Electrical Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$		54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{IL}	Maximum Low Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{OH}	Minimum High Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	$I_{OUT} = -50\ \mu A$
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	$V_{IN}* = V_{IL}$ or V_{IH} I_{OH} -24 mA -24 mA
V_{OL}	Maximum Low Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	$I_{OUT} = 50\ \mu A$
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	$V_{IN}* = V_{IL}$ or V_{IH} I_{OL} 24 mA 24 mA
I_{OZT}	Maximum I/O Leakage Current	5.5		± 0.5	± 10.0	± 5.0	μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}$, GND
I_{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	± 1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC} - 2.1V$
I_{CC}	Max Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 5)
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}					50	-75	mA	$V_{OHD} = 3.85V$ Min

* All outputs loaded; thresholds associated with output under test.

†Maximum test duration 2.0 ms; one output loaded at a time.

DC Electrical Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACTQ		54ACTQ	74ACTQ	Units	Conditions
			$T_A = +25°C$		$T_A =$ $-55°C$ to $+125°C$	$T_A =$ $-40°C$ to $+85°C$		
			Typ	Guaranteed Limits				
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	0.5	0.8			V	*Figures 2-12, 13* (Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.5	−0.85			V	*Figures 2-12, 13* (Notes 2, 3)
V_{OHP}	Maximum Overshoot	5.0	$V_{OH} + 1.0$	$V_{OH} + 1.5$			V	*Figures 2-12, 13* (Notes 1, 3)
V_{OHV}	Minimum V_{CC} Droop	5.0	$V_{OH} - 1.0$	$V_{OH} - 1.8$			V	*Figures 2-12, 13* (Notes 1, 3)
V_{IHD}	Minimum High Dynamic Input Voltage Level	5.0	1.7	2.0			V	(Notes 1, 4)
V_{ILD}	Maximum Low Dynamic Input Voltage Level	5.0	1.2	0.8			V	(Notes 1, 4)

Note 1: Worst case package.

Note 2: Maximum number of outputs that can switch simultaneously is n. (n − 1) outputs are switched LOW and one output held LOW.

Note 3: Maximum number of outputs that can switch simultaneously is n. (n − 1) outputs are switched HIGH and one output held HIGH.

Note 4: Max number of data inputs (n) switching. (n − 1) input switching 0V to 3V ('ACTQ) input under test switching 3V to threshold (V_{ILD})

Note 5: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACTQ			54ACTQ		74ACTQ		Units
			$T_A = +25°C$ $C_L = 50$ pF			$T_A =$ $-55°C$ to $+125°C$ $C_L = 50$ pF		$T_A =$ $-40°C$ to $+85°C$ $C_L = 50$ pF		
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay A_n, B_n to B_n, A_n	5.0	3.2 2.6	5.7 5.1	8.4 7.9	3.2 2.6	9.4 8.7	3.2 2.6	9.0 8.4	ns
t_{PZH}, t_{PZL}	Output Enable Time	5.0	3.7 4.1	6.4 7.4	9.4 10.5	3.7 4.1		2.7 3.4	10.0 11.6	ns
t_{PHZ}, t_{PLZ}	Output Disable Time	5.0	2.2 2.0	5.4 5.2	8.7 8.2	2.2 2.0	9.5 9.1	2.2 2.0	9.3 8.8	ns

* Voltage Range 5.0 is 5.0V ±0.5V.

Extended AC Electrical Characteristics

Symbol	Parameter	74ACTQ			54ACTQ		74ACTQ		54ACTQ		Units
		$T_A = -40°C$ to $+85°C$ V_{CC} = Com $C_L = 50$ pF 16 Outputs Switching (Note 2)			T_A = Mil V_{CC} = Mil $C_L = 50$ pF 16 Outputs Switching (Note 2)		$T_A = -40°C$ to $+85°C$ V_{CC} = Com $C_L = 250$ pF (Note 3)		T_A = Mil V_{CC} = Mil $C_L = 250$ pF (Note 3)		
		Min	Typ	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Data to Output	4.2 3.5		11.9 9.9	4.2 3.5	12.5 10.3	5.9 5.0	14.6 13.4	5.9 5.0	15.3 13.9	ns
t_{PZH} t_{PZL}	Output Enable Time	4.5 4.4		11.4 12.2	4.5 4.4	12.2 13.0	(Note 4)		(Note 4)		ns
t_{PHZ} t_{PZL}	Output Disable Time	3.5 3.1		9.3 8.8	3.5 3.1	9.5 9.1	(Note 5)		(Note 5)		ns
t_{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output			1.2							ns
t_{OSLH} (Note 1)	Pin to Pin Skew LH Data to Output			1.3							ns
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Data to Output			3.0							ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}).

Note 2: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 3: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 4: TRI-STATE delays are load dominated and have been excluded from the datasheet.

Note 5: The Output Disable Time is dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Capacitance

Symbol	Parameter		Typ	Units	Conditions
C_{IN}	Input Pin Capacitance		4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	74ACTQ	25	pF	$V_{CC} = 5.0V$
		54ACTQ	95	pF	$V_{CC} = 5.0V$

FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

Hewlett Packard Model 8180A Word Generator
PC-163A Test Fixture
Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the word generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. Swap out the channels that have more than 150 ps of skew until all channels being used are within 150 ps. It is important to deskew the word generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set V_{CC} to 5.0V.
5. Set the word generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.

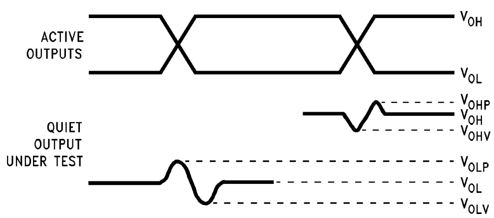

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FIGURE 1. Quiet Output Noise Voltage Waveforms

Note A: V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note B: Input pulses have the following characteristics: f = 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 150 ps.

6. Set the word generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with a digital volt meter.

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output during the HL transition. Measure V_{OHP} and V_{OHV} on the quiet output during the LH transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD}:

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.
- Next increase the input HIGH voltage level on the word generator, V_{IH} until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

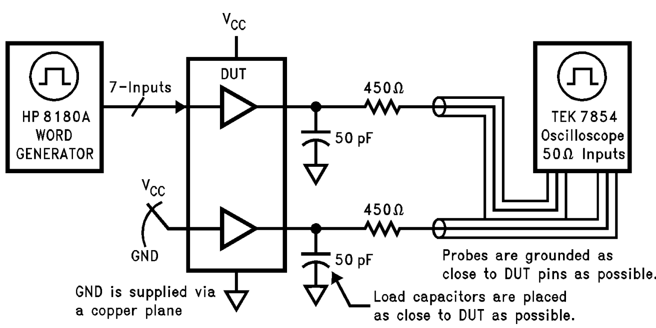

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FIGURE 2. Simultaneous Switching Test Circuit

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

74ACTQ 16245 SS C X

Temperature Range Family
- 74ACTQ = Commercial—TTL Compatible
- 54ACTQ = Military—TTL Compatible

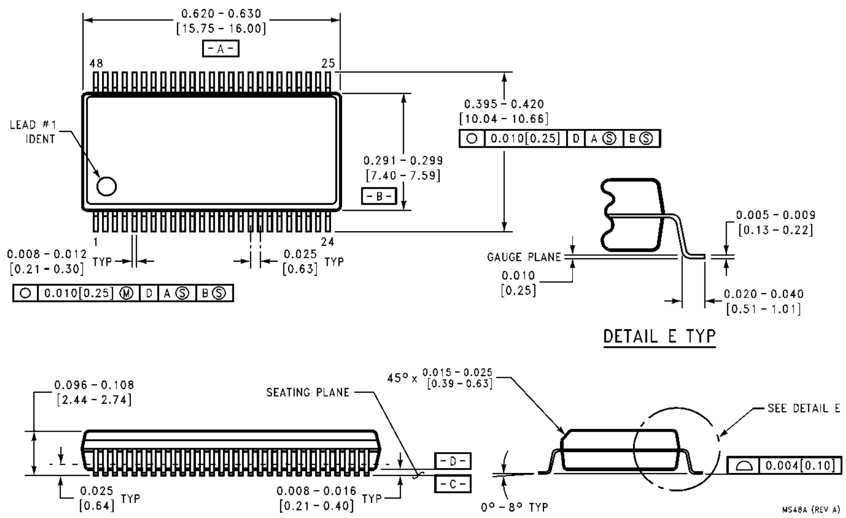
Device Type

Package Code
- SS = Small Outline (SSOP)
- F = CERPAK

Special Variations
- X = Devices shipped in 13″ reels
- QB = 883 Processing

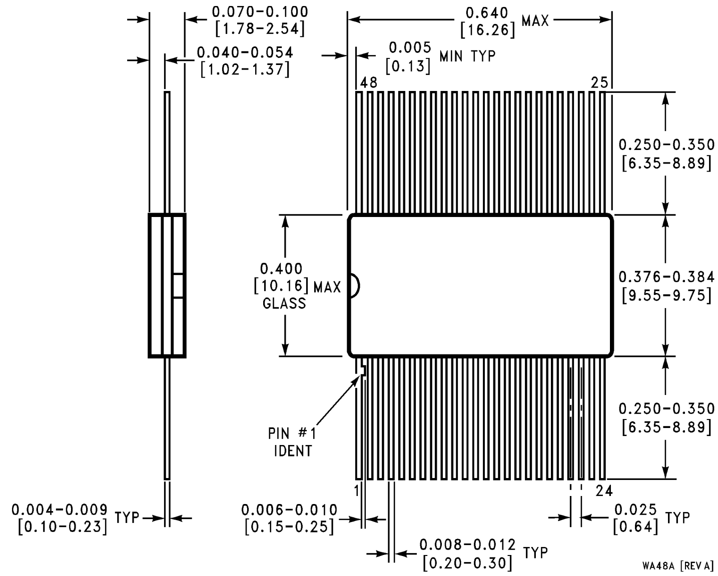
Temperature Range
- C = Commercial Product (−40°C to +85°C)
- M = Military Product (−55°C to +125°C)

Physical Dimensions inches (millimeters)



48-Lead SSOP (0.300″ Wide) (SS)
NS Package Number MS48A

Physical Dimensions (Continued)



48-Lead CERPAK (F)
NS Package Number WA48A

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National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livry-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527649
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Ciba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottinghill, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998