

MM54C915/MM74C915 7-Segment-to-BCD Converter

General Description

The MM54C915/MM74C915 is a monolithic complementary MOS (CMOS) integrated circuit, constructed with N and P-channel enhancement-mode transistors. This circuit accepts 7-segment information and converts it into BCD information. The true state of the Segment inputs can be selected by use of the **Invert/Non-invert** control pin. A logical "0" on the **Invert/Non-invert** control pin selects active high true decoding at the Segment inputs. A logical "1" on the **Invert/Non-invert** control pin selects active low true decoding at the Segment inputs. In addition to 4 TTL compatible BCD outputs, an Error output and Minus output are available. The **Error output** goes to an active "1" whenever a non-standard 7-segment code appears at the Segment inputs. The BCD outputs are forced into a TRI-STATE™ condition when an error is detected. This allows the user to program his own error code by tying the BCD outputs to V_{CC} or Ground via high value resistors (~ 500k). The BCD outputs may also be forced into TRI-STATE by a logical "1" on output enable (**OE**).

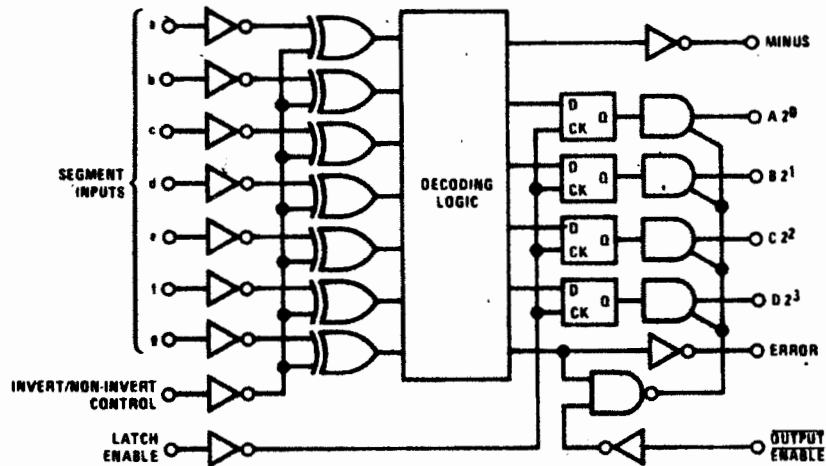
The Minus output goes to a logical "1" whenever a minus code is detected and is useful as a microprocessor interrupt. The BCD outputs are in a flow-through condition when Latch Enable (**LE**) is at a logical "0", and latched when LE is at a logical "1". The inputs will not clamp signals to the positive supply, allowing simple level translation from MOS to TTL.

Features

- Wide supply range
- High noise immunity
- TTL compatible fan out
- Selectable active true inputs
- TRI-STATE outputs
- On-chip latch
- Error output
- Minus output

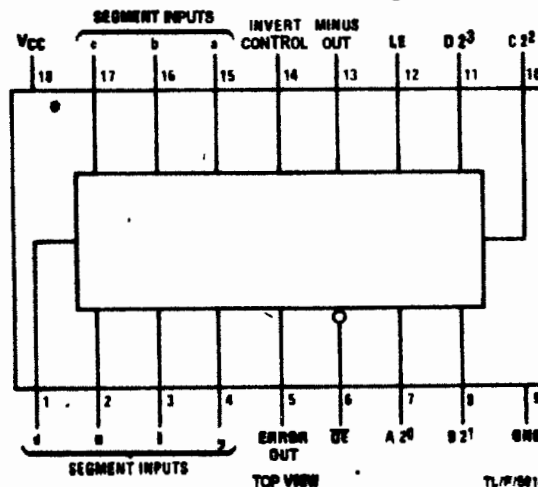
3V–15V
0.45 V_{CC} (typ.)
1 TTL load

Logic and Connection Diagrams



TL/F/5016-1

Dual-In-Line Package



Order Number **MM54C915J** or
MM74C915J
See NS Package **J18A**

Order Number **MM54C915N** or
MM74C915N
See NS Package **N18A**

TL/F/5016-2

Absolute Maximum Ratings

Voltage at Any Output - 0.3V to VCC + 0.3V
 Voltage at Any Input - 0.3V to 18V
 Operating Temperature Range
 MM54C915 -55°C to +125°C
 MM74C915 -40°C to +85°C

Storage Temperature Range -65°C to +150°C
 Package Dissipation 500 mW
 Operating VCC Range 4.0V to 15V
 Maximum VCC 18V
 Lead Temperature, (Soldering, 10 seconds) 300°C

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
VIN(1)	Logical "1" Input Voltage	VCC = 5V VCC = 10V VCC = 15V	3.5 8 12.5			V V V
VIN(0)	Logical "0" Input Voltage	VCC = 5V VCC = 10V VCC = 15V			1.5 2 2.5	V V V
IIN(1)	Logical "1" Input Current	VIN = 15V		0.005	1	µA
IIN(0)	Logical "0" Input Current	VIN = 0V	-1	-0.005		µA
VOUT(1)	Logical "1" Output Voltage	IO = 10 µA VCC = 5V VCC = 10V VCC = 15V	4.5 9 13.5			V V V
VOUT(0)	Logical "0" Output Voltage	IO = 10 µA VCC = 5V VCC = 10V VCC = 15V			0.5 1 1.5	V V V
ICC	Supply Current	VCC = 5V VCC = 10V VCC = 15V		0.25 0.75 1.00	1 2.5 3	mA mA mA

CMOS/FTL INTERFACE

VIN(1)	Logical "1" Input Voltage MM54C915 MM74C915	VCC = 4.5V VCC = 4.75V	VCC-1.7 VCC-1.7			V V
VIN(0)	Logical "0" Input Voltage MM54C915 MM74C915	VCC = 4.5V VCC = 4.75V			0.8 0.8	V V
VOUT(1)	Logical "1" Output Voltage MM54C915 MM74C915	IO = -360 µA VCC = 4.5V VCC = 4.75V	2.4 2.4			V V
VOUT(0)	Logical "0" Output Voltage MM54C915 MM74C915	IO = 1.6 mA VCC = 4.5V VCC = 4.75V			0.4 0.4	V V

OUTPUT DRIVE (Short Circuit Current)

ISOURCE	Output Source Current P-Channel	TA = 25°C, VO = 0V, (Note 2) VCC = 5V VCC = 10V VCC = 15V	-1.75 -8 -15	-3.3 -15 -25		mA mA mA
ISINK	Output Sink Current N-Channel	TA = 25°C, VO = VCC (Note 2) VCC = 5V VCC = 10V VCC = 15V	5 20 30	8 30 50		mA mA mA

AC Electrical Characteristics $T_A = 25^\circ\text{C}$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "0" or a Logical "1"	$C_L = 50\text{ pF}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ $V_{CC} = 15\text{V}$		500 300 300	1000 600 600	ns ns ns
t_{0H}, t_{1H}	Propagation Delay Time From Logical "0" or Logical "1" into High Impedance State	$R_L = 10\text{k}, C_L = 10\text{ pF}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ $V_{CC} = 15\text{V}$		110 75 60	200 130 110	ns ns ns
t_{H0}, t_{H1}	Propagation Delay Time From High Impedance State to a Logical "0" or Logical "1"	$R_L = 10\text{k}, C_L = 50\text{ pF}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ $V_{CC} = 15\text{V}$		150 80 70	250 140 125	ns ns ns
t_s	Input Data Set-Up Time	$C_L = 50\text{ pF}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ $V_{CC} = 15\text{V}$		500 300 300	1000 600 600	ns ns ns
t_H	Input Data Hold Time	$C_L = 50\text{ pF}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ $V_{CC} = 15\text{V}$		-150 -100 -100	0 0 0	ns ns ns
C_{IN}	Input Capacitance	Any Input, (Note 3)		5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance	Any Output, (Note 3)		10		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: These specifications apply to transient operation. It is not meant to imply that the device should be operated at these limits in sustained operation.

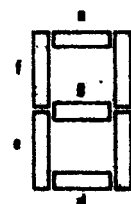
Note 3: Capacitance is guaranteed by periodic testing.

Truth Table

CHARACTER AT SEGMENT INPUTS	BCD OUTPUTS				NON-BCD OUTPUTS	
	D 2^3	C 2^2	B 2^1	A 2^0	ERROR	MINUS
	0	0	0	0	0	0
1	0	0	0	1	0	0
2	0	0	0	1	0	0
3	0	0	1	0	0	0
4	0	0	1	1	0	0
5	0	1	0	0	0	0
6	0	1	0	1	0	0
7	0	1	1	0	0	0
8	0	1	1	1	0	0
9	1	0	0	0	0	0
10	1	0	0	1	0	0
11	1	0	0	1	0	0
12	1	1	1	1	0	0
All other input combinations	X	X	X	X	1	1
	X	X	X	X	1	0
	X	X	X	X	1	0

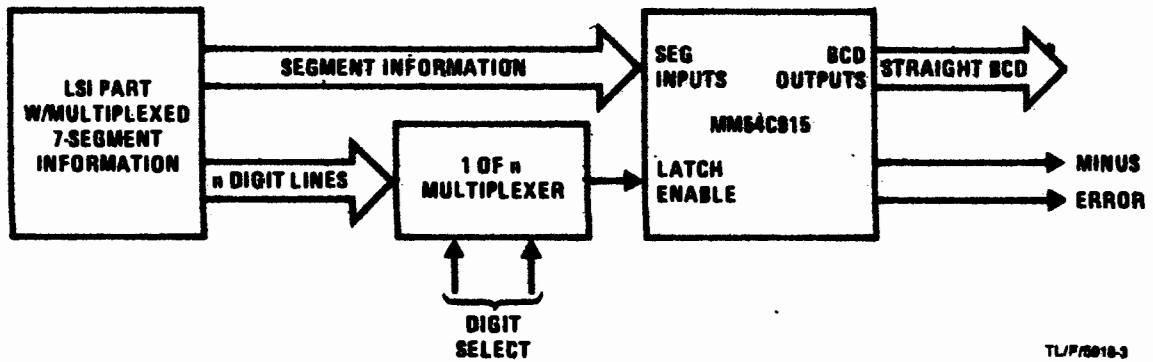
X = represents TRI-STATE condition

SEGMENT IDENTIFICATION



Typical Applications

Multiplex 7-Segment to Straight BCD



Memory Expansion from 7-Segment Outputs

