# SN54F153, SN74F153
# DUAL 1-OF-4 DATA SELECTORS/MULTIPLEXERS

SDFS052A − D2932, MARCH 1987 − REVISED OCTOBER 1993

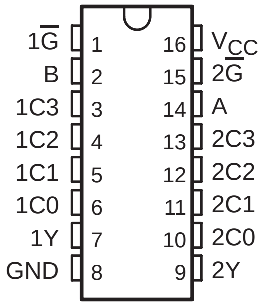
- **Permits Multiplexing From N Lines to One Line**
- **Performs Parallel-to-Serial Conversion**
- **Strobe (Enable) Line Provided for Cascading (N Lines to N Lines)**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

## description

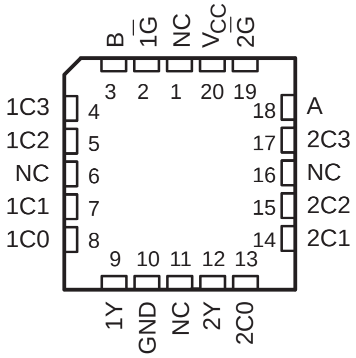
These data selectors/multiplexers contain inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate strobe ($\overline{G}$) inputs are provided for each of the two 4-line sections.

The SN54F153 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F153 is characterized for operation from 0°C to 70°C.

**SN54F153 . . . J PACKAGE**
**SN74F153 . . . D OR N PACKAGE**
**(TOP VIEW)**



**SN54F153 . . . FK PACKAGE**
**(TOP VIEW)**



NC − No internal connection

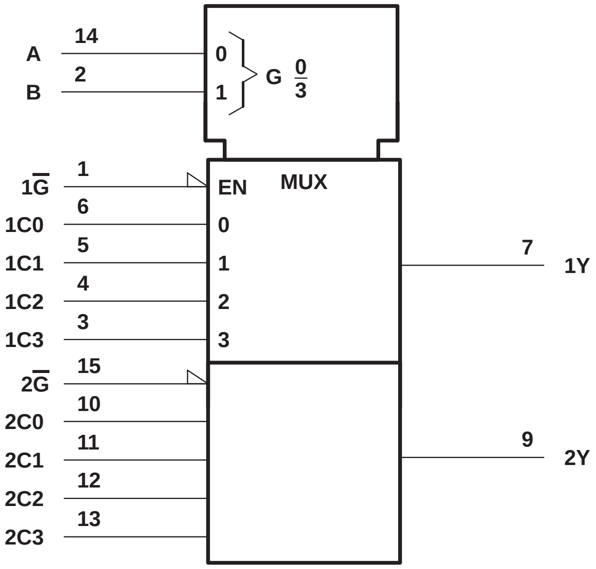
**FUNCTION TABLE**

| INPUTS | | | | | | STROBE | OUTPUT |
|---|---|---|---|---|---|---|---|
| SELECT | | DATA | | | | $\overline{G}$ | Y |
| B | A | C0 | C1 | C2 | C3 | | |
| X | X | X | X | X | X | H | L |
| L | L | L | X | X | X | L | L |
| L | L | H | X | X | X | L | H |
| L | H | X | L | X | X | L | L |
| L | H | X | H | X | X | L | H |
| H | L | X | X | L | X | L | L |
| H | L | X | X | H | X | L | H |
| H | H | X | X | X | L | L | L |
| H | H | X | X | X | H | L | H |

Select inputs A and B are common to both sections.

TEXAS INSTRUMENTS

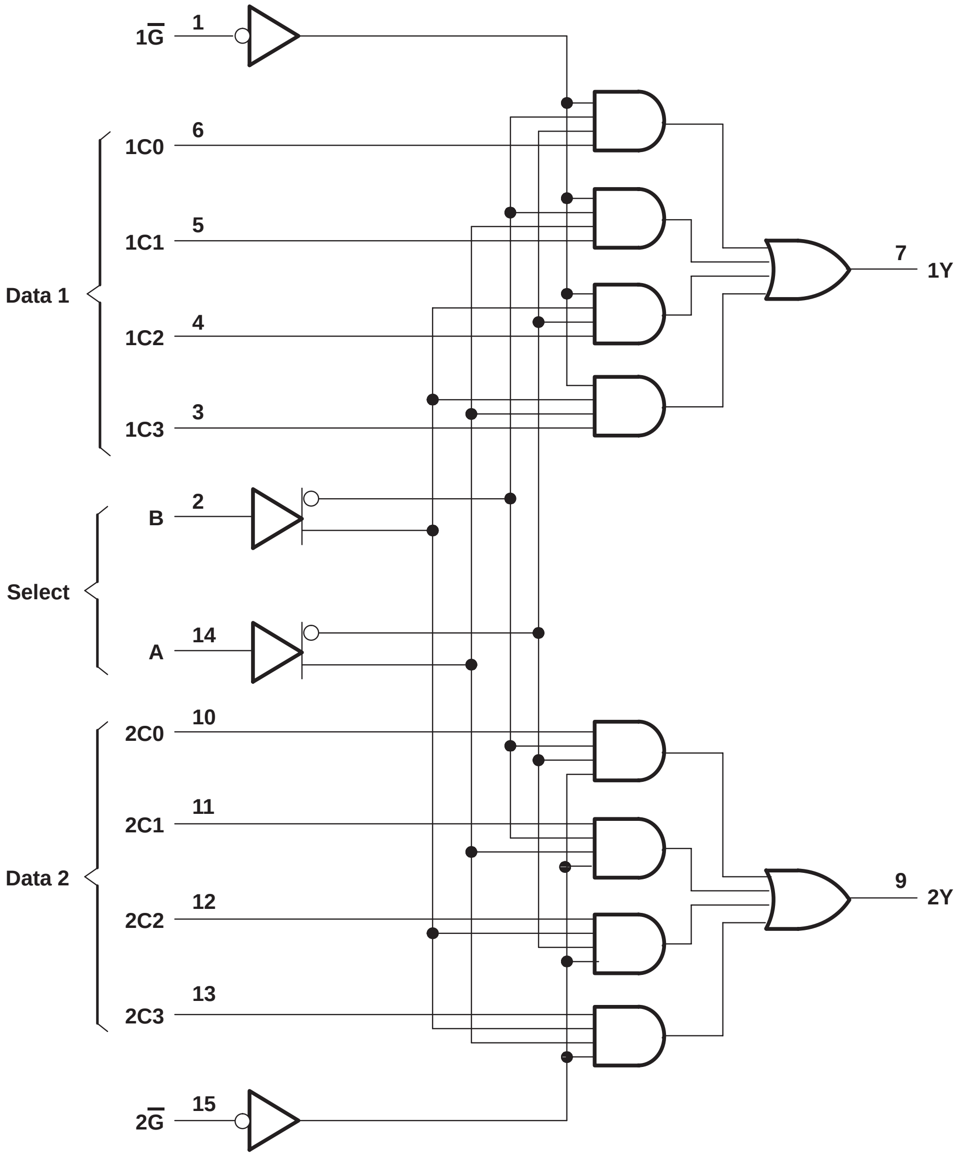
## logic symbol†



---

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

### logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|---|---|
| Supply voltage range, $V_{CC}$ | −0.5 V to 7 V |
| Input voltage range (see Note 1) | −1.2 V to 7 V |
| Input current range | −30 mA to 5 mA |
| Voltage range applied to any output in the high state | −0.5 V to $V_{CC}$ |
| Current into any output in the low state | 40 mA |
| Operating free-air temperature range: SN54F153 | −55°C to 125°C |
| SN74F153 | 0°C to 70°C |
| Storage temperature range | −65°C to 150°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage rating may be exceeded provided that the input current rating is observed.

## recommended operating conditions

| | | SN54F153 | | | SN74F153 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | − 1 | | | − 1 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F153 | | | SN74F153 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP[‡] | MAX | MIN | TYP[‡] | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = − 1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = − 1 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | 0.3 | 0.5 | V |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | − 0.6 | | | − 0.6 | mA |
| $I_{OS}$[§] | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | −60 | | −150 | −60 | | −150 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0 | | 12 | 20 | | 12 | 20 | mA |

[‡] All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | ′F153 | | | SN54F153 | | SN74F153 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | Y | 3.7 | 7.7 | 10.5 | 3.7 | 14 | 3.7 | 12 | ns |
| $t_{PHL}$ | | | 2.7 | 6.6 | 9 | 2.7 | 11 | 2.7 | 10.5 | |
| $t_{PLH}$ | $\overline{G}$ | Y | 3.7 | 6.7 | 9 | 3.7 | 11.5 | 3.7 | 10.5 | ns |
| $t_{PHL}$ | | | 2.2 | 5.3 | 7 | 1.7 | 9 | 1.7 | 8 | |
| $t_{PLH}$ | C | Y | 2.2 | 4.9 | 7 | 1.7 | 9 | 2.2 | 8 | ns |
| $t_{PHL}$ | | | 2.2 | 4.7 | 6.5 | 1.7 | 8 | 1.7 | 7.5 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9758301Q2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-<br>9758301Q2A<br>SNJ54F<br>153FK | Samples |
| 5962-9758301QEA | ACTIVE | CDIP | J | 16 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9758301QE<br>A<br>SNJ54F153J | Samples |
| 5962-9758301QFA | ACTIVE | CFP | W | 16 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9758301QF<br>A<br>SNJ54F153W | Samples |
| JM38510/33902B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/<br>33902B2A | Samples |
| JM38510/33902BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/<br>33902BEA | Samples |
| JM38510/33902BFA | ACTIVE | CFP | W | 16 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/<br>33902BFA | Samples |
| M38510/33902B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/<br>33902B2A | Samples |
| M38510/33902BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/<br>33902BEA | Samples |
| M38510/33902BFA | ACTIVE | CFP | W | 16 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/<br>33902BFA | Samples |
| SN54F153J | ACTIVE | CDIP | J | 16 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | SN54F153J | Samples |
| SN74F153D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | F153 | Samples |
| SN74F153DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | F153 | Samples |
| SN74F153N | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74F153N | Samples |
| SN74F153NSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74F153 | Samples |
| SNJ54F153FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-<br>9758301Q2A<br>SNJ54F | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | 153FK | |
| SNJ54F153J | ACTIVE | CDIP | J | 16 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9758301QEA<br>SNJ54F153J | Samples |
| SNJ54F153W | ACTIVE | CFP | W | 16 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9758301QFA<br>SNJ54F153W | Samples |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54F153, SN74F153 :**

- Catalog: SN74F153

- Military: SN54F153

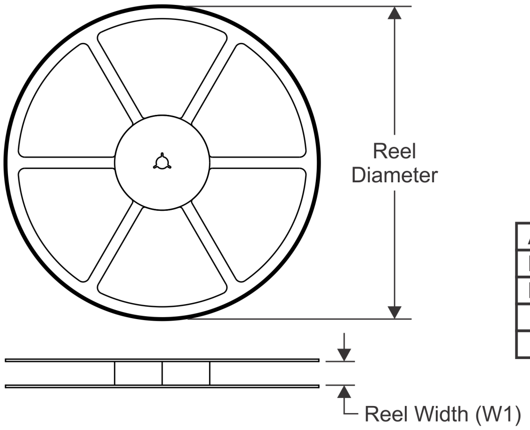
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

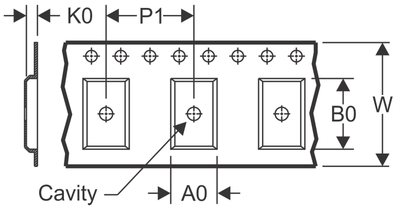
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

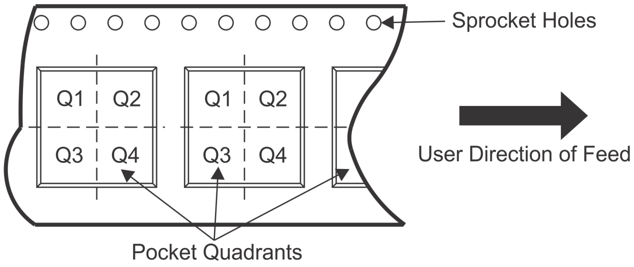


### TAPE DIMENSIONS



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

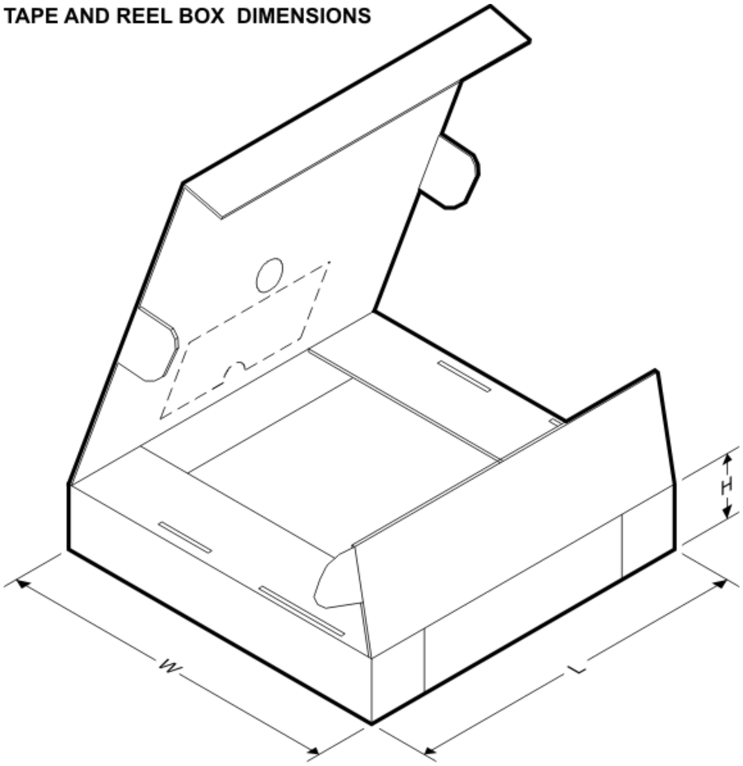
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74F153DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74F153NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

## TAPE AND REEL BOX DIMENSIONS

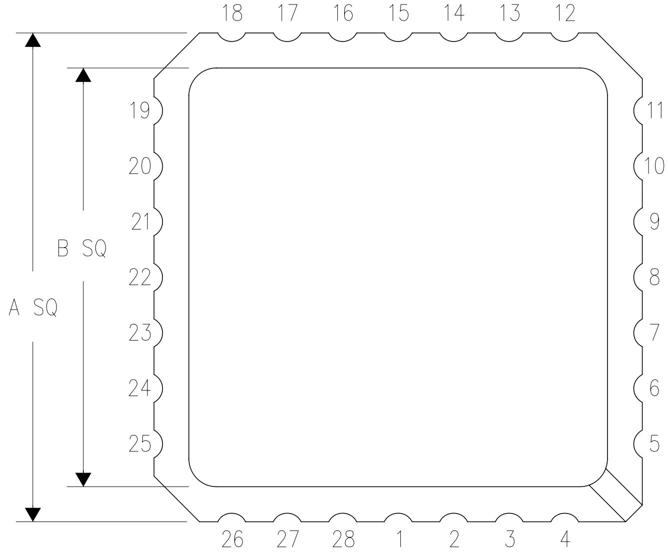


*All dimensions are nominal

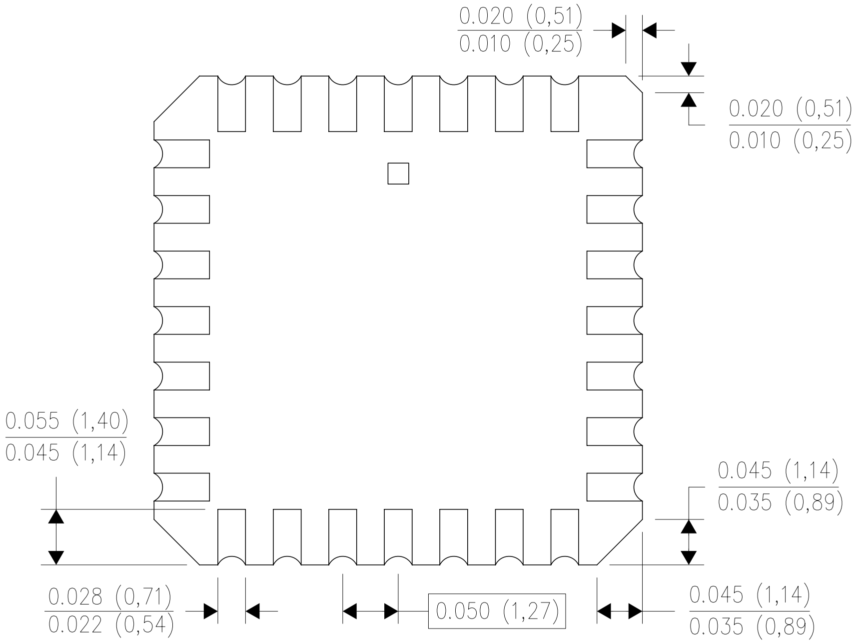
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74F153DR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74F153NSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |

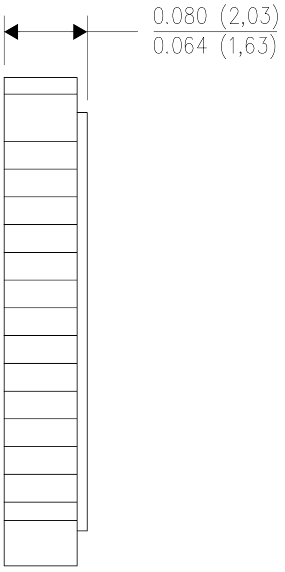
## FK (S-CQCC-N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342<br>(8,69) | 0.358<br>(9,09) | 0.307<br>(7,80) | 0.358<br>(9,09) |
| 28 | 0.442<br>(11,23) | 0.458<br>(11,63) | 0.406<br>(10,31) | 0.458<br>(11,63) |
| 44 | 0.640<br>(16,26) | 0.660<br>(16,76) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 52 | 0.740<br>(18,78) | 0.761<br>(19,32) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 68 | 0.938<br>(23,83) | 0.962<br>(24,43) | 0.850<br>(21,6) | 0.858<br>(21,8) |
| 84 | 1.141<br>(28,99) | 1.165<br>(29,59) | 1.047<br>(26,6) | 1.063<br>(27,0) |

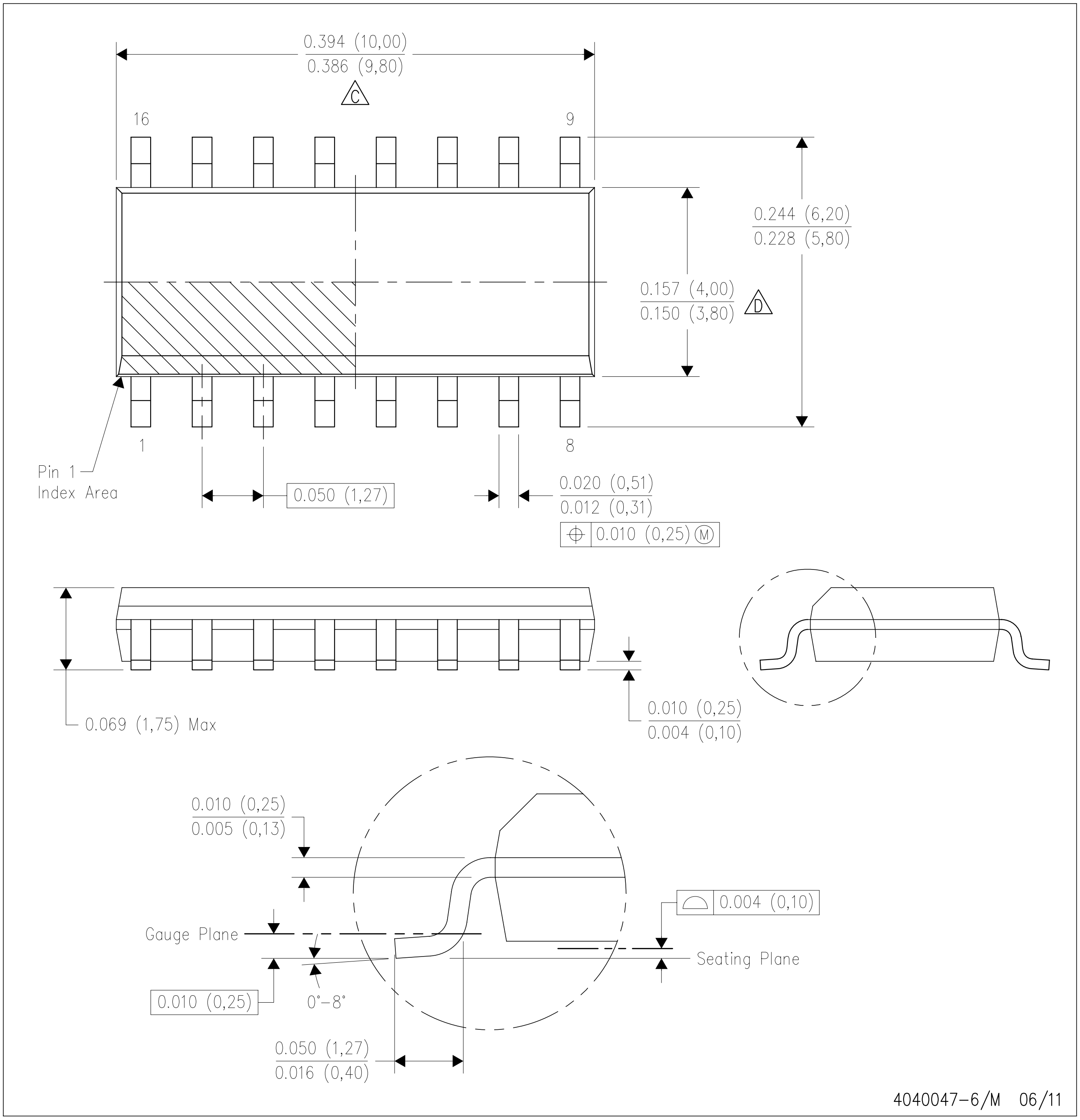




4040140/D 01/11

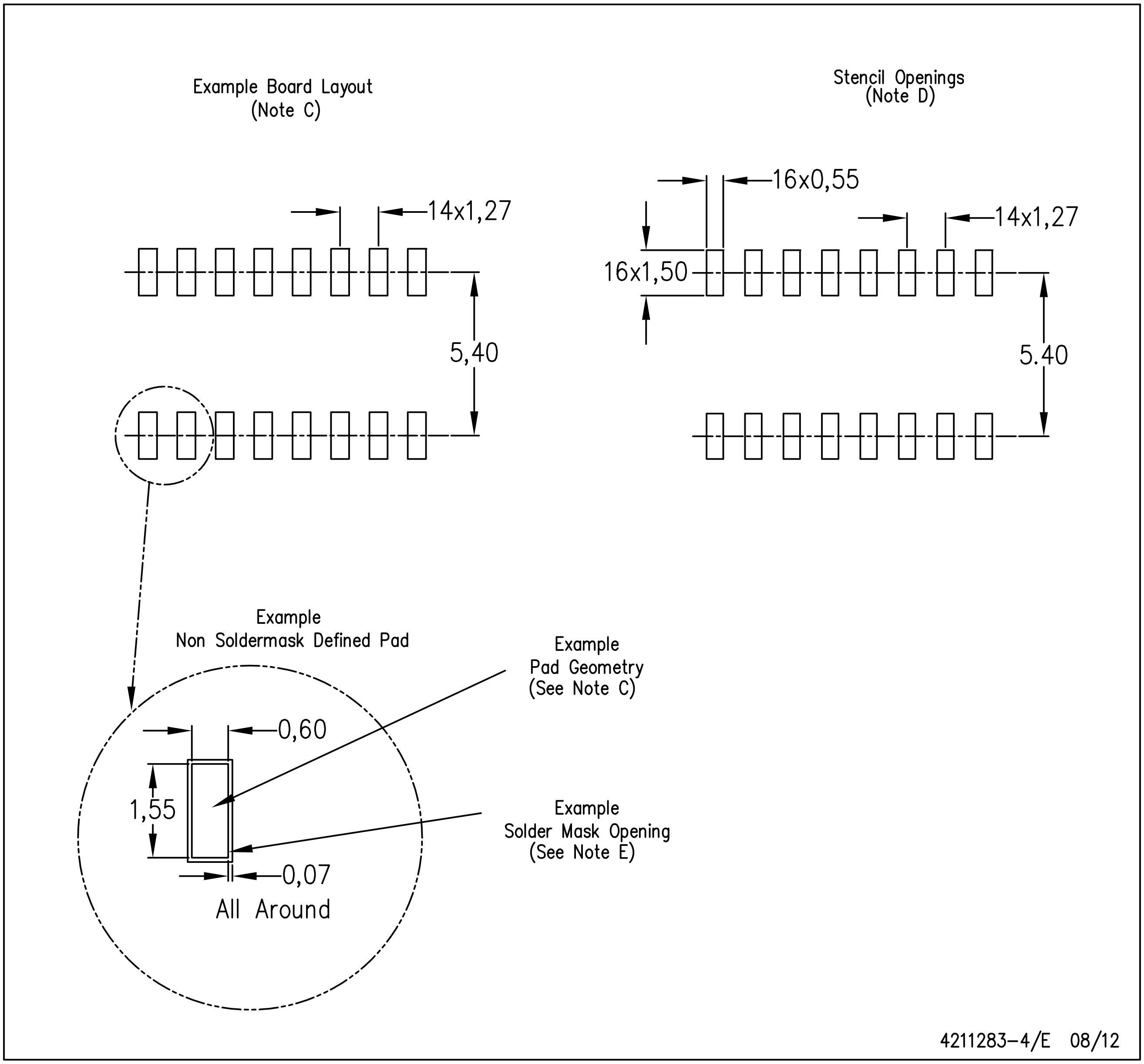
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

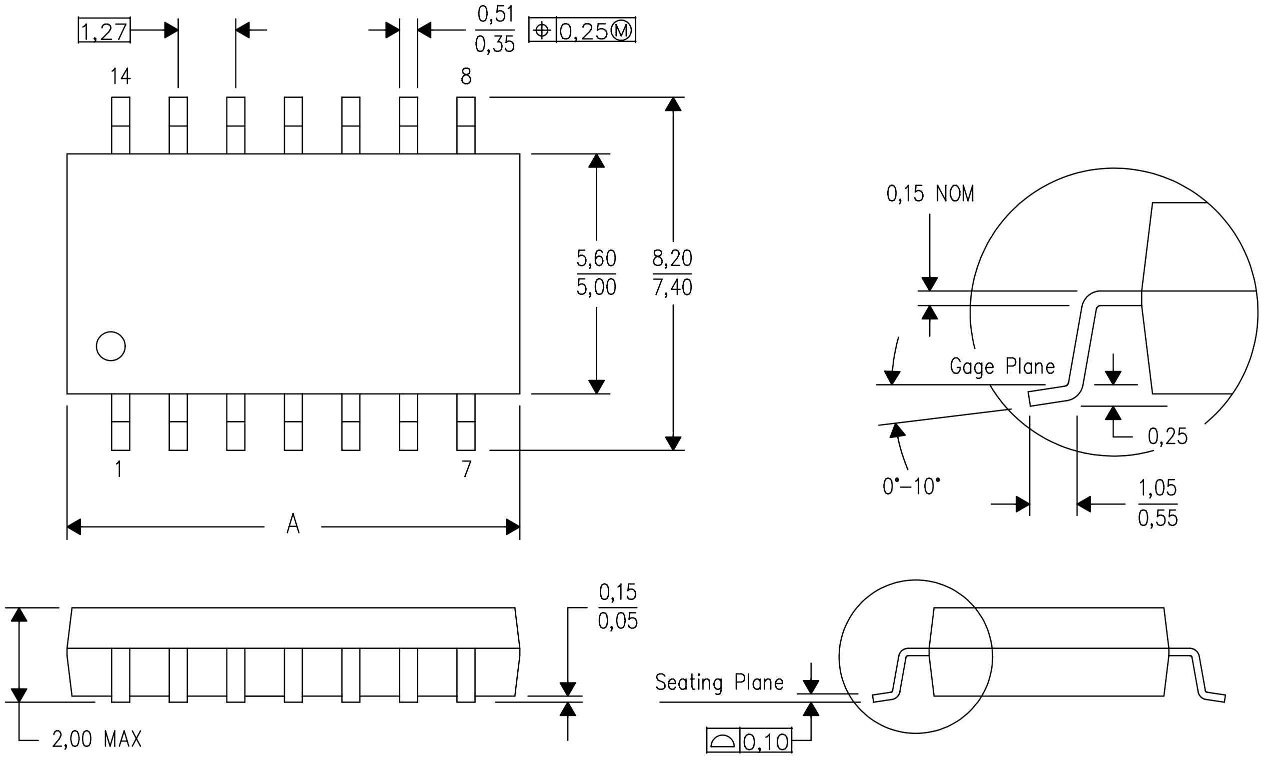


NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

**NS (R-PDSO-G****)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**

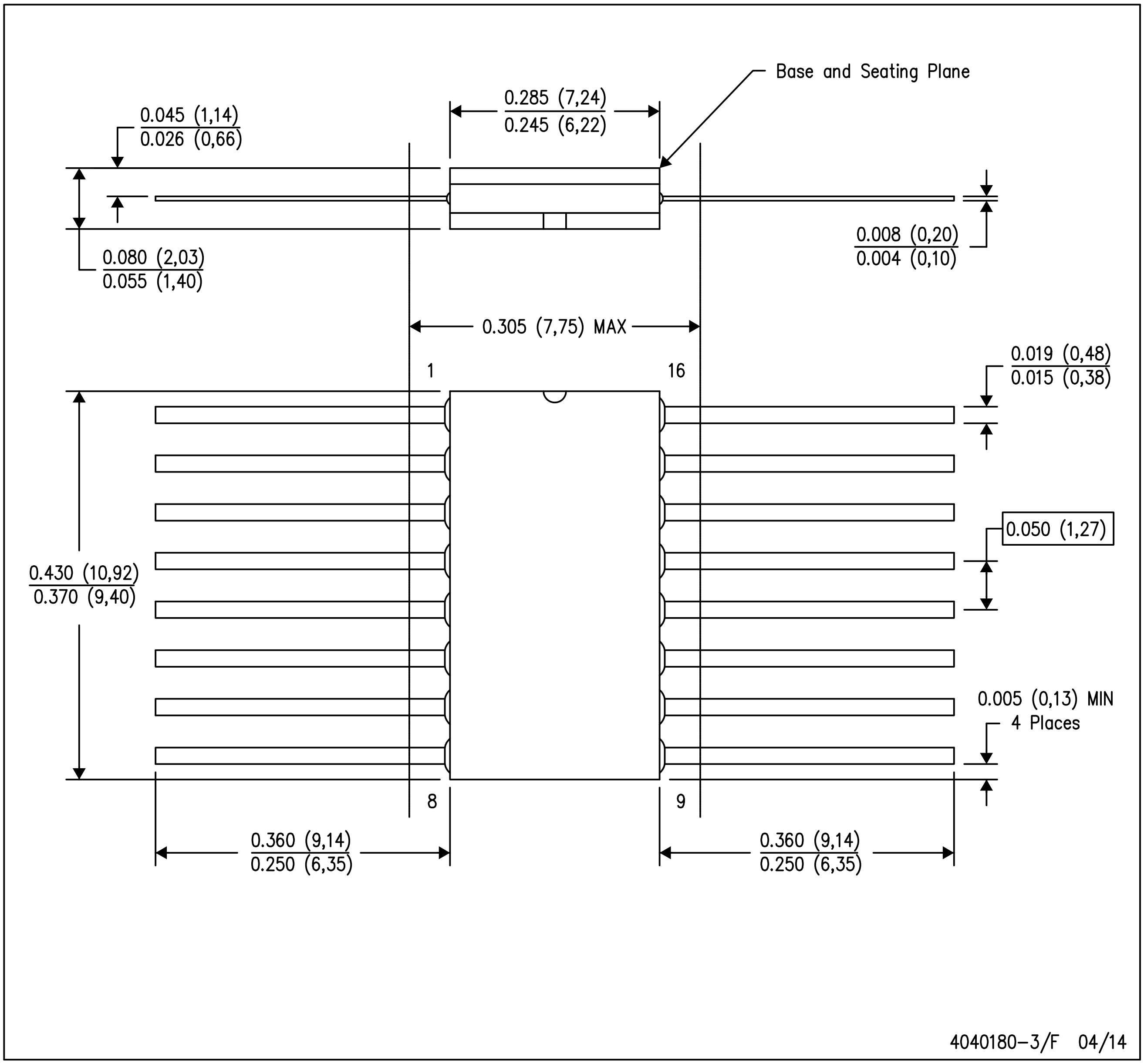


| PINS ** / DIM | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

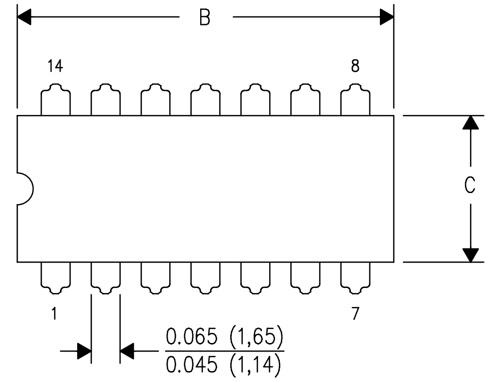
W (R–GDFP–F16) CERAMIC DUAL FLATPACK



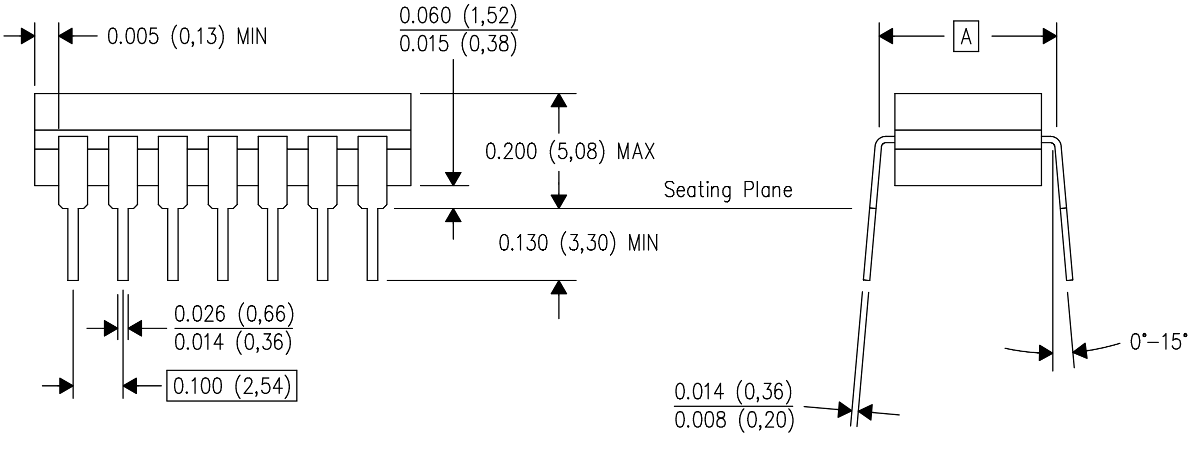
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP2–F16

# J (R-GDIP-T**) CERAMIC DUAL IN-LINE PACKAGE

14 LEADS SHOWN



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX | 0.785<br>(19,94) | .840<br>(21,34) | 0.960<br>(24,38) | 1.060<br>(26,92) |
| B MIN | —— | —— | —— | —— |
| C MAX | 0.300<br>(7,62) | 0.300<br>(7,62) | 0.310<br>(7,87) | 0.300<br>(7,62) |
| C MIN | 0.245<br>(6,22) | 0.245<br>(6,22) | 0.220<br>(5,59) | 0.245<br>(6,22) |

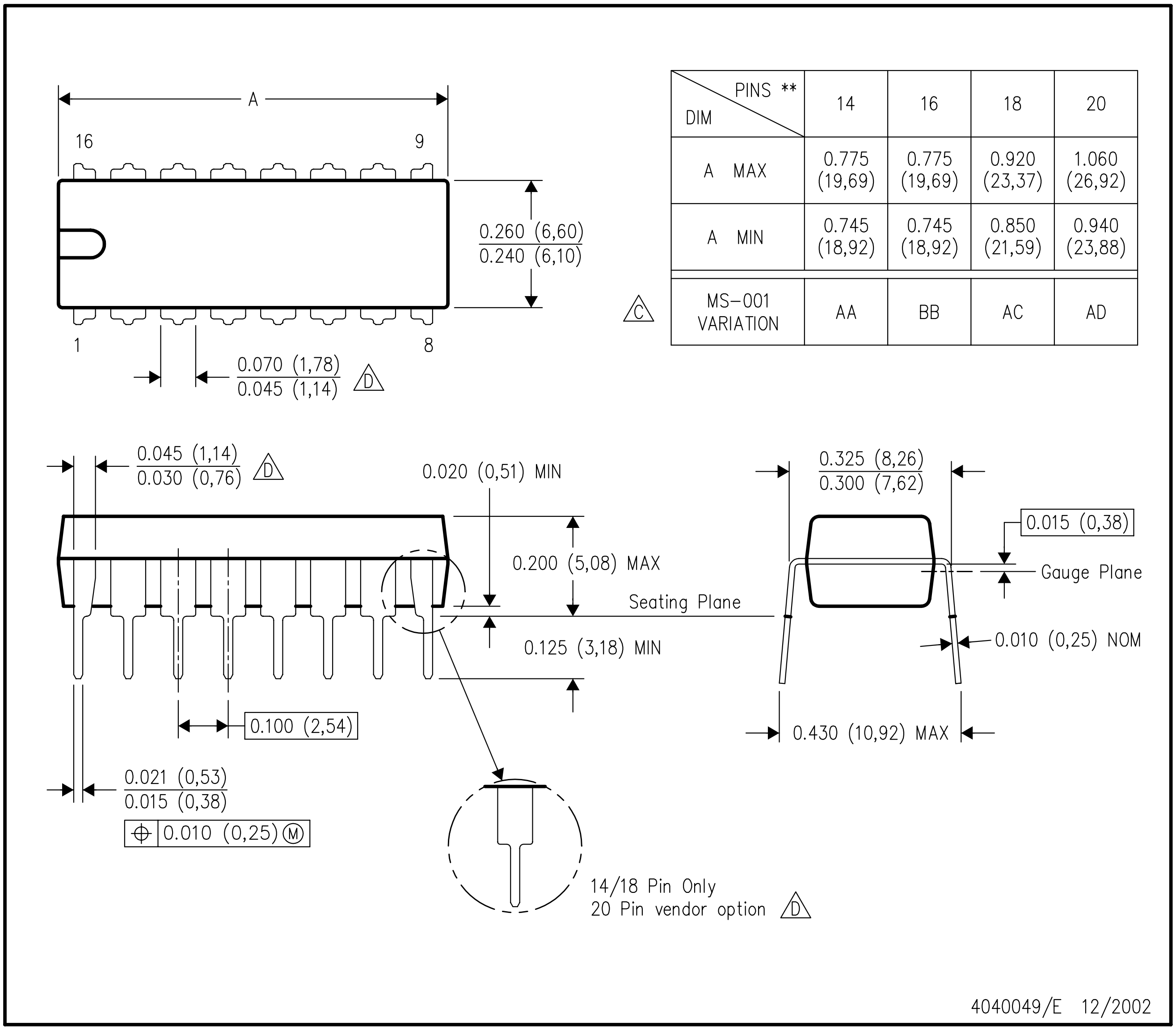


4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

## N (R–PDIP–T**)　　PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS–001 VARIATION | AA | BB | AC | AD |

4040049/E 12/2002

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated