

54H/74H71

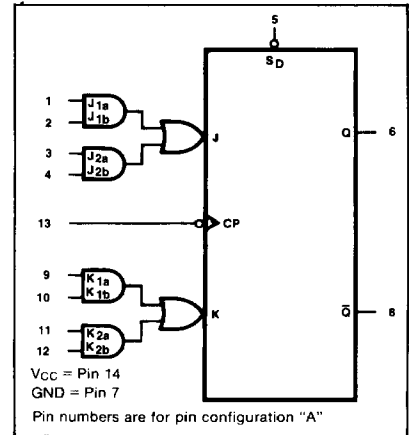
DESCRIPTION

The "71" is a positive pulse triggered master slave flip-flop with AND-OR gated JK inputs and direct Set (\bar{S}_D) input. JK information is loaded into the master while the Clock is HIGH and transferred to the slave on the HIGH-to-LOW Clock transition. The J and K inputs should be stable while the Clock is HIGH for conventional operation. J

or K input transitions from HIGH-to-LOW should be avoided while the Clock is HIGH due to "One's catching" feature of this flip-flop.

The Set (\bar{S}_D) is an asynchronous active LOW input. When LOW, the \bar{S}_D overrides the Clock and data inputs forcing the Q output HIGH and the \bar{Q} output LOW.

LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $-70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$
Plastic DIP	Fig A	N74H71N	
Ceramic DIP	Fig A	N74H71F	S54H71F
Flatpak	Fig B		S54H71W

PIN CONFIGURATIONS

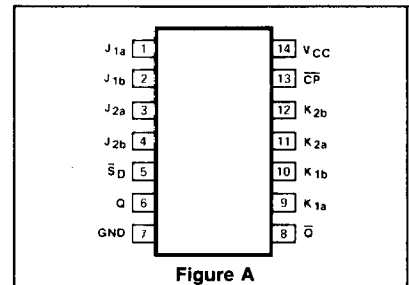


Figure A

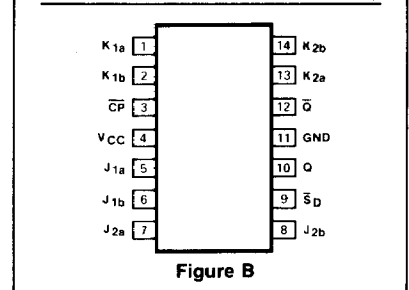


Figure B

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
\overline{CP}	Clock input $I_{IH} (\mu A)$ $I_{IL} (mA)$		100 -4.0		
\bar{S}_D	Set input $I_{IH} (\mu A)$ $I_{IL} (mA)$		150 -6.0		
JK	Data inputs $I_{IH} (\mu A)$ $I_{IL} (mA)$		50 -2.0		
Q & \bar{Q} Outputs	$I_{OH} (\mu A)$ $I_{OL} (mA)$		-500 20		

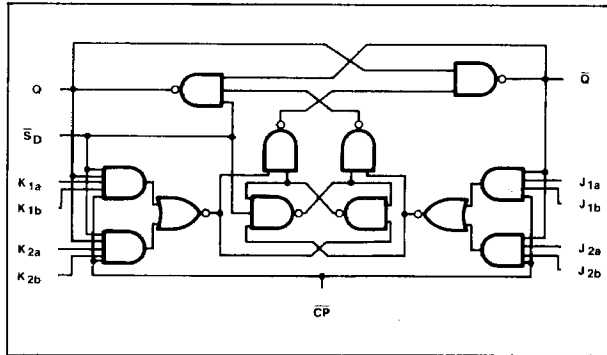
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CC}	Supply current				30					mA

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H and see inside back cover for 54S/74S and 54LS/74LS specification.

LOGIC DIAGRAM



MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	\bar{S}_D	$\bar{C}P$	J	K	Q	\bar{Q}
Asynchronous Set	L	X	X	X	H	L
Toggle	H	\square	h	h	\bar{q}	q
Load "1" (Set)	H	\square	h	l	H	L
Hold "no change"	H	\square	l	l	q	\bar{q}

H = HIGH voltage level steady state.
 L = LOW voltage level steady state.
 h = HIGH voltage level prior to LOW-to-HIGH Clock transition. ^(c)
 l = LOW voltage level prior to LOW-to-HIGH Clock transition. ^(c)
 X = Don't care.
 q = Lower case letters indicate the state of the referenced output prior to the HIGH to LOW Clock transition.
 \square = Positive Clock pulse.

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
				$C_L = 25\text{pF}$ $R_L = 280\Omega$						
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock frequency			25						MHz
t_{PLH} t_{PHL}	Propagation delay Clock to Output				21 27					ns ns
t_{PLH} t_{PHL}	Propagation delay Set to Output				13 24					ns ns

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_w(H)$	Clock pulse width (HIGH)			12						ns
$t_w(L)$	Clock pulse width (LOW)			28						ns
$t_w(L)$	Set pulse width (LOW)			16						ns
t_s	Setup time J or K to Clock			(c)						ns
t_h	Hold time J or K to Clock			0						ns

NOTE

c. The J and K inputs must be stable while the Clock is HIGH for conventional operation.