



54HC164/74HC164(文件编号: S&CIC0464)

8 bit 串入并出移位寄存器

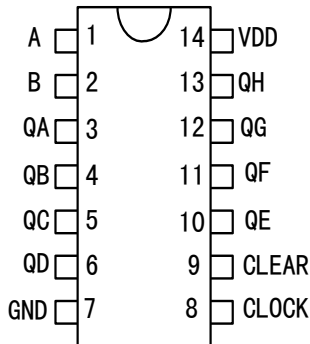
- AND-Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Direct Clear
- Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPS

DESCRIPTION

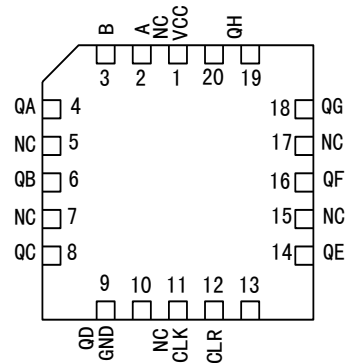
These 8-bit shift registers feature AND-gated serial inputs and an asynchronous clear (CLR) input. The gated serial (A and B) inputs permit complete control over incoming data; a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock (CLK) pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs can be changed while CLK is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of CLK.

The 54HC164 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74HC164 is characterized for operation from -40°C to 85°C.

54HC164...J OR W PACKAGE  
74HC164...D OR N PACKAGE



54HC164...FK PACKAGE (TOP VIEW)



NC-NO internal connection

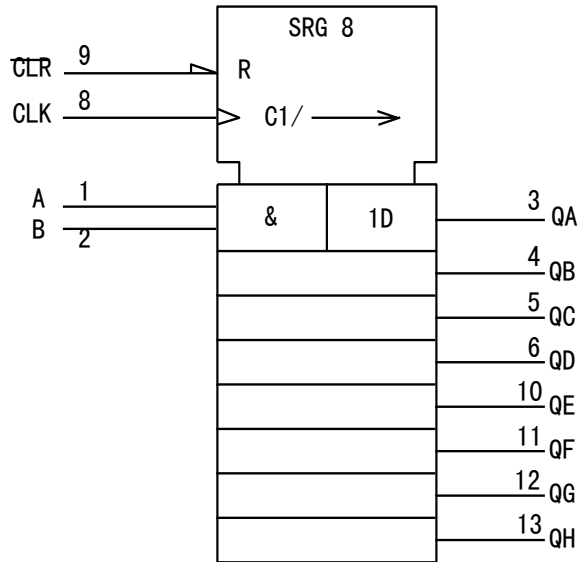
FUNCTION TABLE

INPUTS				OUTPUTS		
CLR	CLK	A	B	QA	QB...QH	
L	X	X	X	L	L	L
H	L	X	X	QA0	QB0	QH0
H	↑	H	H	H	QAn	QGn
H	↑	L	X	L	QAn	QGn
H	↑	X	L	L	QAn	QGn

QA0, QB0, QH0=the level of QA, QB, or QH, respectively, before the indicated steady-state input conditions were established  
QAn, QGn=the level of QA or QG before the most recent ↑ transition of CLK: indicates a 1-bit shift

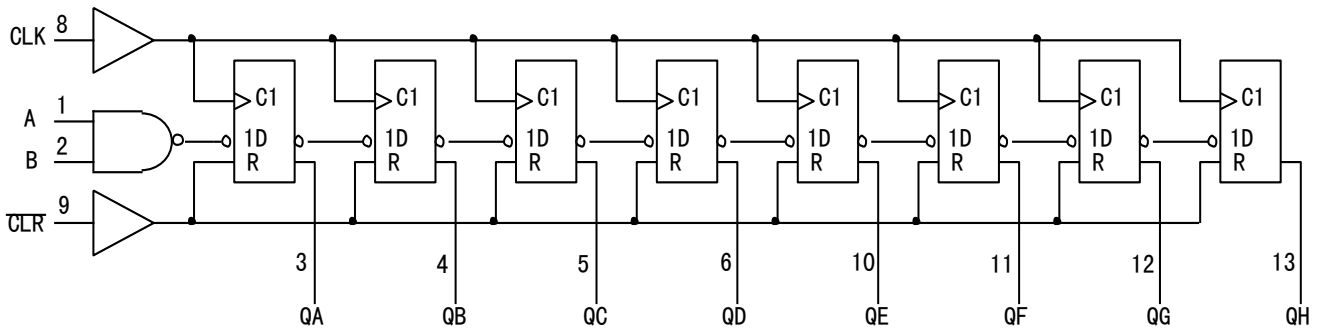


### LOGIC SYMBOL



- This symbol is in accordance with ANS/IEEE Std 91-1984 and IEC publication 617-12.
- Pin numbers shown are for the D, J, N, and W packages.

### LOGIC DIAGRAM (positive logic)



Pin numbers shown are for the D, J, N and W packages.





### RECOMMENDED OPERATING CONDITIONS

		54HC164			74HC164			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub> Supply voltage		2	5	6	2	5	6	
V <sub>IH</sub> High-level input voltage	V <sub>CC</sub> =2V	1.5	-	-	1.5	-	-	
	V <sub>CC</sub> =4.5V	3.15	-	-	3.15	-	-	
	V <sub>CC</sub> =6V	4.2	-	-	4.2	-	-	
V <sub>IL</sub> Low-level input voltage	V <sub>CC</sub> =2V	0	-	0.5	0	-	0.5	
	V <sub>CC</sub> =4.5V	0	-	1.35	0	-	1.35	
	V <sub>CC</sub> =6V	0	-	1.8	0	-	1.8	
V <sub>I</sub> Input voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
V <sub>O</sub> Output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
t <sub>T</sub> Input transition (rise and fall) time	V <sub>CC</sub> =2V	0	-	1000	0	-	1000	ns
	V <sub>CC</sub> =4.5V	0	-	500	0	-	500	
	V <sub>CC</sub> =6V	0	-	400	0	-	400	
T <sub>A</sub> Operating free-air temperature		-55	-	125	-40	-	85	°C

T If this device is used in the threshold region (from V<sub>IL</sub> max=0.5V to V<sub>IH</sub> min=1.5V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at tt=1000ns and V<sub>CC</sub>=2V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

### Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> =25°C			54HC164		74HC164		UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
V <sub>OH</sub>	V <sub>I</sub> =V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> =-20uA	2V	1.9	1.998	-	1.9	-	1.9	V	
			4.5V	4.4	4.499	-	4.4	-	4.4		
		6V	5.9	5.999	-	5.9	-	5.9			
		I <sub>OH</sub> =-4mA	4.5V	3.98	4.3	-	3.7	-	3.84		
		I <sub>OH</sub> =-5.2mA	6V	5.48	5.8	-	5.2	-	5.34		
V <sub>OL</sub>	V <sub>I</sub> =V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> =20uA	2V	-	0.002	0.1	-	0.1	-	0.1	V
			4.5V	-	0.001	0.1	-	0.1	-	0.1	
			6V	-	0.001	0.1	-	0.1	-	0.1	
		I <sub>OL</sub> =4mA	4.5V	-	0.17	0.26	-	0.4	-	0.33	
		I <sub>OL</sub> =5.2mA	6V	-	0.15	0.26	-	0.4	-	0.33	
I <sub>I</sub>	V <sub>I</sub> =V <sub>CC</sub> or 0	6V	-	±0.1	±100	-	±1000	-	±1000	nA	
I <sub>CC</sub>	V <sub>I</sub> =V <sub>CC</sub> or 0, I <sub>O</sub> =0	6V	-	-	8	-	160	-	80	uA	
C <sub>I</sub>		2V to 6V	-	3	10	-	10	-	10	pF	



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Timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		VCC	T <sub>A</sub> =25°C		54HC164		74HC164		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub> Clock frequency		2V	0	6	0	4.2	0	5	MHz
		4.5V	0	31	0	21	0	25	
		6V	0	36	0	25	0	28	
t <sub>w</sub> Pulse duration	CLR low	2V	100	-	150	-	125	-	ns
		4.5V	20	-	30	-	25	-	
		6V	17	-	25	-	21	-	
	CLK high or low	2V	80	-	120	-	100	-	
		4.5V	16	-	24	-	20	-	
		6V	14	-	20	-	18	-	
t <sub>su</sub> Setup time before CLK ↑	Data	2V	100	-	150	-	125	-	ns
		4.5V	20	-	30	-	25	-	
		6V	17	-	25	-	21	-	
	CLR inactive	2V	100	-	150	-	125	-	
		4.5V	20	-	30	-	25	-	
		6V	17	-	25	-	21	-	
t <sub>h</sub> Hold time, data after CLK ↑	2V	5	-	5	-	5	-	ns	
	4.5V	5	-	5	-	5	-		
	6V	5	-	5	-	5	-		

Switching characteristics over recommended operating free-air temperature rang, C<sub>L</sub>=50pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC	T <sub>A</sub> =25°C			54HC164		74HC164		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			2V	6	10	-	4.2	-	5	-	MHz
			4.5V	31	54	-	21	-	25	-	
			6V	36	62	-	25	-	28	-	
t <sub>PHL</sub>	CLR	Any Q	2V	-	140	205	-	295	-	255	ns
			4.5V	-	28	41	-	59	-	51	
			6V	-	24	35	-	51	-	46	
t <sub>pd</sub>	CLK	Any Q	2V	-	115	175	-	265	-	220	ns
			4.5V	-	23	35	-	53	-	44	
			6V	-	20	30	-	45	-	38	
t <sub>t</sub>			2V	-	38	75	-	110	-	95	ns
			4.5V	-	8	15	-	22	-	19	
			6V	-	6	13	-	19	-	16	



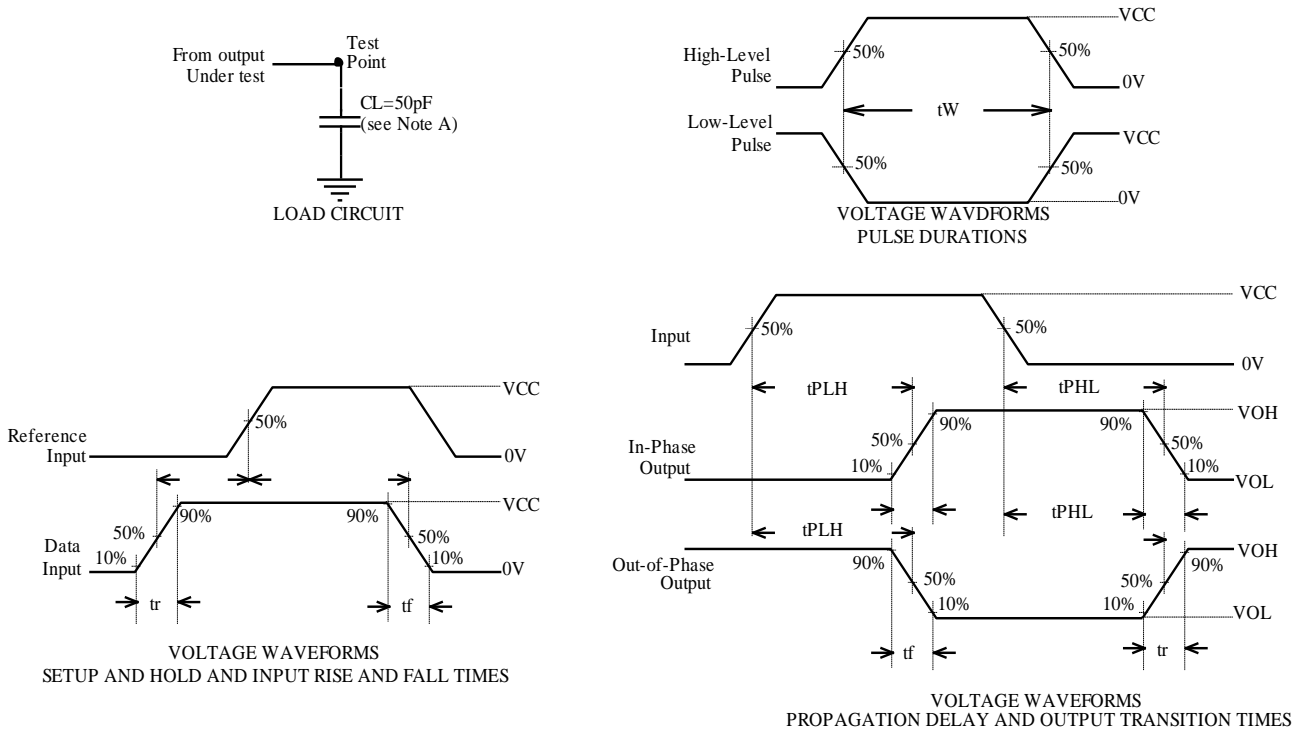
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Operating characteristics,  $T_A=25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
Cpd Power dissipation capacitance	No load	135	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and test-fixture capacitance.  
 B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{MHz}$ ,  $Z_0=50\ \Omega$ ,  $t_r=6\text{ns}$ ,  $t_f=6\text{ns}$ .  
 C. For clock inputs,  $f_{\text{max}}$  is measured when the input duty cycle is 50%  
 D. The outputs are measured one at a time with one input transition per measurement.  
 E.  $t_{\text{PLH}}$  and  $t_{\text{PHL}}$  are the same as  $t_{\text{pd}}$ .

Figure 1. Load Circuit and Voltage Waveforms



PAD ASSIGNMENT

Pad No	Pad Name	X	Y
1	A	-242.00	-53.50
2	B	-250.00	252.00
3	QA	-135.00	-188.50
4	QB	0.00	-188.50
5	QC	115.00	-188.50
6	QD	252.00	-188.50
7	GND	252.00	-73.50
8	CLOCK	241.85	41.50
9	CLEAR	252.00	180.50
10	QE	137.00	190.50
11	QF	2.00	190.50
12	QG	-113.00	190.50
13	QH	-250.00	190.50
14	VDD	-250.00	61.50

附图:

