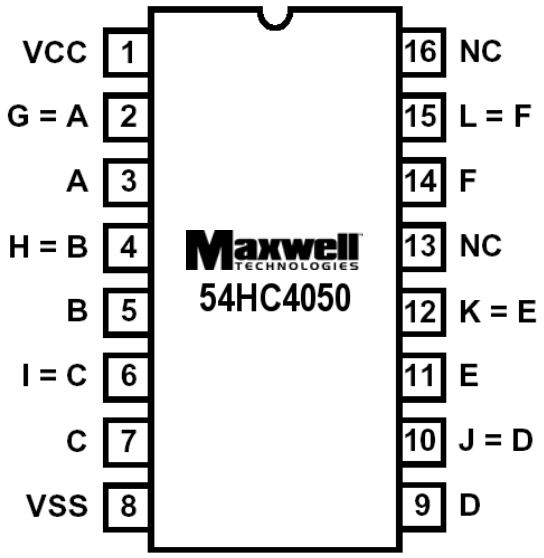
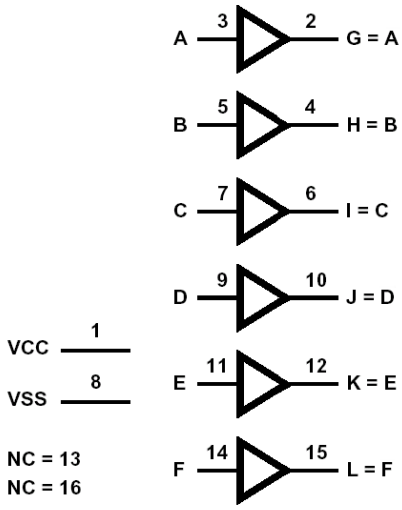
54HC4050
CMOS Logic Hex Non-Inverting Buffers





Logic Diagram

FEATURES:

- High speed CMOS logic hex non-inverting buffers
- RAD-PAK® radiation hardened against natural space radiation
- Single Event Effects:
  - SEL: > 120 MeV/mg/cm2
- Total dose hardness:
- - > 100 Krad (Si), depending upon space mission
- Package:
  -16 Pin RAD-PAK® Flat Pack
- Typical propagation delay:
  - 6ns at V_{CC} = 5V, C_L = 15pF, T_A = 25°C
- High-to-Low voltage level converter for up to V_I = 16V
- Fanout (over temperature range)
  -10 LSTTL loads (Standard Outputs)
  -15 LSTTL loads (Bus Driver Outputs)
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL logic ICs
- 2V to 6V operation
- High noise immunity
- $-N_{IL}$ = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V

DESCRIPTION:

Maxwell Technologies' 54HC4050 high speed CMOS Logic Hex Non-Inverting Buffers features a greater than 100 krad(Si) total dose tolerance, depending upon space mission. These parts have a modified input protection structure that enables them to be used as logic level translators which will convert high-level logic to a low-level logic while operating off the low-level logic supply. For example, 15V input pulse levels can be down-converted to 0V to 5V logic levels. The modified input protection structure protects the input from negative electrostatic discharge. The 54HC4050 can be used as simple buffers or inverters without level translation.

Maxwell Technologies' patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK provides greater than 100 krad (Si) radiation dose tolerance. This product is available with screening up to Class S.

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TABLE 1. 54HC4050 PINOUT DESCRIPTIONS

PIN	SYMBOL	DESCRIPTION
1	V_{CC}	Power supply
8	V_{SS}	Ground
13, 16	NC	Not Connected
3, 5, 7, 9, 11, 14	A - F	Inputs
2	G = A	Buffered Output
4	H = B	Buffered Output
6	I = C	Buffered Output
10	J = D	Buffered Output
12	K = E	Buffered Output
15	L = F	Buffered Output

TABLE 2. 54HC4050 ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Storage Temperature	T_S	-65	150	°C
Operating Temperature Range	T_A	-55	125	°C
DC Supply Voltage	V_{CC}	-0.5	7.0	V
DC Input Diode Current For V_I < -0.5V or V_I > V_{CC} +0.5V	I_{IK}	-20	+20	mA
DC Output Diode Current For V_O < -0.5V or V_O > V_{CC} +0.5V	I_{OK}	-20	+20	mA
DC Output Source or Sink Current per Output Pin For V_O > -0.5V or V_O < V_{CC} +0.5V	I_O	-25	+25	mA
DC V_{CC} or Ground Current	I_{CC} or I_{GND}	-50	+50	mA

TABLE 3. DELTA LIMITS

PARAMETER	VARIATION
I_{CC}	±10% of specified value in Table 5

TABLE 4. 54HC4050 RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	V_{CC}	2	6	V
DC Input or output Voltage	V_I, V_O	0	V_{CC}	V
Input Rise and Fall Time 2V 4.5V 6V		--	 1000 500 400	ns
Temperature Range	T_A	-55	125	°C

TABLE 5. 54HC4050 DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = -55 TO 125°C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNIT
High Level Output Voltage CMOS Loads	V_{OH}	$V_I = V_{IH}$ or V_{IL}, I_O = -0.02mA V_{CC} = 2V V_{CC} = 4.5V V_{CC} = 6V		 1.9 4.4 5.9	 -- -- --	V
High Level Output Voltage TTL Loads		$V_I = V_{IH}$ or V_{IL}, I_O = -4mA V_{CC} = 4.5V	+25°C	3.98	--	
			-55 to 125°C	3.7		
		$V_I = V_{IH}$ or V_{IL}, I_O = -5.2mA V_{CC} = 6V	+25°C	5.48	--	
			-55 to 125°C	5.2	--	
Low Level Output Voltage CMOS Loads	V_{OL}	$V_I = V_{IH}$ or V_{IL}, I_O = -0.02mA V_{CC} = 2V V_{CC} = 4.5V V_{CC} = 6V		 	 0.1 0.1 0.1	V
Low Level Output Voltage TTL Loads		$V_I = V_{IH}$ or V_{IL}, I_O = 4mA V_{CC} = 4.5V	+25°C	0.26	--	
			-55 to 125°C	0.4	--	
		$V_I = V_{IH}$ or V_{IL}, I_O = 5.2mA V_{CC} = 6V	+25°C	0.36	--	
			-55 to 125°C	0.4	--	
High Level Input Voltage	V_{IH}	V_{CC} = 2V V_{CC} = 4.5V V_{CC} = 6V		1.5 3.15 4.2	-- -- --	V
Low Level Input Voltage	V_{IL}	V_{CC} = 2V V_{CC} = 4.5V V_{CC} = 6V		-- -- --	0.5 1.35 1.8	V
Input Leakage Current	I_I	V_{CC} = 6V, $V_I = V_{CC}$ or GND	+25°C	--	±0.1	µA
			-55 to 125°C	--	±1	
		V_{CC} = 6V, V_I = 15V	+25°C	--	±0.5	
			-55 to 125°C	--	±5	

TABLE 5. 54HC4050 DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = -55 TO 125°C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNIT
Quiescent Device Current	I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0mA V_{CC} = 6V	+25°C	--	2	µA
			-55 to 125°C	--	40	

TABLE 6. 54HC4050 AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = -55 TO 125°C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITION		MIN	MAX	UNIT
Propogation Delay nA to nY	t_{PLH}, t_{PHL}	C_L = 50pF V_{CC} = 2V	+25°C	--	85	ns
			-55 to 125°C	--	130	
		V_{CC} = 4.5V	+25°C	--	17	
			-55 to 125°C	--	26	
		V_{CC} = 6V	+25°C	--	14	
			-55 to 125°C	--	22	
Transition Times (Figure 1)	t_{TLH}, t_{THL}	C_L = 50pF V_{CC} = 2V	+25°C	--	75	ns
			-55 to 125°C	--	110	
		V_{CC} = 4.5V	+25°C	--	15	
			-55 to 125°C	--	22	
		V_{CC} = 6V	+25°C	--	13	
			-55 to 125°C	--	19	

TABLE 7. 54HC4050 CAPACITANCE[1]

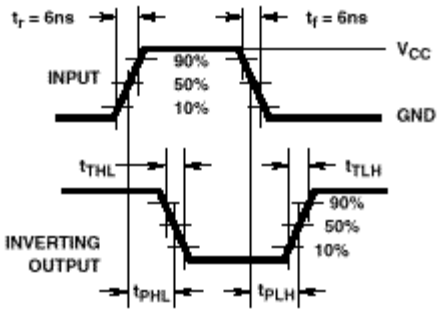
PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNIT
Input Capacitance	C_I		10	pF
Power Dissipation Capacitance[2, 3]	C_{PD}	V_{CC} = 5V	35	pF

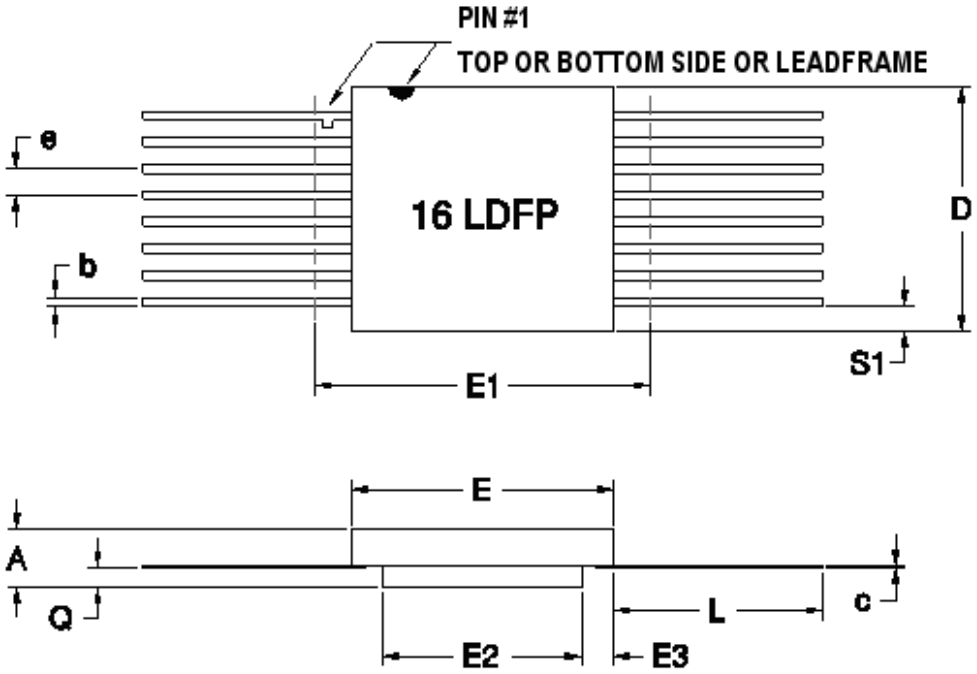
1. Guaranteed by design.

2. C_{PD} is used to determine the dynamic power consumption, per gate.

3. $P_D = V_{CC}^2$ fi ($C_{PD} + C_L$) where fi = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

FIGURE 1. TRANSITION TIMES AND PROPOGATION DELAY TIMES, COMBINATION LOGIC





16-PIN RAD-PAK® FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.115	0.135	0.150
b	0.015	0.017	0.019
c	0.004	0.005	0.007
D	0.407	0.415	0.423
E	0.275	0.280	0.285
E1	--	--	0.500
E2	0.150	0.156	0.162
E3	0.030	0.062	--
e	0.050 BSC		
L	0.325	0.335	0.345
Q	0.020	0.033	0.045
S1	0.005	0.024	0.045
N	16		

F16-01
Note: All dimensions in inches

Important Notice:

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