High Speed CMOS TTL Input – 54HCT86

Quadruple 2-Input Exclusive OR Gate IC in bare die form

Rev 1.0
09/01/19

Description

The 54HCT86 Hex Inverter is fabricated using a 2.5µm 5V CMOS process with the same high speed performance of LSTTL combined with CMOS low power consumption. The device contains four independent gates and performs the Boolean function Y = A ⊕ B = AB + AB in positive logic. The device is characterized over the full Military Temperature Range. All inputs are protected against ESD and excess voltage transients. Device inputs directly accept LSTTL or CMOS.

Features:

- Output Drive Capability: 10 LSTTL Loads
- Low Input Current: 1µA
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 4.5V to 5.5V
- TTL / CMOS compatible Input Levels
- Function compatible with 54LS86
- Full Military Temperature Range.

Ordering Information

The following part suffixes apply:

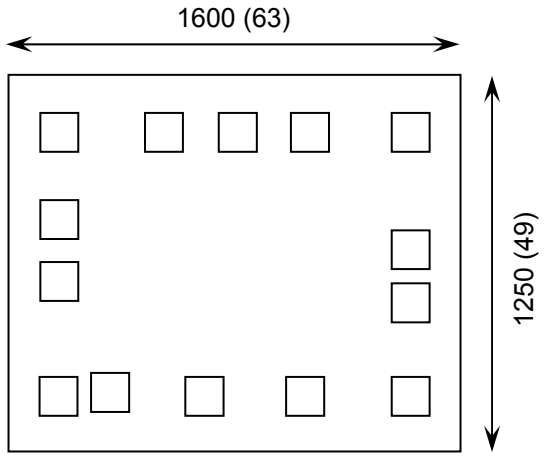
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1600 x 1250 63 x 49	µm mils
Minimum Bond Pad Size	120 x 120 4.72 x 4.72	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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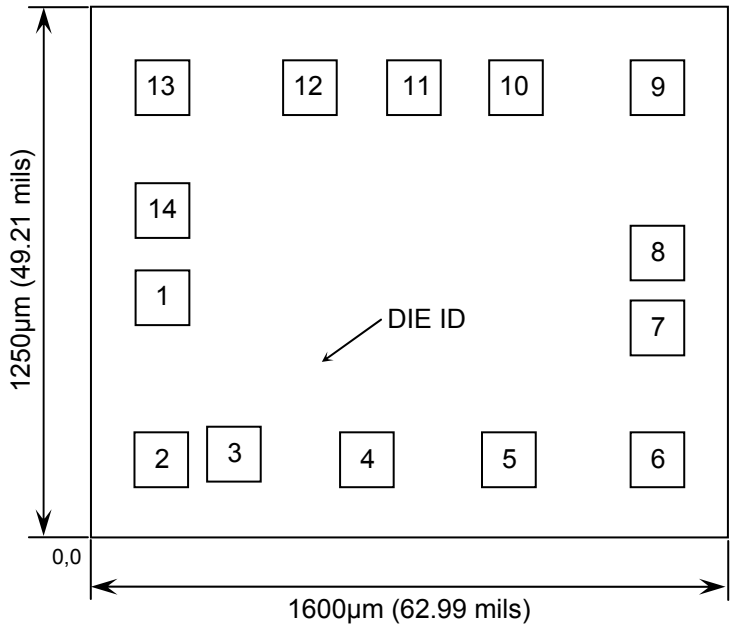
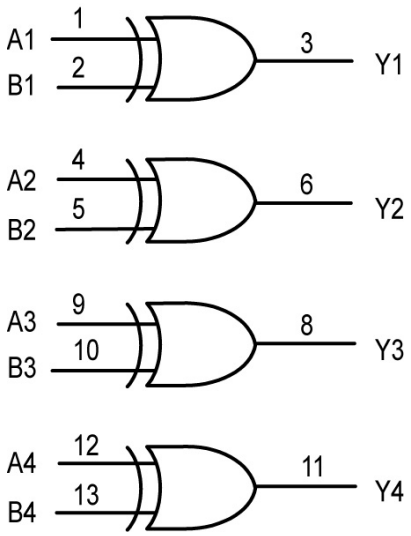
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	A1	0.125	0.500
2	B1	0.125	0.125
3	Y1	0.305	0.130
4	A2	0.635	0.125
5	B2	0.995	0.125
6	Y2	1.355	0.125
7	GND	1.355	0.435
8	Y3	1.355	0.610
9	A3	1.355	1.000
10	B3	0.995	1.000
11	Y4	0.745	1.000
12	A4	0.485	1.000
13	B4	0.125	1.000
14	V_{CC}	0.125	0.710
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

Logic Diagram



$Y = A \oplus B$
$= \overline{A}B + A\overline{B}$

Function Table

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High level (steady state)
L = Low level (steady state)

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Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-0.5 to V_{CC} +0.5	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Input Current	I_{IN}	±20	mA
DC Output Current, per pad	I_{OUT}	±25	mA
DC Supply Current, V_{CC} or GND, per pad	I_{CC}	±50	mA
Power Dissipation in Still Air	P_D	750	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.

Recommended Operating Conditions[2] (Voltages referenced to GND)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{CC}	4.5	5.5	V
DC Input or Output Voltage	V_{IN} ,V_{OUT}	0	V_{CC}	V
Operating Temperature Range	T_A	-55	+125	°C
Input Rise or Fall Times	t_r, t_f	-	500	ns

2. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				-55°C to 25°C	≤ 85°C	≤ 125°C	
Minimum High-Level Input Voltage	V_{IH}	4.5V	V_{OUT} = 0.1V or V_{CC}-1 $\lvert I_{OUT} \rvert$ ≤ 20µA	2.0	2.0	2.0	V
		5.5V		2.0	2.0	2.0	
Maximum Low-Level Input Voltage	V_{IL}	4.5V	V_{OUT} = 0.1V or V_{CC}-1 $\lvert I_{OUT} \rvert$ ≤ 20µA	0.8	0.8	0.8	V
		5.5V		0.8	0.8	0.8	
Minimum High-Level Output Voltage	V_{OH}	4.5V	V_{IN} = V_{IL} or V_{IH} $\lvert I_{OUT} \rvert$ ≤ 20µA	4.4	4.4	4.4	V
		5.5V		5.4	5.4	5.4	
		4.5V	V_{IN} = V_{IL} or V_{IH} $\lvert I_{OUT} \rvert$ ≤ 4.0mA	3.98	3.84	3.70	
Maximum Low-Level Output Voltage	V_{OL}	4.5V	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT} \rvert$ ≤ 20µA	0.1	0.1	0.1	V
		5.5V		0.1	0.1	0.1	
		4.5V	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT} \rvert$ ≤ 4.0mA	0.26	0.33	0.40	

DC Electrical Characteristics Continued (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				-55°C to 25°C	≤ 85°C	≤ 125°C	
Maximum Input Leakage Current	I_{IN}	5.5V	V_{IN} = V_{CC} or GND	±0.1	±1.0	±1.0	µA
Maximum Quiescent Supply Leakage Current[3]	I_{CC}	5.5V	V_{IN} = V_{CC} or GND I_{OUT} = 0µA	2	20	40	µA
Additional Quiescent Supply Current[3]	ΔI_{CC}	5.5V	V_{IN} = 2.4V, Any One Input. V_{IN} = V_{CC} or GND, Other Inputs I_{OUT} = 0µA	≥ -55°C	25°C to 125°C		mA
				2.9	2.4		

3. Total Supply Current = I_{CC} + $\Sigma\Delta I_{CC}$.

AC Electrical Characteristics[4]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				-55°C to 25°C	≤ 85°C	≤ 125°C	
Maximum Propagation Delay, Input A to Input Y (Figure 1,2)	t_{PLH}	5V ±10%	C_L = 50pF, t_r = t_f = 6ns	24	30	36	ns
Maximum Propagation Delay, Input A to Input Y (Figure 1,2)	t_{PHL}	5V ±10%	C_L = 50pF, t_r = t_f = 6ns	24	30	36	
Maximum Output Rise and Fall Time (Figure 1,2)	t_{TLH}, t_{THL}	5V ±10%	C_L = 50pF, t_r = t_f = 6ns	15	19	22	ns
Maximum Input Capacitance	C_{IN}	-	-	10	10	10	pF
Power Dissipation Capacitance Per Gate[5]	C_{PD}	-	T_A = 25°C, V_{CC} =5.0V	TYPICAL			pF
				36			

4. Not production tested in die form, characterized by chip design and tested in package LAT.
5. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

Switching Waveform

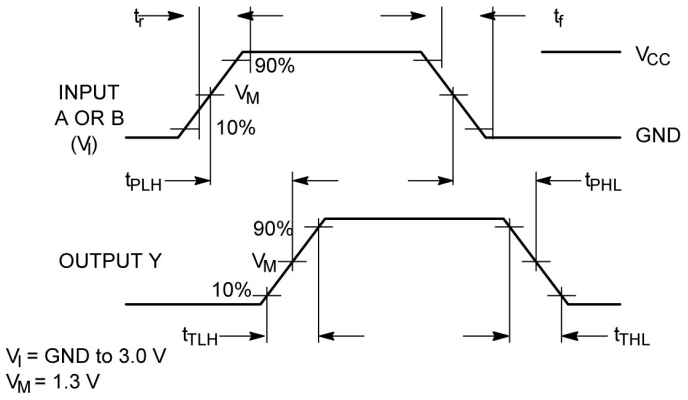
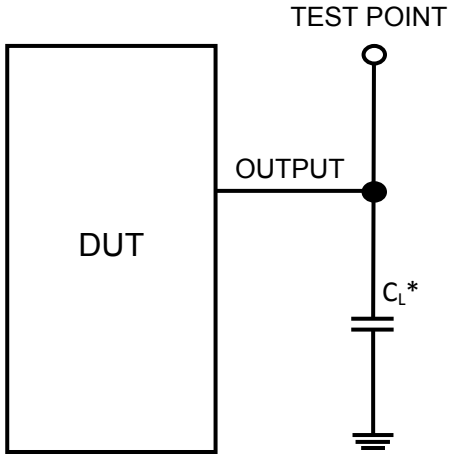


Figure 1 – Propagation Delay & Output Transition Time

Test Circuit



* Includes all probe and jig capacitance

Figure 2