

DM54LS190/DM74LS190, DM54LS191/DM74LS191 Synchronous 4-Bit Up/Down Counters with Mode Control

General Description

These circuits are synchronous, reversible, up/down counters. The LS191 is a 4-bit binary counter and the LS190 is a BCD counter. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high level transition of the clock input, if the enable input is low. A high at the enable input inhibits counting. Level changes at either the enable input or the down/up input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

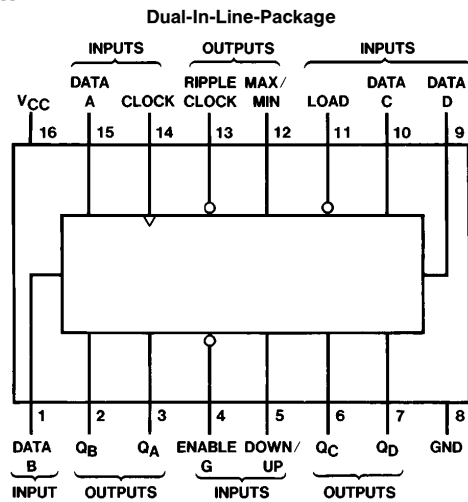
The clock, down/up, and load inputs are buffered to lower the drive requirement; which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Features

- Counts 8-4-2-1 BCD or binary
- Single down/up count control line
- Count enable control input
- Ripple clock output for cascading
- Asynchronously presettable with load control
- Parallel outputs
- Cascadable for n-bit applications
- Average propagation delay 20 ns
- Typical clock frequency 25 MHz
- Typical power dissipation 100 mW

Connection Diagram



TL/F/6405-1

Order Number DM54LS190J, DM54LS191J, DM54LS190W,
DM54LS191W, DM74LS190M, DM74LS191M, DM74LS190N, or DM74LS191N
See NS Package Number
J16A, M16A, N16A or W16A

DM54LS190/DM74LS190, DM54LS191/DM74LS191
Synchronous 4-Bit Up/Down Counters with Mode Control

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--------------------------------------|-----------------|
| Supply Voltage | 7V |
| Input Voltage | 7V |
| Operating Free Air Temperature Range | |
| DM54LS | −55°C to +125°C |
| DM74LS | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

| Symbol | Parameter | DM54LS190, LS191 | | | DM74LS190, LS191 | | | Units |
|------------------|--------------------------------|------------------|-----|------|------------------|-----|------|-------|
| | | Min | Nom | Max | Min | Nom | Max | |
| V _{CC} | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V _{IH} | High Level Input Voltage | 2 | | | 2 | | | V |
| V _{IL} | Low Level Input Voltage | | | 0.7 | | | 0.8 | V |
| I _{OH} | High Level Output Current | | | −0.4 | | | −0.4 | mA |
| I _{OL} | Low Level Output Current | | | 4 | | | 8 | mA |
| f _{CLK} | Clock Frequency (Note 4) | 0 | | 20 | 0 | | 20 | MHz |
| t _w | Pulse Width (Note 4) | Clock | 25 | | 25 | | | ns |
| | | Load | 35 | | 35 | | | |
| t _{SU} | Data Setup Time (Note 4) | 20 | | | 20 | | | ns |
| t _H | Data Hold Time (Note 4) | 0 | | | 0 | | | ns |
| t _{EN} | Enable Time to Clock (Note 4) | 30 | | | 30 | | | ns |
| T _A | Free Air Operating Temperature | −55 | | 125 | 0 | | 70 | °C |

'LS190 and 'LS191 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ (Note 1) | Max | Units | |
|-----------------|-----------------------------------|----------------------------------------------------------------------------------------------|--------|--------------|-------|-------|---|
| V _I | Input Clamp Voltage | V _{CC} = Min, I _I = −18 mA | | | −1.5 | V | |
| V _{OH} | High Level Output Voltage | V _{CC} = Min, I _{OH} = Max V _{IL} = Max, V _{IH} = Min | DM54 | 2.5 | 3.4 | V | |
| | | | DM74 | 2.7 | 3.4 | | |
| V _{OL} | Low Level Output Voltage | V _{CC} = Min, I _{OL} = Max V _{IL} = Max, V _{IH} = Min | DM54 | | 0.25 | 0.4 | V |
| | | | DM74 | | 0.35 | 0.5 | |
| | | I _{OL} = 4 mA, V _{CC} = Min | DM74 | | 0.25 | 0.4 | |
| I _I | Input Current @ Max Input Voltage | V _{CC} = Max V _I = 7V | Enable | | 0.3 | mA | |
| | | | Others | | 0.1 | | |
| I _{IH} | High Level Input Current | V _{CC} = Max V _I = 2.7V | Enable | | 60 | μA | |
| | | | Others | | 20 | | |
| I _{IL} | Low Level Input Current | V _{CC} = Max V _I = 0.4V | Enable | | −1.08 | mA | |
| | | | Others | | −0.4 | | |
| I _{OS} | Short Circuit Output Current | V _{CC} = Max (Note 2) | DM54 | −20 | −100 | mA | |
| | | | DM74 | −20 | −100 | | |
| I _{CC} | Supply Current | V _{CC} = Max (Note 3) | | 20 | 35 | mA | |

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Note 4: T_A = 25°C and V_{CC} = 5V.

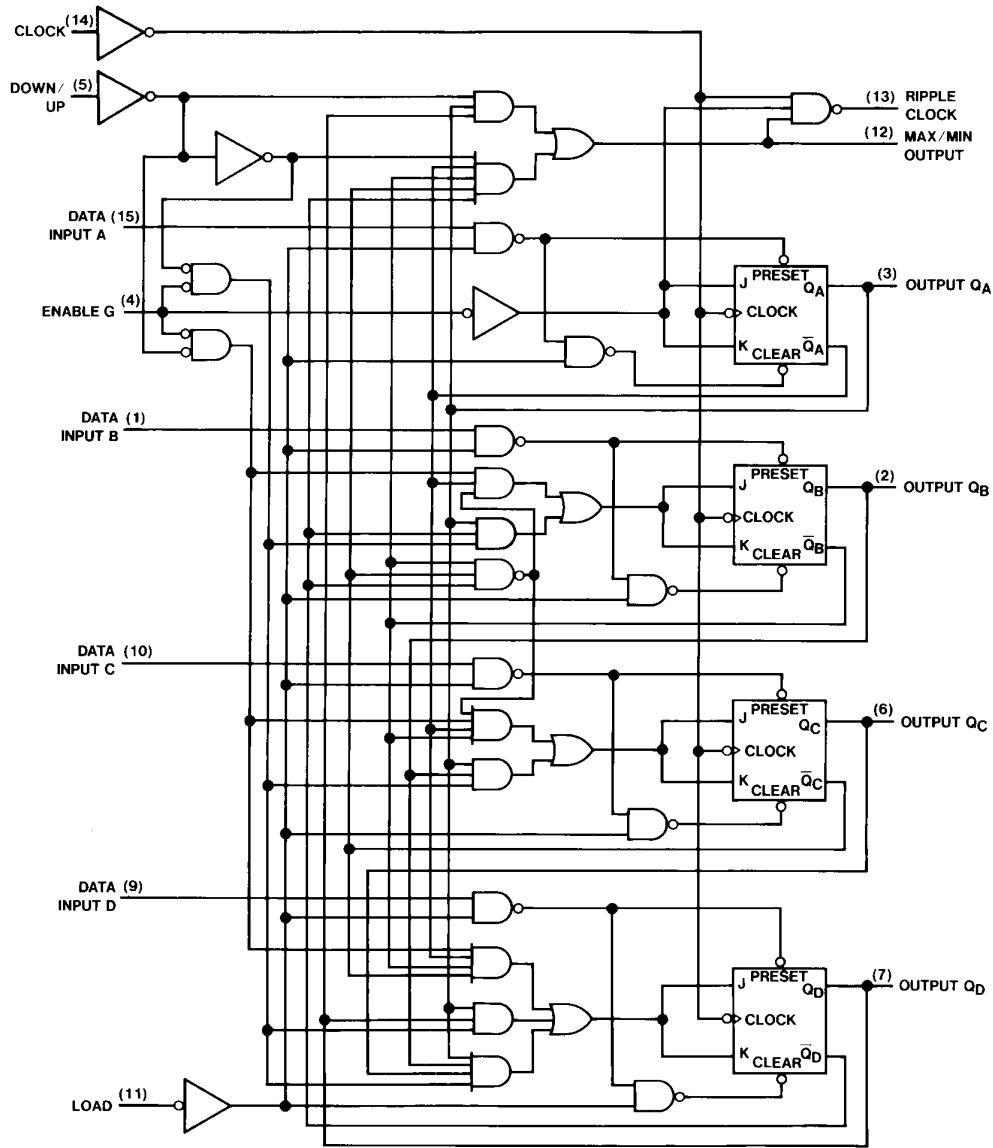
'LS190 and 'LS191 Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25^\circ C$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | From (Input) To (Output) | $R_L = 2\text{ k}\Omega$ | | | | Units |
|-----------|----------------------------------------------------|-----------------------------|--------------------------|-----|----------------------|-----|-------|
| | | | $C_L = 15\text{ pF}$ | | $C_L = 50\text{ pF}$ | | |
| | | | Min | Max | Min | Max | |
| f_{MAX} | Maximum Clock Frequency | | 20 | | 20 | | MHz |
| t_{PLH} | Propagation Delay Time Low to High Level Output | Load to Any Q | | 33 | | 43 | ns |
| t_{PHL} | Propagation Delay Time High to Low Level Output | Load to Any Q | | 50 | | 59 | ns |
| t_{PLH} | Propagation Delay Time Low to High Level Output | Data to Any Q | | 22 | | 26 | ns |
| t_{PHL} | Propagation Delay Time High to Low Level Output | Data to Any Q | | 50 | | 62 | ns |
| t_{PLH} | Propagation Delay Time Low to High Level Output | Clock to Ripple Clock | | 20 | | 24 | ns |
| t_{PHL} | Propagation Delay Time High to Low Level Output | Clock to Ripple Clock | | 24 | | 33 | ns |
| t_{PLH} | Propagation Delay Time Low to High Level Output | Clock to Any Q | | 24 | | 29 | ns |
| t_{PHL} | Propagation Delay Time High to Low Level Output | Clock to Any Q | | 36 | | 45 | ns |
| t_{PLH} | Propagation Delay Time Low to High Level Output | Clock to Max/Min | | 42 | | 47 | ns |
| t_{PHL} | Propagation Delay Time High to Low Level Output | Clock to Max/Min | | 52 | | 65 | ns |
| t_{PLH} | Propagation Delay Time Low to High Level Output | Up/Down to Ripple Clock | | 45 | | 50 | ns |
| t_{PHL} | Propagation Delay Time High to Low Level Output | Up/Down to Ripple Clock | | 45 | | 54 | ns |
| t_{PLH} | Propagation Delay Time Low to High Level Output | Down/Up to Max/Min | | 33 | | 36 | ns |
| t_{PHL} | Propagation Delay Time High to Low Level Output | Down/Up to Max/Min | | 33 | | 42 | ns |
| t_{PLH} | Propagation Delay Time Low to High Level Output | Enable to Ripple Clock | | 33 | | 36 | ns |
| t_{PHL} | Propagation Delay Time High to Low Level Output | Enable to Ripple Clock | | 33 | | 42 | ns |

Logic Diagrams

LS190 Decade Counters

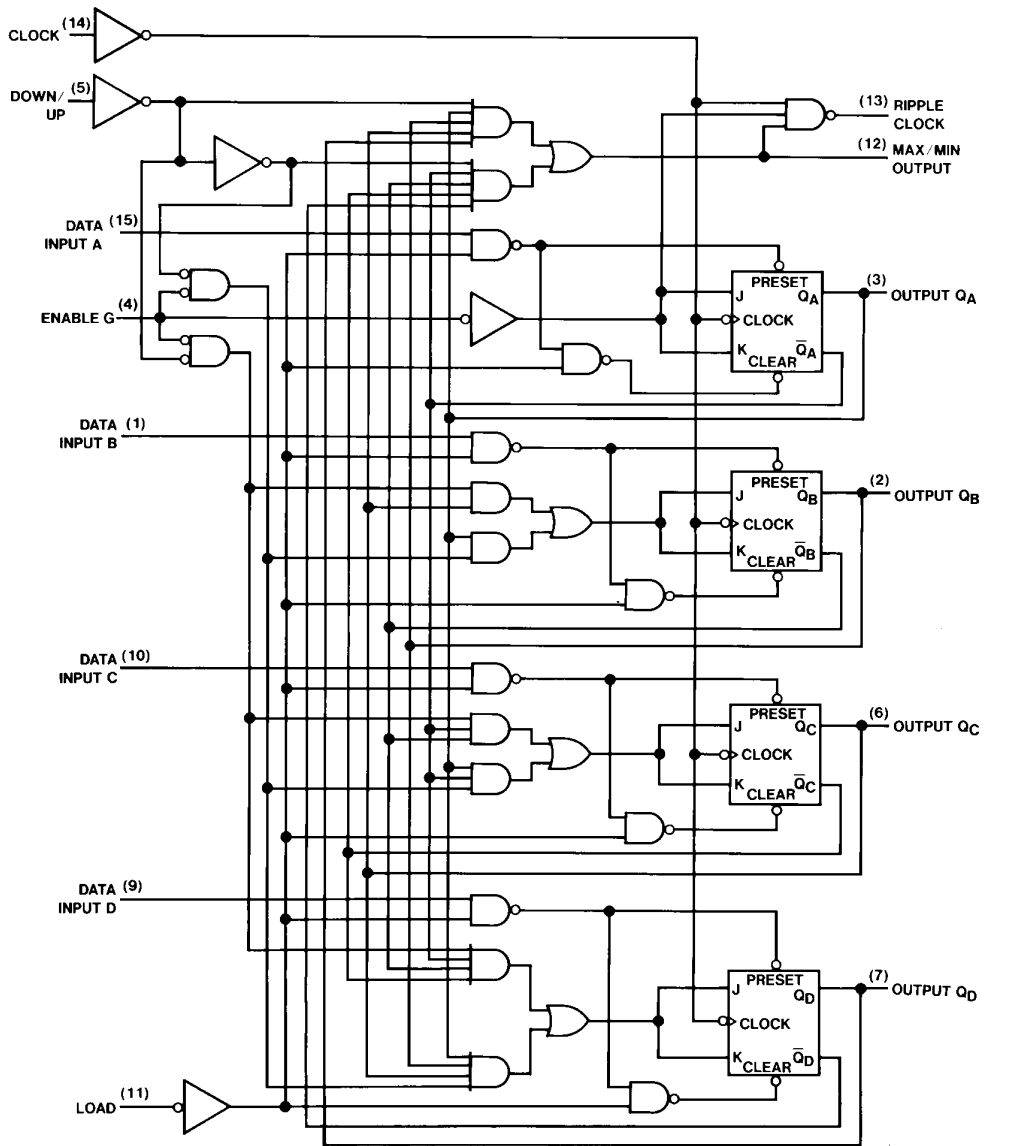


Pin (16) = V_{CC} , Pin (8) = GND

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Logic Diagrams (Continued)

LS191 Binary Counters

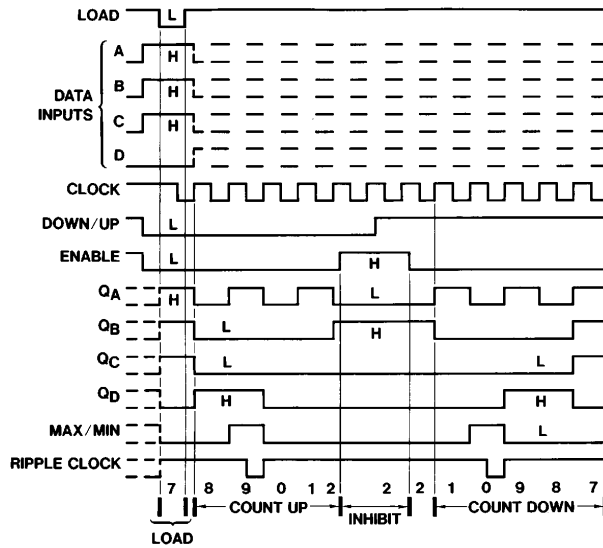


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Pin (16) = V_{CC}, Pin (8) = GND

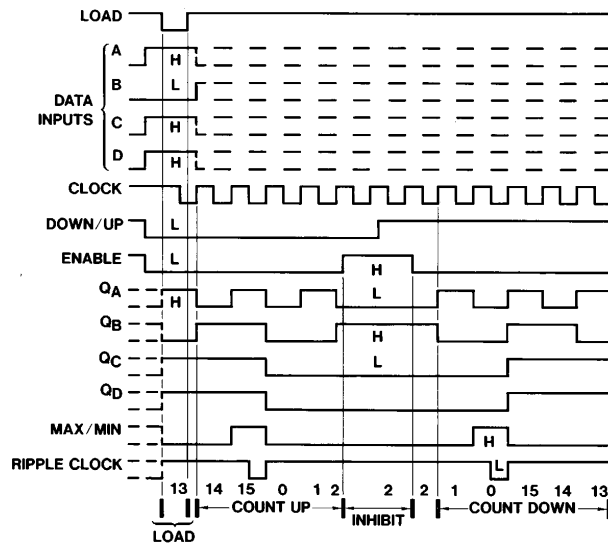
Timing Diagrams

LS190 Decade Counters
Typical Load, Count, and Inhibit Sequences



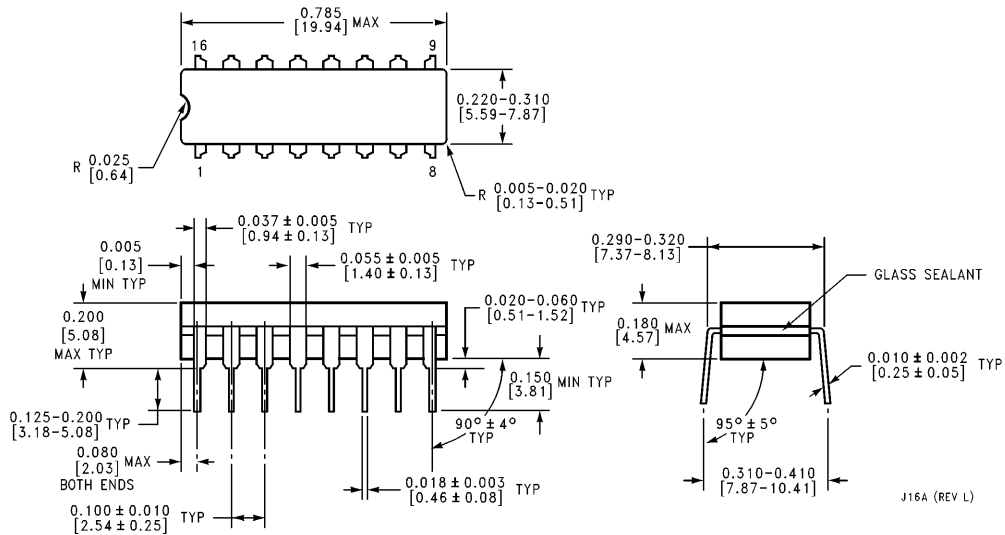
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LS191 Binary Counters
Typical Load, Count, and Inhibit Sequences

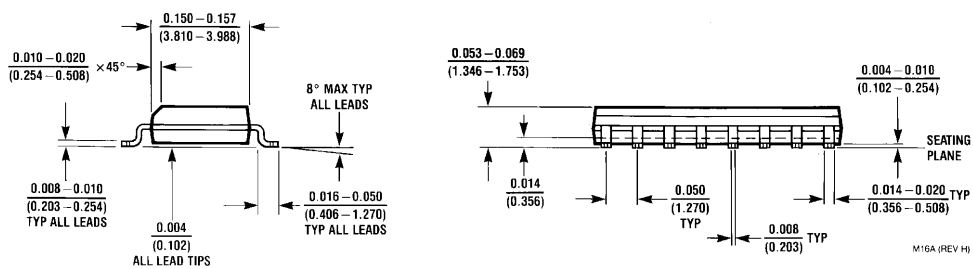
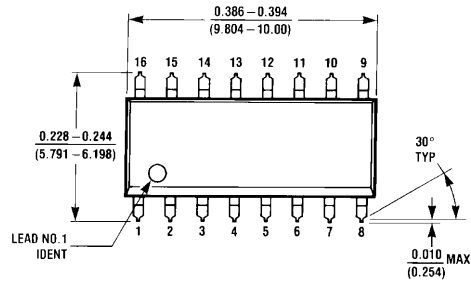


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Physical Dimensions inches (millimeters)



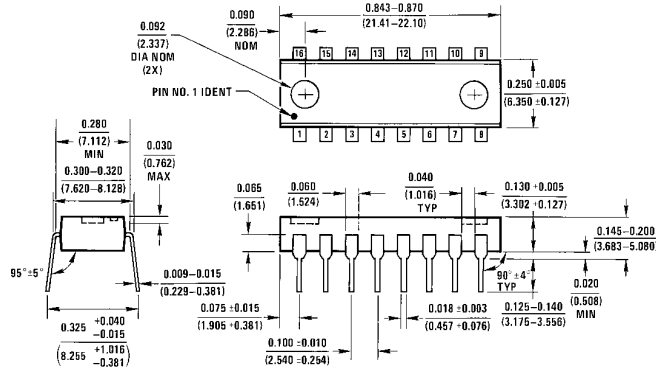
16-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS190J, DM54LS191J
NS Package Number J16A



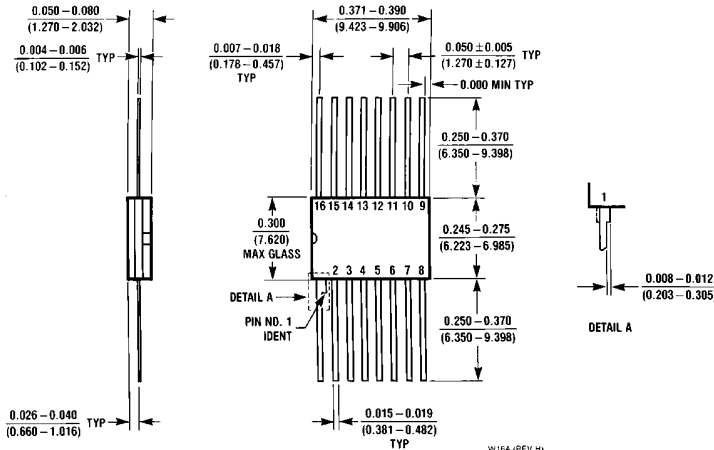
16-Lead Small Outline Molded Package (M)
Order Number DM74LS190M, DM74LS191M
NS Package Number M16A

DM54LS190/DM74LS190, DM54LS191/DM74LS191
Synchronous 4-Bit Up/Down Counters with Mode Control

Physical Dimensions inches (millimeters) (Continued)



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS190N, DM74LS191N
NS Package Number N16E



16-Lead Ceramic Flat Package (W)
Order Number DM54LS190W or DM54LS191W
NS Package Number W16A

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