- **Separate Supply Voltage Pins for Isolation of Frequency Control Inputs and Oscillators from Output Circuitry**
- **Highly Stable Operation over Specified Temperature and/or Supply Voltage Ranges**

DEVICE TYPE	SIMILAR TO	NUMBER VCO's	COMP'L Z OUT	ENABLE	RANGE INPUT	R_{ext}
'LS624	'LS324	single	yes	yes	yes	no
'LS625	'LS325	dual	yes	no	no	no
'LS626	'LS326	dual	yes	yes	no	no
'LS627	'LS327	dual	no	no	no	no
'LS628	'LS324	single	yes	yes	yes	yes
'LS629	'LS124	dual	no	yes	yes	no

description

These voltage-controlled oscillators (VCOs) are improved versions of the original VCO family: SN54LS124, SN54LS324 thru SN54LS327, SN74LS124, and SN74LS324 thru SN74LS327. These new devices feature improved voltage-to-frequency linearity, range, and compensation. With the exception of the 'LS624 and 'LS628, all of these devices feature two independent VCOs in a single monolithic chip. The 'LS624, 'LS625, 'LS626, and 'LS628 have complementary Z outputs. The output frequency for each VCO is established by a single external component (either a capacitor or crystal) in combination with voltage-sensitive inputs used for frequency control and frequency range. Each device has a voltage-sensitive input for frequency control; however, the 'LS624, 'LS628, and 'LS629 devices also have one for frequency range. (See Figures 1 thru 6).

The 'LS628 offers more precise temperature compensation than its 'LS624 counterpart. The 'LS624 features a 600 ohm internal timing resistor. The 'LS628 requires a timing resistor to be connected externally across R_{ext} pins. Temperature compensation will be improved dur to the temperature coefficient of the external resistor.

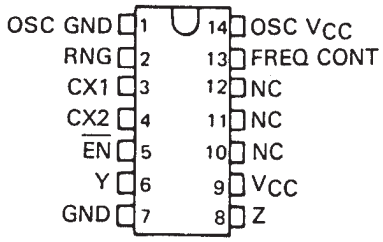
Figure 3 and Figure 6 contain the necessary information to choose the proper capacitor value to obtain the desired operating frequency.

A single 5-volt supply can be used: however, one set of supply voltage and ground pins (V_{CC} and GND) is provided for the enable, synchronization-gating, and output sections, and a separate set (OSC V_{CC} and OSC GND) is provided for the oscillator and associated frequency-control circuits so that effective isolation can be accomplished in the system. For operation of frequencies greater than 10 MHz, it is recommended that two independent supplies be used. Disabling either VCO of the 'LS625 and 'LS625 and 'LS627 can be achieved by removing the appropriate OSC V_{CC}. An enable input is provided on the 'LS624, 'LS626, 'LS628, and 'LS629. When the enable input is low, the output is enabled: when the enable input is high, the internal oscillator is disabled, Y is high, and Z is low. Caution! Crosstalk may occur in the dual devices ('LS625, 'LS626, 'LS627 and 'LS629) when both VCOs are operated simultaneously. To minimize crosstalk, either of the following are recommended: (A) If frequencies are widely separated, use a 10-μh inductor between V_{CC} pins. (B) If frequencies are closely spaced, use two separate V_{CC} supplies or place two series diodes between the V_{CC} pins.

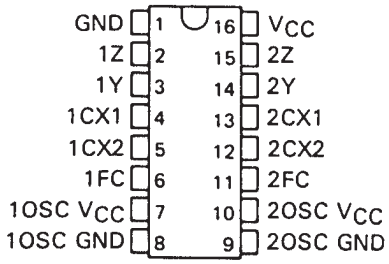
The pulse-synchronization-gating section ensures that the first output pulse is neither clipped nor extended. The duty cycle of the square-wave output is fixed at approximately 50 percent.

The SN54LS624 thru SN54LS629 are characterized for operation over the full military temperature range of $-55°C$ to $125°C$. The SN74LS624 thru SN74LS629 are characterized for operation from $0°C$ to $70°C$.

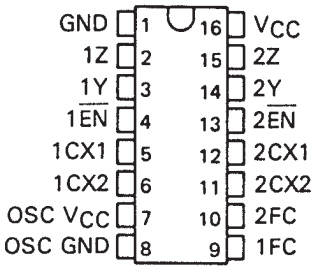
SN54LS624 . . . J OR W PACKAGE
SN74LS624 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS625 . . . J OR W PACKAGE
SN74LS625 . . . D OR N PACKAGE
(TOP VIEW)

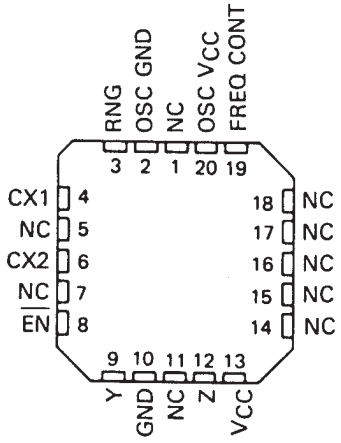


SN54LS626 . . . J OR W PACKAGE
SN74LS626 . . . D OR N PACKAGE
(TOP VIEW)

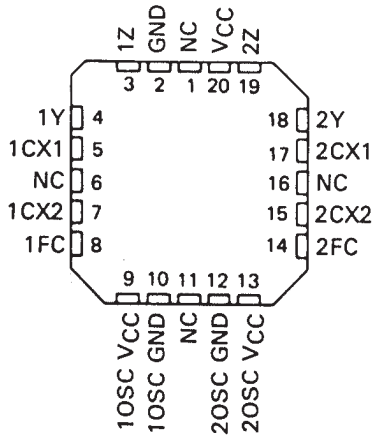


NC – No internal connection

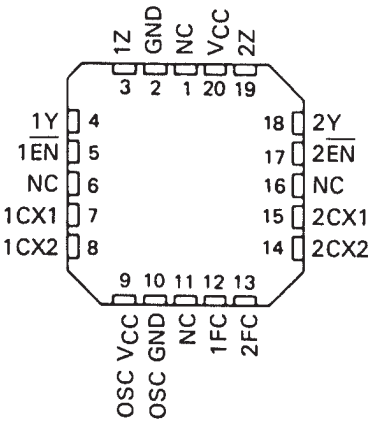
SN54LS624 . . . FK PACKAGE
(TOP VIEW)



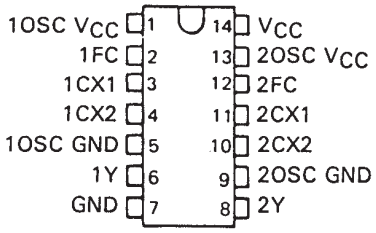
SN54LS625 . . . FK PACKAGE
(TOP VIEW)



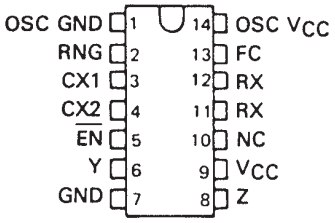
SN54LS626 . . . FK PACKAGE
(TOP VIEW)



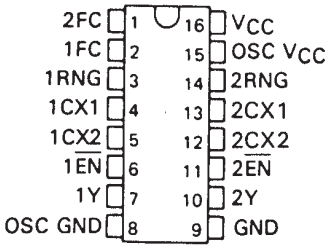
SN54LS627 . . . J OR W PACKAGE
SN74LS627 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS628 . . . J OR W PACKAGE
SN74LS628 . . . D OR N PACKAGE
(TOP VIEW)

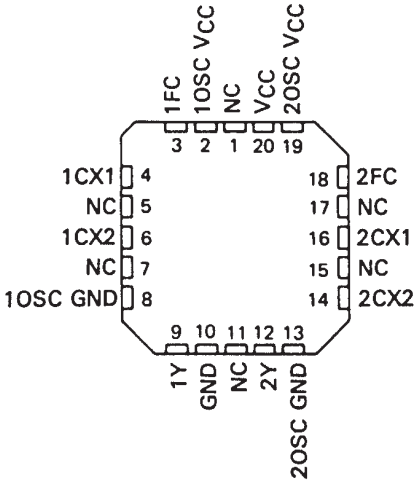


SN54LS629 . . . J OR W PACKAGE
SN74LS629 . . . D OR N PACKAGE
(TOP VIEW)

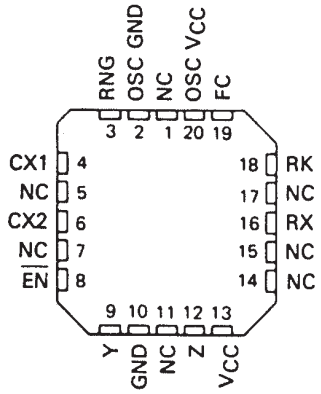


NC-No internal connection

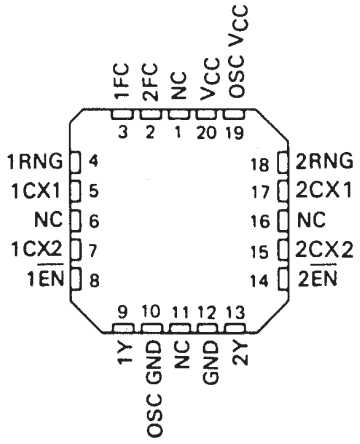
SN54LS627 . . . FK PACKAGE
(TOP VIEW)



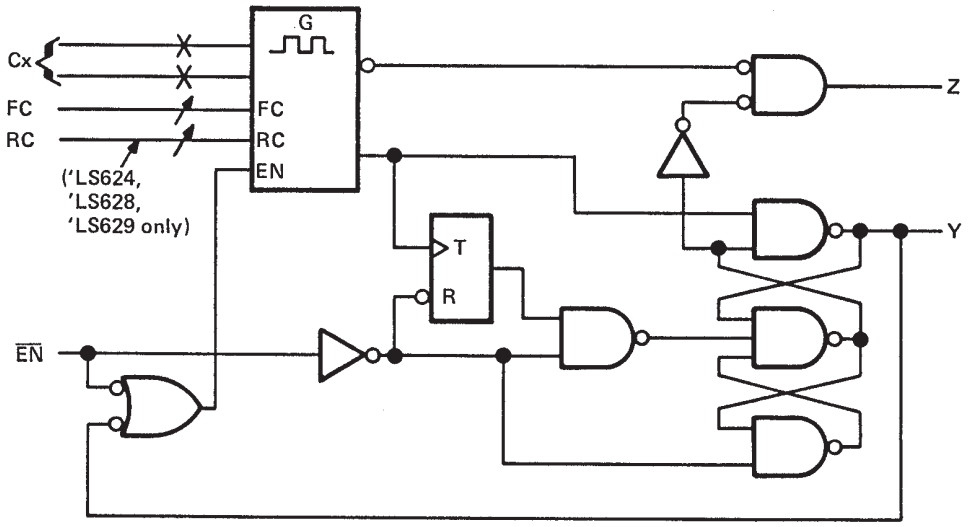
SN54LS628 . . . FK PACKAGE
(TOP VIEW)



SN54LS629 . . . FK PACKAGE
(TOP VIEW)

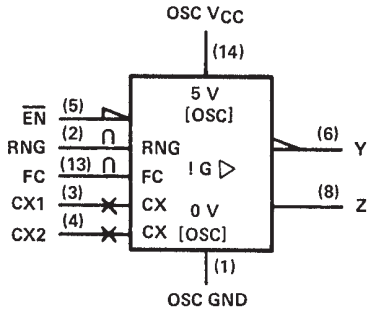


logic diagram (positive logic)

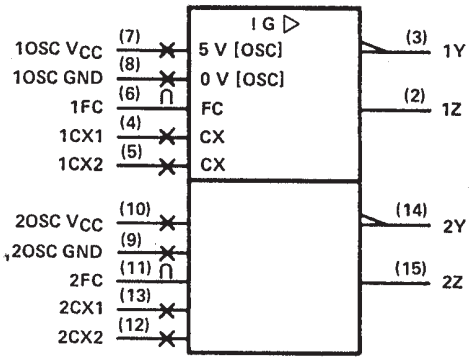


logic symbols†

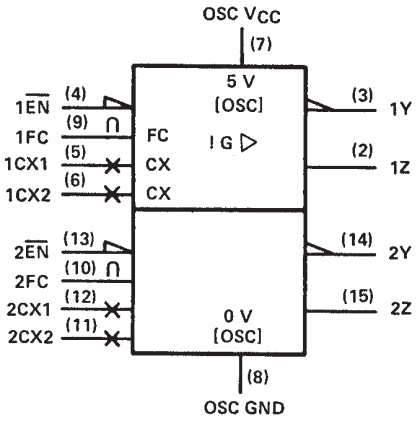
'LS624



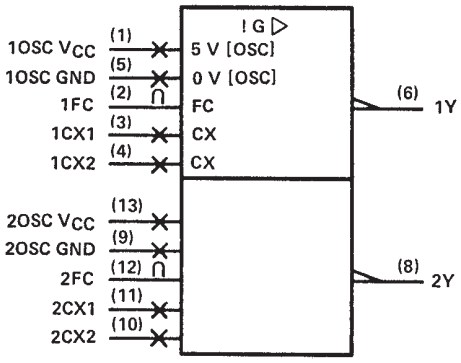
'LS625



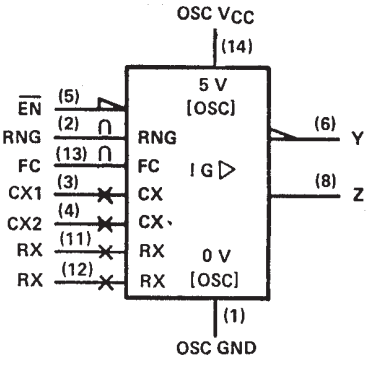
'LS626



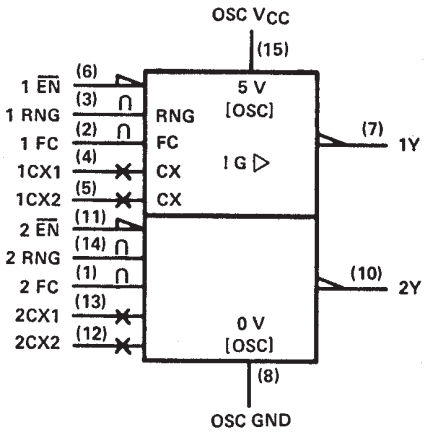
'LS627



'LS628

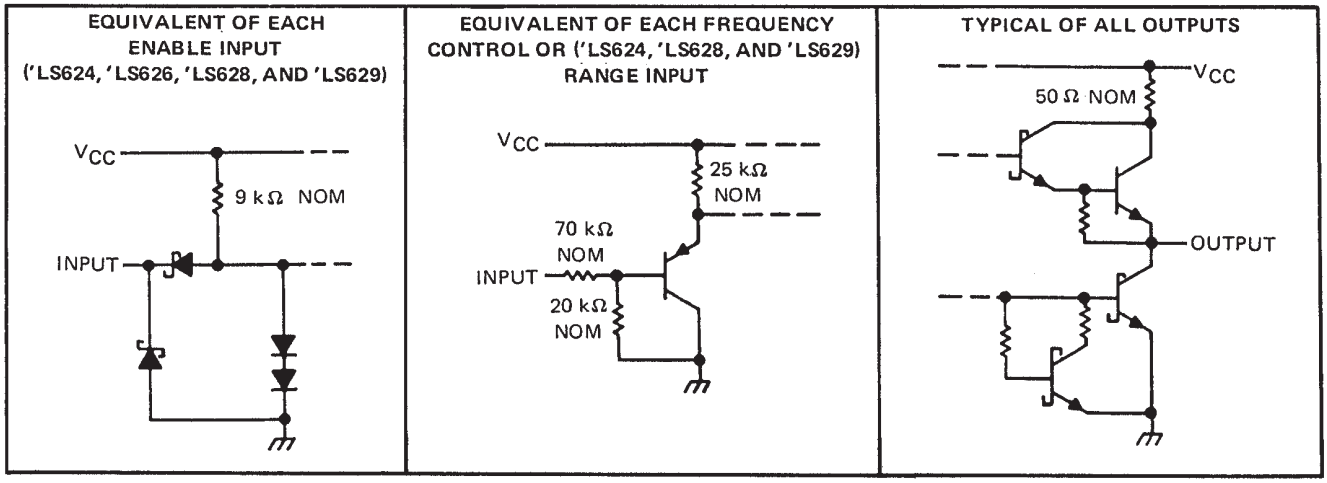


'LS629



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Notes 1 and 2) . . . . . 7 V
Input voltage: Enable input† . . . . . 7 V
Frequency control or range input‡ . . . . . V_{CC}
Operating free-air temperature range: SN54LS' Circuits . . . . . −55°C to 125°C
SN74LS' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† The enable input is provided only on the 'LS624, 'LS626, 'LS628, and 'LS629.
‡ The range input is provided only on 'LS624, 'LS628, and 'LS629.

NOTE: 1. Voltage values are with respect to the appropriate ground terminal.
2. Throughout the data sheet, the symbol V_{CC} is used for the voltage applied to both the V_{CC} and OSC V_{CC} terminals, unless otherwise noted.

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Input voltage at frequency control or range input, $V_{I(freq)}$ or $V_{I(rng)}$	0		5	0		5	V
High-level output current, I_{OH}			−1.2			−1.2	mA
Low-level output current, I_{OL}			12			24	mA
Output frequency, f_o	1			1			Hz
			20			20	MHz
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage at enable#				2			2			V
V_{IL}	Low-level input voltage at enable#						0.7			0.8	V
V_{IK}	Input clamp voltage at enable#		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = −1.2 mA, $\overline{EN}$ at V_{IL} max, See Note 3		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, $\overline{EN}$ at V_{IL} max, See Note 3	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_I	Input current	Freq control or range¶	V_{CC} = MAX	V_I = 5 V		50	250		50	250	μA
				V_I = 1 V		10	50		10	50	
I_I	Input current at maximum input voltage	Enable#	V_{CC} = MAX, V_I = 7 V				0.2			0.2	mA
I_{IH}	High-level input current	Enable#	V_{CC} = MAX, V_I = 2.7 V				40			40	μA
I_{IL}	Low-level input current	Enable#	V_{CC} = MAX, V_I = 0.4 V				−0.8			−0.8	mA
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply current, total into V_{CC} and OSC V_{CC} pins		V_{CC} = MAX, Enable# = 4.5 V, See Note 4	'LS624		20	35		20	35	mA
				'LS625		35	55		35	55	
				'LS626		35	55		35	55	
				'LS627		35	55		35	55	
				'LS628		20	35		20	35	
				'LS629		35	55		35	55	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
¶The range input is provided only on the 'LS624, 'LS628, and 'LS629.
#The enable input is provided only on the 'LS624, 'LS626, 'LS628, and 'LS629.

NOTES: 3. V_{OH} for Y outputs and V_{OL} for Z outputs are measured while enable inputs are at V_{IL} MAX, with individual 1-kΩ resistors connected from CX1 to V_{CC} and from CX2 to ground. The resistor connections are reversed for testing V_{OH} for Z outputs and V_{OL} for Y inputs.
4. For 'LS624, 'LS626, 'LS628, and 'LS629, I_{CC} is measured with the outputs disabled and open. For 'LS625 and 'LS627, I_{CC} is measured with one OSC V_{CC} = MAX, and with the other OSC V_{CC} and outputs open.

switching characteristics, V_{CC} = 5 V (unless otherwise noted), R_L = 667 Ω, C_L = 45 pF, T_A = 25 °C

PARAMETER		TEST CONDITIONS		'LS624, 'LS628, 'LS629			'LS625, 'LS626, 'LS627			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_O	Output frequency	C_{ext} = 50 pF	$V_{I(freq)}$ = 5 V, $V_{I(rng)}$ = 0 V	15	20	25				MHz
			$V_{I(freq)}$ = 1 V, $V_{I(rng)}$ = 5 V	1.1	1.6	2.1				
			$V_{I(freq)}$ = 5 V				7	9.5	12	
			$V_{I(freq)}$ = 0 V				0.9	1.2	1.5	

TYPICAL CHARACTERISTICS

'LS624, 'LS628, 'LS629

OUTPUT FREQUENCY
vs
FREQUENCY-CONTROL INPUT VOLTAGE†

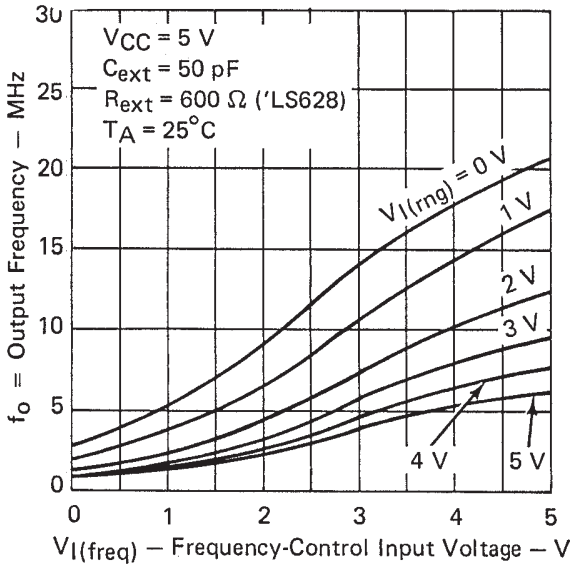


FIGURE 1

'LS624, 'LS628, 'LS629

OUTPUT FREQUENCY
vs
FREQUENCY-CONTROL INPUT VOLTAGE†

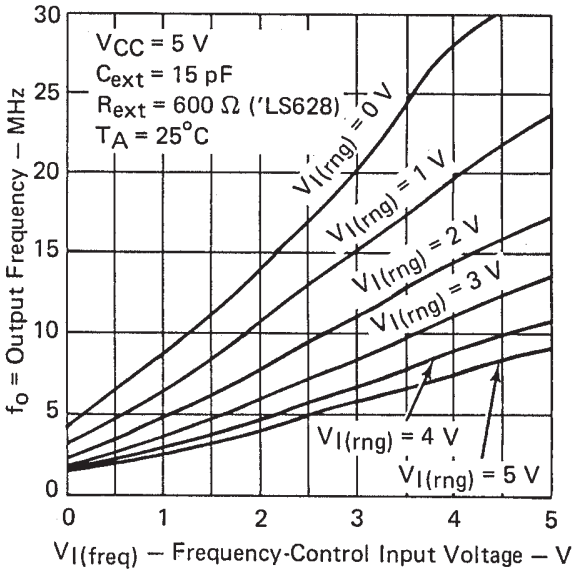


FIGURE 2

†Due to the effects of stray capacitance the output frequency may be unstable when the frequency control voltage is less than 1 volt.

TYPICAL CHARACTERISTICS

'LS624, 'LS628, 'LS629

OUTPUT FREQUENCY
vs
EXTERNAL CAPACITANCE

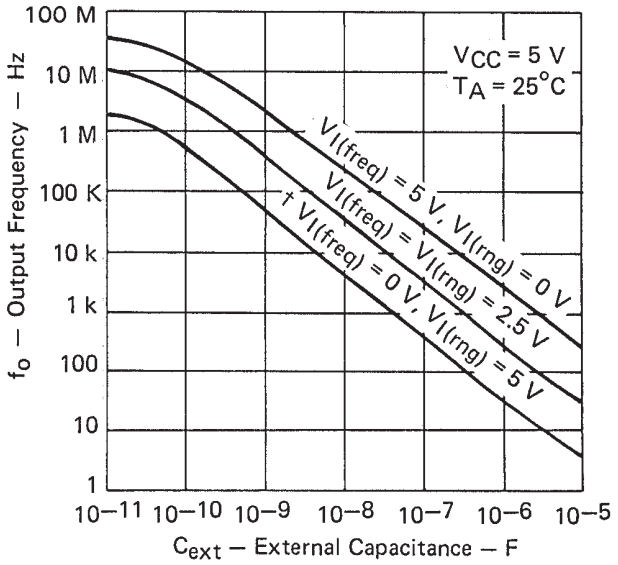


FIGURE 3

'LS625, 'LS626, 'LS627

OUTPUT FREQUENCY
vs
FREQUENCY-CONTROL INPUT VOLTAGE†

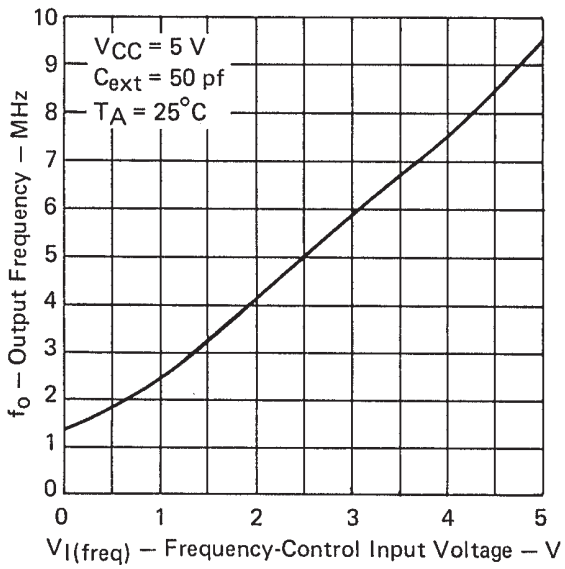


FIGURE 4

'LS625, 'LS626, 'LS627

OUTPUT FREQUENCY
vs
FREQUENCY-CONTROL INPUT VOLTAGE

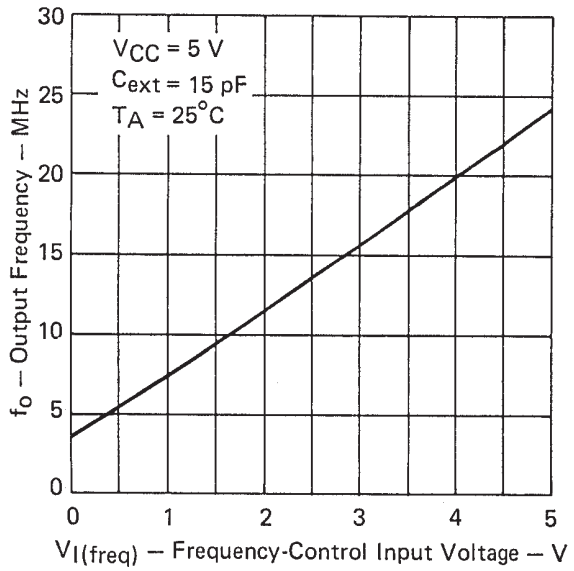


FIGURE 5

'LS625, 'LS626, 'LS627

OUTPUT FREQUENCY
vs
EXTERNAL CAPACITANCE

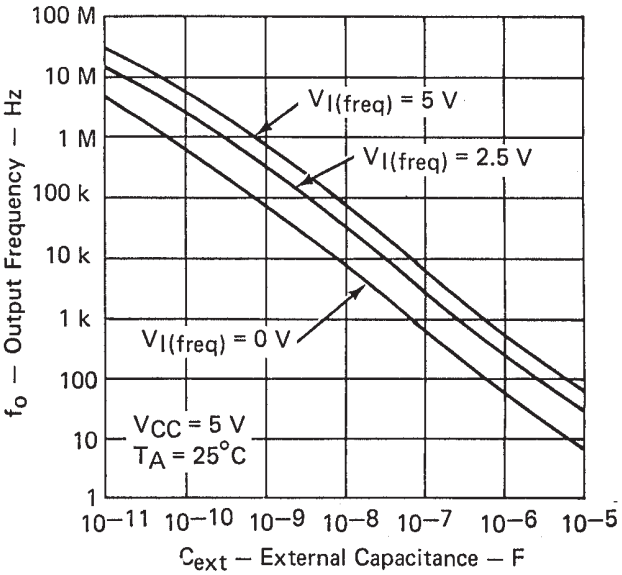


FIGURE 6

† Due to the effects of stray capacitance the output frequency may be unstable when the frequency control voltage is less than 1 volt.

TYPICAL CHARACTERISTICS

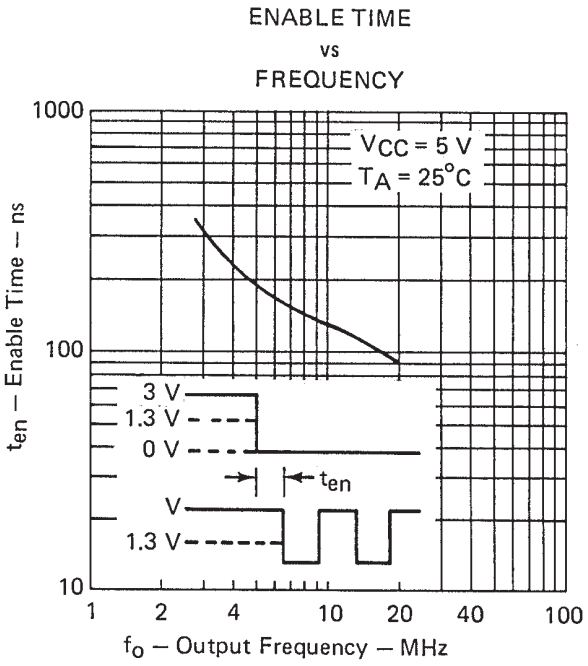
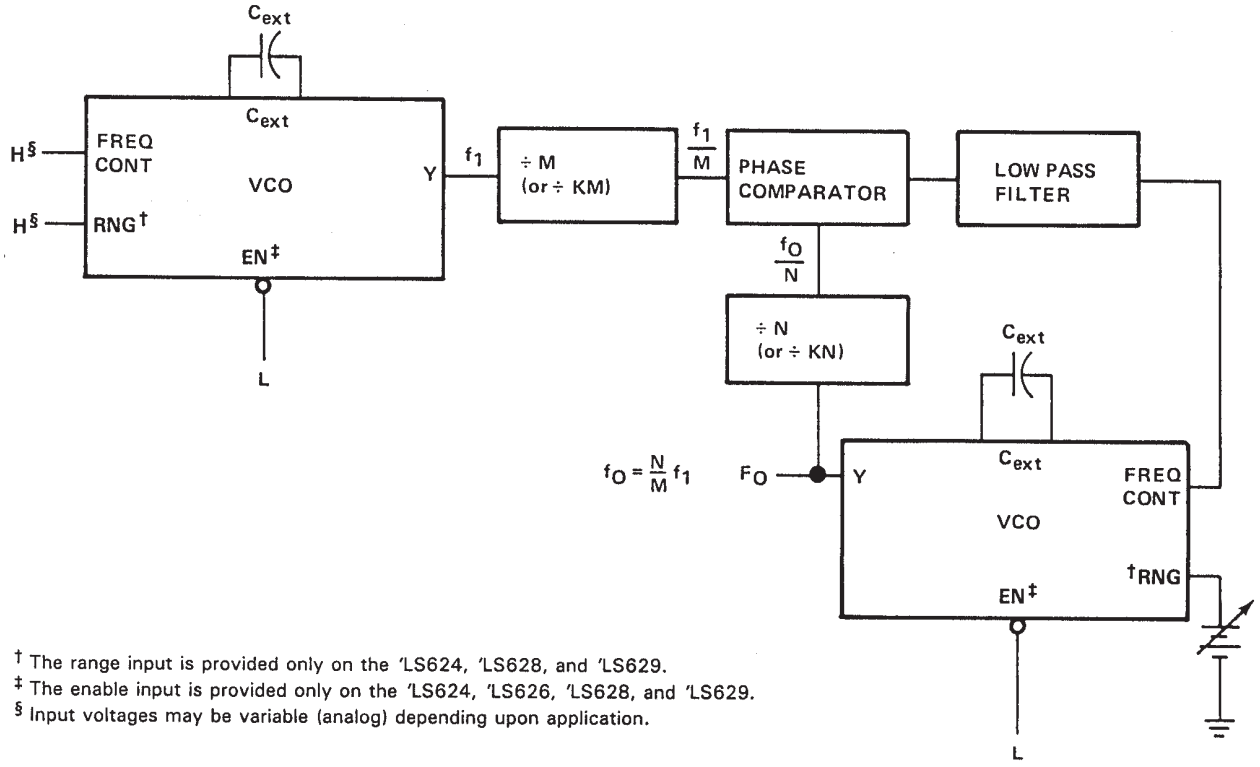


FIGURE 7

TYPICAL APPLICATIONS DATA

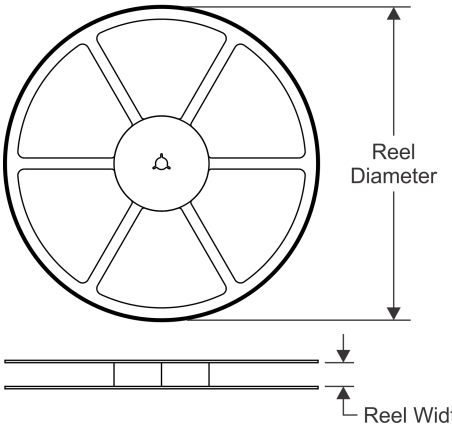


† The range input is provided only on the 'LS624, 'LS628, and 'LS629.
‡ The enable input is provided only on the 'LS624, 'LS626, 'LS628, and 'LS629.
§ Input voltages may be variable (analog) depending upon application.

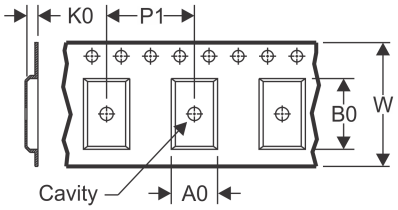
FIGURE A–PHASE-LOCKED LOOP.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

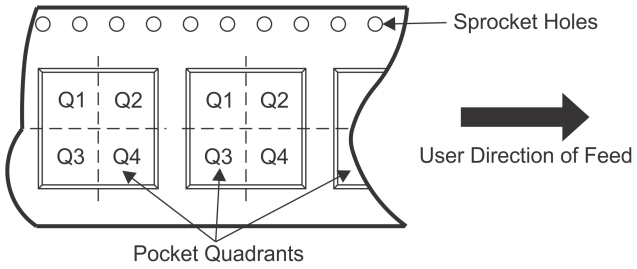


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

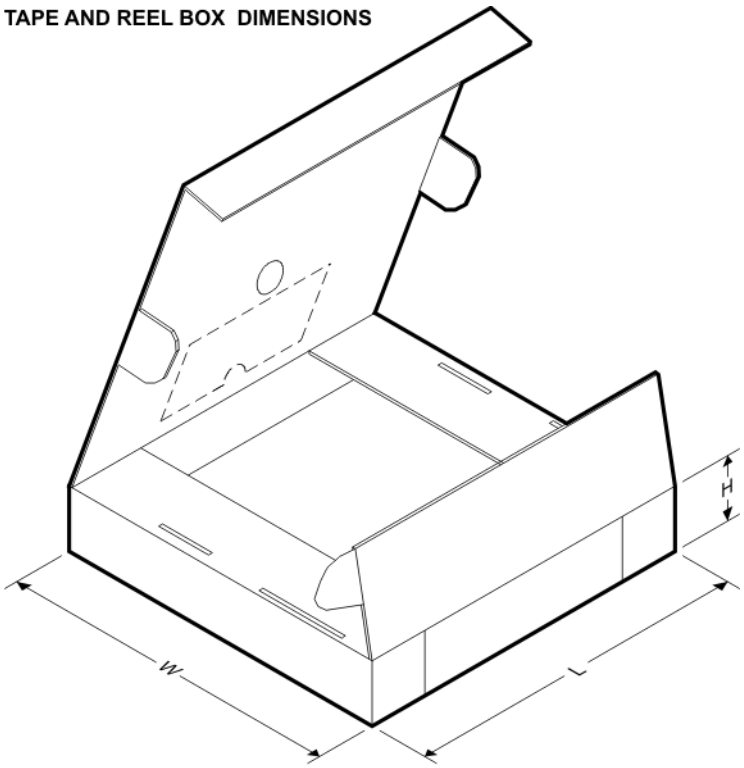
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS624DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS624NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LS628DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

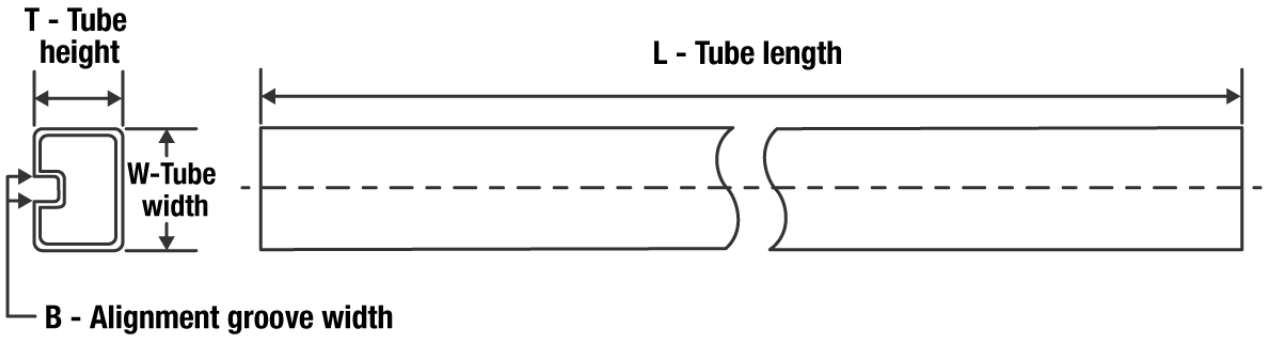
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS624DR	SOIC	D	14	2500	853.0	449.0	35.0
SN74LS624NSR	SO	NS	14	2000	853.0	449.0	35.0
SN74LS628DR	SOIC	D	14	2500	853.0	449.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9204601M2A	FK	LCCC	20	1	506.98	12.06	2030	NA
81021012A	FK	LCCC	20	1	506.98	12.06	2030	NA
SN74LS624D	D	SOIC	14	50	506.6	8	3940	4.32
SN74LS624N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS624N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS628D	D	SOIC	14	50	506.6	8	3940	4.32
SN74LS628N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS628N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS628NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS628NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS629D	D	SOIC	16	40	507	8	3940	4.32
SN74LS629N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS629N	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54LS628FK	FK	LCCC	20	1	506.98	12.06	2030	NA
SNJ54LS629FK	FK	LCCC	20	1	506.98	12.06	2030	NA

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265