National Semiconductor

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54LVX3245
8-Bit Dual Supply Translating Transceiver with TRI-STATE® Outputs

General Description

The LVX3245 is a dual-supply, 8-bit translating transceiver that is designed to interface between a 3V bus and a 5V bus in a mixed 3V/5V supply environment. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a TRI-STATE condition. The A port interfaces with the 3V bus; the B port interfaces with the 5V bus.

The LVX3245 is suitable for mixed voltage applications such as systems using 3.3V memories which must interface with existing busses or other components operating at 5.0V.

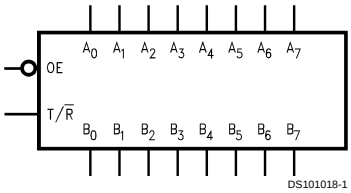
Features

- Bidirectional interface between 3V and 5V buses
- Inputs compatible with TTL level
- 3V data flow at A port and 5V data flow at B port
- Outputs source/sink 24 mA
- Available in ceramic DIP and Flatpack packages
- Implements proprietary EMI reduction circuitry
- Functionally compatible with the 54 series 245
- Standard Microcircuit Drawing (SMD) 5962-9860501

Ordering Code

Order Number	Package Number	Package Description
54LVX3245J-QML	J24F	24-Lead Ceramic Dual-in-line
54LVX3245W-QML	W24C	24-Lead Cerpack

Logic Symbol



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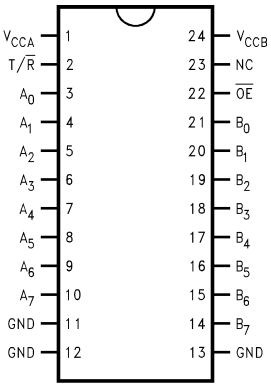
Connection Diagram

Pin Assignment for CDIP and Cerpack



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Pin Descriptions

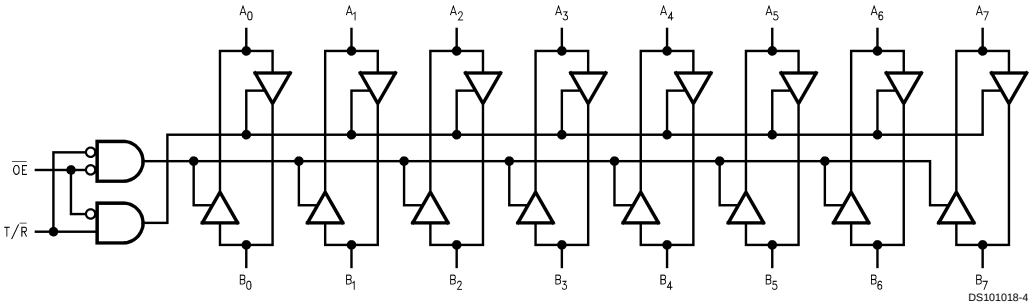
Pin Names	Description
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or TRI-STATE Outputs
B_0–B_7	Side B Inputs or TRI-STATE Outputs

Truth Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = High Voltage Level
L = Low Voltage Level
I = Immaterial

Logic Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CCA}, V_{CCB})	−0.5V to +7.0V
DC Input Voltage (V_I) @ $\overline{OE}$, T/$\overline{R}$	−0.5V to V_{CCB} + 0.5V
DC Input/Output Voltage ($V_{I/O}$)	
@ A(n)	−0.5V to V_{CCA} + 0.5V
@ B(n)	−0.5V to V_{CCB} + 0.5V
DC Input Diode Current (I_{IN}) @ $\overline{OE}$, T/$\overline{R}$	±20 mA
DC Output Diode Current (I_{OK})	±50 mA
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
and Max Current @ I_{CCA}	±200 mA
@ I_{CCB}	±200 mA
Storage Temperature Range (T_{STG})	−65˚C to +150˚C

Recommended Operating Conditions (Note 2)

Supply Voltage	
V_{CCA}	2.7V to 3.6V
V_{CCB}	4.5V to 5.5V
Input Voltage (V_I) @ $\overline{OE}$, T/$\overline{R}$	0V to V_{CCB}
Input/Output Voltage ($V_{I/O}$)	
@ A(n)	0V to V_{CCA}
@ B(n)	0V to V_{CCB}
Free Air Operating Temperature (T_A)	−55˚C to +125˚C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	8 ns/V
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V, 4.5V, 5.5V	

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: Unused Pins (inputs and I/Os) must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter		V_{CCA} (V)	V_{CCB} (V)	T_A = −55˚C to +125˚C Guaranteed Limits	Units	Conditions
V_{IHA}	Minimum High Level Input Voltage	A(n), T/$\overline{R}$, $\overline{OE}$	3.6	5.0	2.0	V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
			2.7	5.0	2.0		
V_{IHB}		B(n)	3.3	4.5	2.0		
			3.3	5.5	2.0		
V_{ILA}	Maximum Low Level Input Voltage	A(n), T/$\overline{R}$, $\overline{OE}$	3.6	5.0	0.8	V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
			2.7	5.0	0.8		
V_{ILB}		B(n)	3.3	4.5	0.8		
			3.3	5.5	0.8		
V_{OHA}	Minimum High Level Output Voltage		2.7	4.5	2.6	V	I_{OH} = −100 µA
			3.6	5.5	3.5		I_{OH} = −100 µA
			2.7	4.5	2.2		I_{OH} = −12 mA
			3.0	4.5	2.4		I_{OH} = −12 mA
			3.0	4.5	2.2		I_{OH} = −24 mA
V_{OHB}			2.7	4.5	4.4	V	I_{OH} = −100 µA
			3.6	5.5	5.4		I_{OH} = −100 µA
			3.0	4.5	3.7		I_{OH} = −24 mA
V_{OLA}	Maximum Low Level Output Voltage		2.7	4.5	0.1	V	I_{OL} =100 µA
			3.6	5.5	0.1		I_{OL} =100 µA
			2.7	4.5	0.4		I_{OL} = 12 mA
			3.0	4.5	0.3		I_{OL} = 12 mA
			3.0	4.5	0.4		I_{OL} = 24 mA
V_{OLB}			2.7	4.5	0.1	V	I_{OL} = 100 µA
			3.6	5.5	0.1		I_{OL} = 100 µA
			3.0	4.5	0.4		I_{OL} = 24 mA

DC Electrical Characteristics (Continued)

Symbol	Parameter		V_{CCA} (V)	V_{CCB} (V)	$T_A = -55^\circ C$ to $+125^\circ C$ Guaranteed Limits	Units	Conditions
I_{IN}	Maximum Input Leakage Current @ $\overline{OE}$, T/$\overline{R}$		3.6	5.5	±1.0	µA	$V_I = V_{CCB}$, GND
I_{OZA}	Maximum TRI-STATE Output Leakage @ A(n)		3.6	5.5	±5.0	µA	T/$\overline{R}$ = 0.0V, $\overline{OE}$ = V_{IH} $V_O = V_{CCA}$, GND
I_{OZB}	Maximum TRI-STATE Output Leakage @ B(n)		3.6	5.5	±5.0	µA	T/$\overline{R}$ = 3.6V, $\overline{OE}$ = V_{IH} $V_O = V_{CCB}$, GND
ΔI_{CC}	Maximum	B(n)	3.6	5.5	1.5	mA	$V_I = V_{CCB} - 2.1V$, T/$\overline{R}$ = 0.0V
	I_{CCT}/Input @	A(n), T/$\overline{R}$, $\overline{OE}$	3.6	5.5	500	µA	$V_I = V_{CCA} - 0.6V$ T/$\overline{R}$ = 3.6V
I_{CCA}	Quiescent V_{CCA} Supply Current		3.6	5.5	10	µA	B(n) = V_{CCB} or GND $\overline{OE}$ = GND, T/$\overline{R}$ = GND
I_{CCB}	Quiescent V_{CCB} Supply Current		3.6	5.5	40	µA	A(n) = V_{CCA} or GND $\overline{OE}$ = GND, T/$\overline{R}$ = V_{CCA}
V_{OLPA}	Quiet Output Maximum		3.3	5.0	1.1	V	(Note 4) (Note 5)
V_{OLPB}	Dynamic V_{OL}		3.3	5.0	1.6		
V_{OLVA}	Quiet Output Minimum		3.3	5.0	-0.8	V	(Note 4) (Note 5)
V_{OLVB}	Dynamic V_{OL}		3.3	5.0	-1.1		

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: Worst case package.

Note 5: Max number of outputs defined as (n). Data inputs are driven 0V to V_{CC} level; one output at GND.

AC Electrical Characteristics

Symbol	Parameters	T_A = −55˚C to +125˚C C_L = 50 pF V_{CCA} = 3.3V (Note 7) V_{CCB} = 5.0V (Note 6)		T_A = −55˚C to +125˚C C_L = 50 pF V_{CCA}=2.7V V_{CCB}=5.0V (Note 6)		Units
		Min	Max	Min	Max	
t_{PHL}	Propagation Delay	1.0	8.5	1.0	9.0	ns
t_{PLH}	A to B	1.0	8.5	1.0	9.0	
t_{PHL}	Propagation Delay	1.0	8.0	1.0	8.5	ns
t_{PLH}	B to A	1.0	8.0	1.0	8.5	
t_{PZL}	Output Enable	1.0	8.5	1.0	9.0	ns
t_{PZH}	Time $\overline{OE}$ to B	1.0	8.5	1.0	9.0	
t_{PZL}	Output Enable	1.0	9.5	1.0	10.5	ns
t_{PZH}	Time $\overline{OE}$ to A	1.0	9.5	1.0	10.5	
t_{PHZ}	Output Disable	1.0	7.5	1.0	7.5	ns
t_{PLZ}	Time $\overline{OE}$ to B	1.0	7.5	1.0	7.5	
t_{PHZ}	Output Disable	1.0	7.0	1.0	7.0	ns
t_{PLZ}	Time $\overline{OE}$ to A	1.0	7.0	1.0	7.0	
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 8) Data to Output		1.5		1.5	ns

Note 6: Voltage Range 5.0V is 5.0V ±0.5V.

Note 7: Voltage Range 3.3V is 3.3V ±0.3V.

Note 8: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

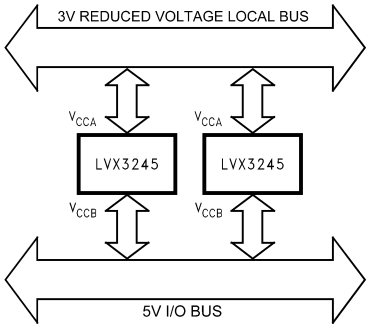
Symbol	Parameter	Max	Units	Conditions
C_{IN}	Input Capacitance	10	pF	V_{CC} = Open
$C_{I/O}$	Input/Output Capacitance	12	pF	V_{CCA} = 3.3V V_{CCB} = 5.0V
C_{PD}	Power Dissipation Capacitance	50	pF	V_{CCB} = 5.0V V_{CCA} = 3.3V

Note 9: C_{PD} is measured at 10 MHz

8-Bit Dual Supply Translating Transceiver

The LVX3245 is a dual supply device capable of bidirectional signal translation. This level shifting ability provides an efficient interface between low voltage CPU local bus with memory and a standard bus defined by 5V I/O levels. The device control inputs can be controlled by either the low voltage CPU and core logic or a bus arbitrator with 5V I/O levels.

Manufactured on a sub-micron CMOS process, the LVX3245 is suitable for mixed voltage applications such as systems using 3.3V memories which must interface with existing busses or other components operating at 5.0V.



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Applications: Mixed Mode Dual Supply Interface Solution

LVX3245 is designed to solve 3V/5V interfacing issues when CMOS devices cannot tolerate I/O levels above their applied V_{CC}. If an I/O pin of 3V ICs is driven by 5V ICs, the P-Channel transistor in 3V ICs will conduct causing current flow from I/O bus to the 3V power supply. The resulting high current flow can cause destruction of 3V ICs through latchup effects. To prevent this problem, a current limiting resistor is used typically under direct connection of 3V ICs and 5V ICs, but it causes speed degradation.

In a better solution, the LVX3245 configures two different output levels to handle the dual supply interface issues. The "A" port is a dedicated 3V port to interface 3V ICs. The "B" port is a dedicated port to interface 5V ICs. *Figure 1* shows how LVX3245 fits into a system with 3V subsystem and 5V subsystem.

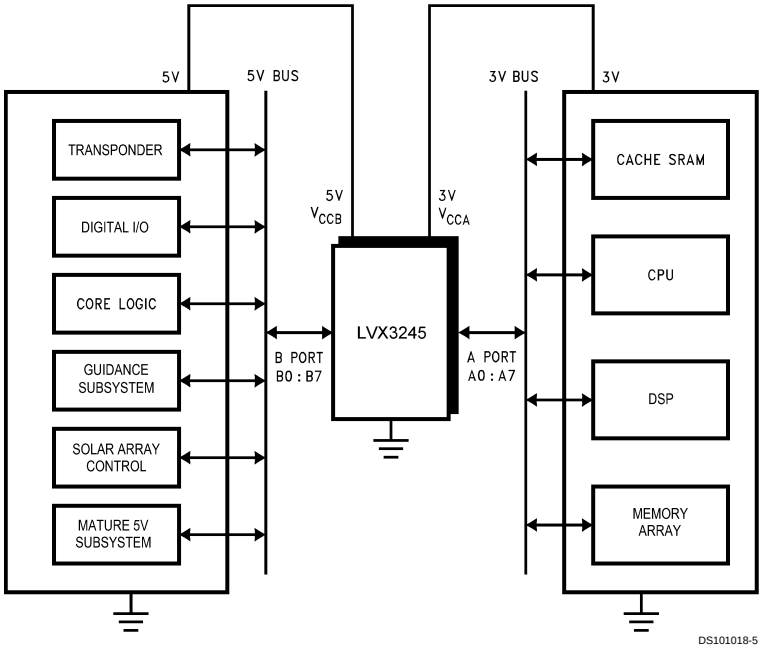
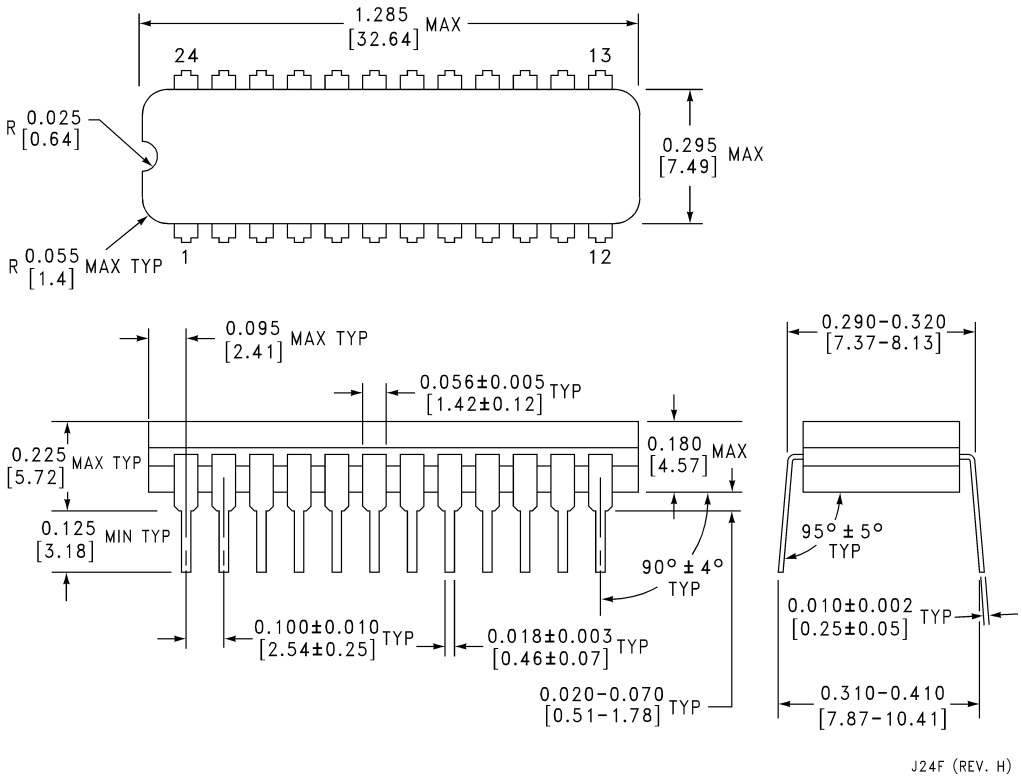
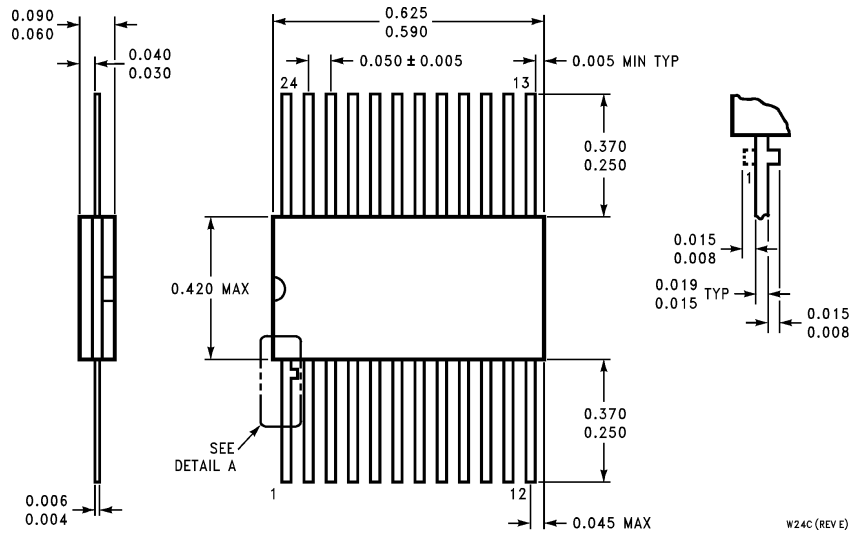


FIGURE 1. LVX3245 Fits into a System with 3V Subsystem and 5V Subsystem

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Ceramic DIP
Package Number J24F



24-Lead Cerpack
Package Number W24C

Notes

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