REVISIONS

| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
|---|---|---|---|
| A | Change AC limits in table I. Add vendor CAGE 18714 to device type 01CX. Editorial changes throughout. | 87-11-16 | R. R. Evans |
| B | Changes in accordance with NOR 5962-R100-93. | 93-03-23 | Monica L. Poelking |
| C | Changes in accordance with NOR 5962-R181-93. | 93-06-25 | Monica L. Poelking |
| D | Add vendor CAGE F8859. Add device Class V criteria. Add delta limits, table III. Add case outline X. Update boilerplate to MIL-PRF-38535 requirements. – lgt | 01-03-23 | Raymond Monnin |
| E | Add section 1.5, radiation features. Update the boilerplate to include radiation hardness assured requirements. Editorial changes throughout. - TVN | 03-10-01 | Thomas M. Hess |

**THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.**
**CURRENT CAGE CODE 67268**

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|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV | | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | | |
| REV | E | | | | | | | | | | | | | | | | | | | |
| SHEET | 15 | | | | | | | | | | | | | | | | | | | |

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| REV STATUS OF SHEETS | REV | E | E | E | E | E | E | E | E | D | D | E | E | E | E |
| | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |

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| PMIC N/A | PREPARED BY<br>Greg A. Pitz | **DEFENSE SUPPLY CENTER COLUMBUS**<br>**COLUMBUS, OHIO 43216**<br>**http://www.dscc.dla.mil** |
| **STANDARD MICROCIRCUIT DRAWING**<br>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE<br>AMSC N/A | CHECKED BY<br>N. A. Hauck | |
| | APPROVED BY<br>N. A. Hauck | MICROCIRCUIT, DIGITAL, ADVANCED CMOS, QUAD 2-INPUT NAND GATE, MONOLITHIC SILICON |
| | DRAWING APPROVAL DATE<br>87-04-29 | |
| | REVISION LEVEL<br>**E** | SIZE **A** / CAGE CODE **14933** / **5962-87549** |
| | | SHEET 1 OF 15 |

## 1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:

For device classes M and Q:

```
    5962              -              87549      01          C          A
     |                |                         |           |          |
  Federal            RHA                      Device       Case       Lead
  stock class      designator                 type        outline    finish
  designator       (see 1.2.1)              (see 1.2.2)  (see 1.2.4) (see 1.2.5)
\_________________  _________________/
                  \/
            Drawing number
```

For device class V:

```
    5962              F              87549      01          V           X           A
     |                |                         |           |           |           |
  Federal            RHA                      Device      Device       Case        Lead
  stock class      designator                 type        class       outline     finish
  designator       (see 1.2.1)              (see 1.2.2)  designator  (see 1.2.4) (see 1.2.5)
                                                         (see 1.2.3)
\_________________  _________________/
                  \/
            Drawing number
```

1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | 54AC00 | Quad 2-input NAND gate |
| 02 | 54AC11000 | Quad 2-input NAND gate |

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing, device classes M and Q designators will not be included in the PIN and will not be marked on the device.

| Device class | Device requirements documentation |
|---|---|
| M | Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A |
| Q or V | Certification and qualification to MIL-PRF-38535 |

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| C | GDIP1-T14 or CDIP2-T14 | 14 | Dual-in-line |
| D | GDFP1-F14 or CDFP2-F14 | 14 | Flat pack |
| E | GDIP1-T16 or CDIP2-T16 | 16 | Dual-in-line |
| F | GDFP2-F16 or CDFP3-F16 | 16 | Flat pack |
| 2 | CQCC1-N20 | 20 | Square leadless chip carrier |
| X | CDFP3-F14 | 14 | Flat pack |

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

| | |
|---|---|
| Supply voltage range ($V_{CC}$) | -0.5 V dc to +7.0 V dc |
| DC input voltage range ($V_{IN}$) | -0.5 V dc to $V_{CC}$ + 0.5 V dc |
| DC output voltage range ($V_{OUT}$) | -0.5 V dc to $V_{CC}$ + 0.5 V dc |
| Clamp diode current ($I_{IK}$, $I_{OK}$) | ±20 mA |
| DC output current | ±50 mA |
| DC $V_{CC}$ or GND current (per pin) | ±50 mA |
| Storage temperature range ($T_{STG}$) | -65°C to +150°C |
| Maximum power dissipation ($P_D$) | 500 mW |
| Lead temperature (soldering, 10 seconds) | +260°C |
| Thermal resistance, junction-to-case ($\theta_{JC}$) | See MIL-STD-1835 |
| Junction temperature ($T_J$) | +175°C 4/ |

1.4 Recommended operating conditions. 2/ 3/ 5/ 6/

| | |
|---|---|
| Supply voltage range ($V_{CC}$) | +2.0 V dc to +6.0 V dc |
| Input voltage range ($V_{IN}$) | +0.0 V dc to $V_{CC}$ |
| Output voltage range ($V_{OUT}$) | +0.0 V dc to $V_{CC}$ |
| Case operating temperature range ($T_C$) | -55°C to +125°C |
| Minimum input rise or fall rate ($\Delta V/\Delta t$): | |
| Device type 01 | 0 to 8 ns/V |
| Device type 02 | 0 to 10 ns/V |

1.5 Radiation features.

| | |
|---|---|
| Device type 01: | |
| Total dose (dose rate = 50 – 300 rads (Si)/s) | 300 krads (Si) |
| Single Event Latchup (SEL) or Single Event Upset (SEU) | ≥ 93 MeV-cm$^2$/mg |

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1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ The limits for the parameters specified herein shall apply over the full specified $V_{CC}$ range and case temperature range of -55°C to +125°C.

4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

5/ Operation from 2.0 V dc to 3.0 V dc is provided for compatibility with data retention and battery back-up systems. Data retention implies no input transition and no stored data loss with the following conditions: $V_{IH} \geq 70\%$ $V_{CC}$, $V_{IL} \leq 30\%$ $V_{CC}$, $V_{OH} \geq 70\%$ $V_{CC}$ at -20µA, $V_{OL} \leq 30\%$ $V_{CC}$ at 20 µA.

6/ Unused inputs must be held high or low to prevent them from floating.

## 2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

JEDEC Standard No. 20 - Standard for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High-Speed CMOS Devices.

(Applications for copies should be addressed to the Electronics Industries Alliance, 2500 Wilson Boulevard, Arlington, VA, 22201-3834.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 36 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ 3/ -55°C ≤ $T_C$ ≤ +125°C +3.0 V ≤ $V_{CC}$ ≤ +5.5 V Unless otherwise specified | Device type and Device class | $V_{CC}$ | Group A subgroups | Limits 4/ | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| Positive input<br>clamp voltage<br>3022 | $V_{IC+}$ | For input under test, $I_{IN}$ = 1.0 mA | All<br>Q, V | 0.0 V | 1 | 0.4 | 1.5 | V |
| Negative input<br>clamp voltage<br>3022 | $V_{IC-}$ | For input under test, $I_{IN}$ = -1.0 mA | All<br>Q, V | Open | 1 | -0.4 | -1.5 | V |
| High level output<br>voltage<br>3006 | $V_{OH}$<br>5/ | $V_{IN}$ = $V_{IH}$ minimum or $V_{IL}$ maximum<br>$I_{OH}$ = -50 µA | All<br>All | 3.0 V | 1, 2, 3 | 2.9 | | V |
| | | | | 4.5 V | | 4.4 | | |
| | | | | 5.5 V | | 5.4 | | |
| | | $V_{IN}$ = $V_{IH}$ minimum or $V_{IL}$ maximum<br>$I_{OH}$ = -12 mA | All<br>All | 3.0 V | 1 | 2.56 | | |
| | | | | | 2, 3 | 2.4 | | |
| | | $V_{IN}$ = $V_{IH}$ minimum or $V_{IL}$ maximum<br>$I_{OH}$ = -24 mA | All<br>All | 4.5 V | 1 | 3.86 | | |
| | | | | | 2, 3 | 3.7 | | |
| | | | | 5.5 V | 1 | 4.86 | | |
| | | | | | 2, 3 | 4.7 | | |
| | | $V_{IN}$ = $V_{IH}$ minimum or $V_{IL}$ maximum<br>$I_{OH}$ = -50 mA | All<br>All | 5.5 V | 1, 2, 3 | 3.85 | | |
| Low level output<br>voltage<br>3007 | $V_{OL}$<br>5/ | $V_{IN}$ = $V_{IH}$ minimum or $V_{IL}$ maximum<br>$I_{OL}$ = 50 µA | All<br>All | 3.0 V | 1, 2, 3 | | 0.1 | V |
| | | | | 4.5 V | | | 0.1 | |
| | | | | 5.5 V | | | 0.1 | |
| | | $V_{IN}$ = $V_{IH}$ minimum or $V_{IL}$ maximum<br>$I_{OL}$ = 12 mA | All<br>All | 3.0 V | 1 | | 0.36 | |
| | | | | | 2, 3 | | 0.5 | |
| | | $V_{IN}$ = $V_{IH}$ minimum or $V_{IL}$ maximum<br>$I_{OL}$ = 24 mA | All<br>All | 4.5 V | 1 | | 0.36 | |
| | | | | | 2, 3 | | 0.5 | |
| | | | | 5.5 V | 1 | | 0.36 | |
| | | | | | 2, 3 | | 0.5 | |
| | | $V_{IN}$ = $V_{IH}$ minimum or $V_{IL}$ maximum<br>$I_{OL}$ = 50 mA | All<br>All | 5.5 V | 1, 2, 3 | | 1.65 | |
| High level input<br>voltage | $V_{IH}$<br>6/ | | All<br>All | 3.0 V | 1, 2, 3 | 2.1 | | V |
| | | | | 4.5 V | | 3.15 | | |
| | | | | 5.5 V | | 3.85 | | |
| Low level input<br>voltage | $V_{IL}$<br>6/ | | All<br>All | 3.0 V | 1, 2, 3 | | 0.9 | V |
| | | | | 4.5 V | | | 1.35 | |
| | | | | 5.5 V | | | 1.65 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ 3/<br>$-55°C \leq T_C \leq +125°C$<br>$+3.0 V \leq V_{CC} \leq +5.5 V$<br>Unless otherwise specified | Device type and Device class | $V_{CC}$ | Group A subgroups | Limits 4/ |  | Unit |
|---|---|---|---|---|---|---|---|---|
|  |  |  |  |  |  | Min | Max |  |
| Input leakage current low 3009 | $I_{IL}$ | $V_{IN}$ = 0.0 V | All<br>All | 5.5 V | 1 |  | -0.1 | µA |
|  |  |  |  |  | 2, 3 |  | -1.0 |  |
| Input leakage current high 3010 | $I_{IH}$ | $V_{IN}$ = 5.5 V | All<br>All | 5.5 V | 1 |  | 0.1 | µA |
|  |  |  |  |  | 2, 3 |  | 1.0 |  |
| Quiescent supply current, output high 3005 | $I_{CCH}$ | $V_{IN} = V_{CC}$ or GND<br>$I_{OUT}$ = 0 A | All<br>All | 5.5 V | 1 |  | 2.0 | µA |
|  |  |  |  |  | 2, 3 |  | 40 |  |
|  |  | M, D, P, L, R, F 7/ | 01<br>Q, V |  | 1 |  | 50 |  |
| Quiescent supply current, output low 3005 | $I_{CCL}$ | $V_{IN} = V_{CC}$ or GND<br>$I_{OUT}$ = 0 A | All<br>All | 5.5 V | 1 |  | 2.0 | µA |
|  |  |  |  |  | 2, 3 |  | 40 |  |
|  |  | M, D, P, L, R, F 7/ | 01<br>Q, V |  | 1 |  | 50 |  |
| Input capacitance 3012 | $C_{IN}$ | See 4.4.1c<br>$T_C$ = +25°C | All<br>All | 5.0 V | 4 |  | 10.0 | pF |
| Power dissipation capacitance | $C_{PD}$ 8/ | See 4.4.1c<br>$T_C$ = +25°C, f = 1 MHz | All<br>All | 5.0 V | 4 |  | 88.0 | pF |
| Functional tests 3014 | 9/ | $V_{IN} = V_{IH}$ or $V_{IL}$<br>Verify output $V_{OUT}$<br>See 4.4.1b | All<br>All | 3.0 V | 7, 8 | L | H |  |
|  |  |  |  | 5.5 V | 7, 8 | L | H |  |
| Propagation delay time, mA or mB to mY 3003 | $t_{PHL}$ 10/ | $C_L$ = 50 pF minimum<br>$R_L$ = 500Ω<br>See figure 4 | 01<br>All | 3.0 V | 9 | 1.0 | 9.5 | ns |
|  |  |  |  |  | 10, 11 | 1.0 | 11.0 |  |
|  |  |  | 02<br>All |  | 9 | 1.0 | 9.8 |  |
|  |  |  |  |  | 10, 11 | 1.0 | 11.9 |  |
|  |  |  | 01<br>All | 4.5 V | 9 | 1.5 | 8.0 |  |
|  |  |  |  |  | 10, 11 | 1.0 | 8.5 |  |
|  |  |  | 02<br>All |  | 9 | 1.0 | 6.5 |  |
|  |  |  |  |  | 10, 11 | 1.0 | 8.1 |  |
|  | $t_{PLH}$ 10/ |  | 01<br>All | 3.0 V | 9 | 1.0 | 9.5 |  |
|  |  |  |  |  | 10, 11 | 1.0 | 11.0 |  |
|  |  |  | 02<br>All |  | 9 | 1.0 | 9.8 |  |
|  |  |  |  |  | 10, 11 | 1.0 | 11.9 |  |
|  |  |  | 01<br>All | 4.5 V | 9 | 1.5 | 8.0 |  |
|  |  |  |  |  | 10, 11 | 1.0 | 8.5 |  |
|  |  |  | 02<br>All |  | 9 | 1.0 | 6.5 |  |
|  |  |  |  |  | 10, 11 | 1.0 | 8.1 |  |

See footnotes on next sheet.

TABLE I. Electrical performance characteristics – Continued.

1/ For tests not listed in the referenced MIL-STD-883, [e.g. $V_{IH}$, $V_{IL}$], utilize the general test procedure under the conditions listed herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except as follows:

a. $V_{IC}$ (pos) tests, the GND terminal can be open. $T_C = +25°C$.
b. $V_{IC}$ (neg) tests, the $V_{CC}$ terminal shall be open. $T_C = +25°C$.
c. All $I_{CC}$ tests, the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

3/ RHA parts for device type 01 meet all levels M, D, P, L, R, and F of irradiation. However, these parts are only tested at the "F" level. Pre and post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, $T_A = 25°C$.

4/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet or exceed the limits specified in table I, as applicable, at $3.0 \text{ V} \leq V_{CC} \leq 3.6 \text{ V}$ and $4.5 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$.

5/ The $V_{OH}$ and $V_{OL}$ tests shall be tested at $V_{CC} = 3.0$ V and 4.5 V. The $V_{OH}$ and $V_{OL}$ tests are guaranteed, if not tested, for other values of $V_{CC}$. Limits shown apply to operation at $V_{CC} = 3.3 \text{ V} \pm 0.3$ V and $V_{CC} = 5.0 \text{ V} \pm 0.5$ V. Tests with input current at +50 mA or -50 mA are performed on only one input at a time with duration not to exceed 2 ms. Transmission driving tests may be performed using $V_{IN} = V_{CC}$ or GND. When $V_{IN} = V_{CC}$ or GND is used, the test is guaranteed for $V_{IN} = V_{IH}$ minimum and $V_{IL}$ maximum.

6/ The $V_{IH}$ and $V_{IL}$ tests are not required if applied as forcing functions for $V_{OH}$ and $V_{OL}$ tests.

7/ The maximum limit for this parameter at 100 krads (Si) is 2 µA.

8/ Power dissipation capacitance ($C_{PD}$) determines both the power consumption ($P_D$) and dynamic current consumption ($I_S$). Where:

$P_D = (C_{PD} + C_L)(V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC})$
$I_S = (C_{PD} + C_L) V_{CC} f + I_{CC}$

f is the frequency of the input signal and $C_L$ is the external output load capacitance.

9/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. Allowable tolerances in accordance with MIL-STD-883 for the input voltage levels may be incorporated. For $V_{OUT}$ measurements, $L \leq 0.3V_{CC}$ and $H \geq 0.7V_{CC}$.

10/ For propagation delay tests, all paths must be tested. AC limits at $V_{CC} = 5.5$ V are equal to the limits at $V_{CC} = 4.5$ V and guaranteed by testing at $V_{CC} = 4.5$ V. AC limits at $V_{CC} = 3.6$ V are equal to limits at $V_{CC} = 3.0$ V and guaranteed by testing at $V_{CC} = 3.0$ V. Minimum ac limits for $V_{CC} = 5.5$ V are 1.0 ns and guaranteed by guardbanding the $V_{CC} = 4.5$ V minimum limits to 1.5 ns.

| Device types | 01 | | 02 | |
|---|---|---|---|---|
| Case outlines | C, D, and X | 2 | E and F | 2 |
| Terminal number | Terminal symbol | | Terminal symbol | |
| 1 | 1A | NC | 1A | NC |
| 2 | 1B | 1A | 1Y | $V_{CC}$ |
| 3 | 1Y | 1B | 2Y | 2B |
| 4 | 2A | 1Y | GND | 2A |
| 5 | 2B | NC | GND | 1B |
| 6 | 2Y | 2A | 3Y | NC |
| 7 | GND | NC | 4Y | 1A |
| 8 | 3Y | 2B | 4B | 1Y |
| 9 | 3A | 2Y | 4A | 2Y |
| 10 | 3B | GND | 3B | GND |
| 11 | 4Y | NC | 3A | NC |
| 12 | 4A | 3Y | $V_{CC}$ | GND |
| 13 | 4B | 3A | $V_{CC}$ | 3Y |
| 14 | $V_{CC}$ | 3B | 2B | 4Y |
| 15 | --- | NC | 2A | 4B |
| 16 | --- | 4Y | 1B | NC |
| 17 | --- | NC | --- | 4A |
| 18 | --- | 4A | --- | 3B |
| 19 | --- | 4B | --- | 3A |
| 20 | --- | $V_{CC}$ | --- | $V_{CC}$ |

NC = No connection

FIGURE 1. Terminal connections.

| Inputs | | Outputs |
|---|---|---|
| mA | mB | mY |
| L | L | H |
| H | L | H |
| L | H | H |
| H | H | L |

H = High voltage level
L = Low voltage level

FIGURE 2. Truth table.

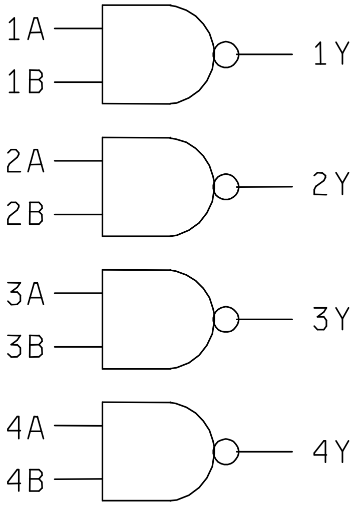
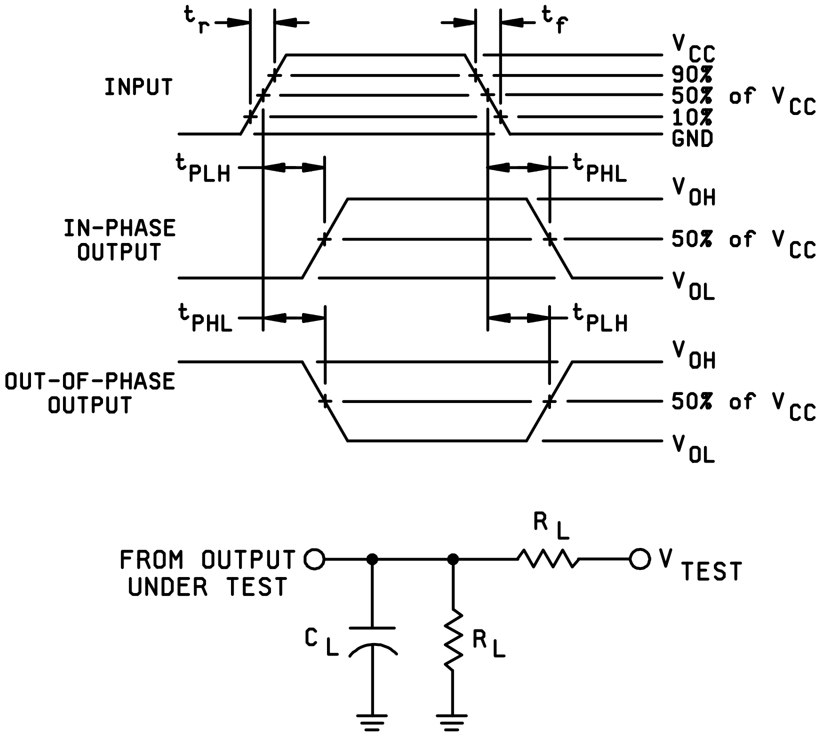


FIGURE 3. Logic diagram.



NOTES:

1. When measuring $t_{PLH}$ and $t_{PHL}$: $V_{TEST}$ = open.
2. $C_L$ = 50 pF or equivalent (includes probe and jig capacitance).
3. $R_L = 500\Omega$ or equivalent.
4. Input signal from pulse generator: $V_{IN}$ = 0.0 V to $V_{CC}$; PRR ≤ 1 MHz; $Z_O = 50\Omega$; $t_r \leq 3.0$ ns; $t_f \leq 3.0$ ns; $t_r$ and $t_f$ shall be measured from 10% of $V_{CC}$ to 90% of $V_{CC}$ and from 90% of $V_{CC}$ to 10% of $V_{CC}$, respectively; duty cycle = 50 percent.
5. Timing parameters shall be tested at a minimum input frequency of 1MHz.
6. The outputs are measured one at a time with one transition per measurement.

FIGURE 4. Switching waveforms and test circuit.

## 4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

  (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

  (2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE II. Electrical test requirements.

| Test requirements | Subgroups (in accordance with MIL-STD-883, method 5005, table I) | Subgroups (in accordance with MIL-PRF-38535, table III) | |
|---|---|---|---|
| | Device class M | Device class Q | Device class V |
| Interim electrical parameters (see 4.2) | - - - | - - - | 1 |
| Final electrical parameters (see 4.2) | 1/ 1, 2, 3, 7, 8, 9 | 1/ 1, 2, 3, 7, 8, 9 | 2/ 3/ 1, 2, 3, 7, 8, 9 |
| Group A test requirements (see 4.4) | 1, 2, 3, 4, 7, 8, 9, 10, 11 | 1, 2, 3, 4, 7, 8, 9, 10, 11 | 1, 2, 3, 4, 7, 8, 9, 10, 11 |
| Group C end-point electrical parameters (see 4.4) | 1, 2, 3 | 1, 2, 3 | 3/ 1, 2, 3, 7,8, 9, 10, 11 |
| Group D end-point electrical parameters (see 4.4) | 1, 2, 3 | 1, 2, 3 | 1, 2, 3 |
| Group E end-point electrical parameters (see 4.4) | 1, 7, 9 | 1, 7, 9 | 1, 7, 9 |

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1, 7, and deltas.
3/ Delta limits as specified in table III shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters.

TABLE III. Burn-in and operating life test Delta parameters (+25°C). 1/

| Parameter 2/ | Symbol | Delta Limits |
|---|---|---|
| Quiescent supply current | $I_{CCH}$, $I_{CCL}$ | ±150 nA |
| Input current low level | $I_{IL}$ | ±20 nA |
| Input current high level | $I_{IH}$ | ±20 nA |
| Output voltage low level ($V_{CC}$ = 5.5 V, $I_{OL}$ = 24 mA) | $V_{OL}$ | ±0.04 V |
| Output voltage high level ($V_{CC}$ = 5.5 V, $I_{OH}$ = -24 mA) | $V_{OH}$ | ±0.2 V |

1/ This table is representation of what vendor CAGE F8859 has experienced and is guaranteed and not meant to be construed as a quality assurance requirement for any other vendor.
2/ These parameters shall be recorded before and after the required burn-in and life tests to determine the delta limits.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. $C_{IN}$ and $C_{PD}$ shall be measured only for initial qualification and after process or design changes which may affect capacitance. $C_{IN}$ shall be measured between the designated terminal and GND at a frequency of 1 MHz. $C_{PD}$ shall be tested in accordance with the latest revision of JEDEC Standard No. 20 and table I herein. For $C_{IN}$ and $C_{PD}$, test all applicable pins on five devices with zero failures.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. $T_A$ = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A$ = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. RHA tests for device classes M, Q, and V for levels M, D, P, L, R, and F shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

d. Prior to irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition A, and as specified herein. Prior to and during total dose irradiation characterization and testing, the devices for characterization shall be biased so that 50 percent are at inputs high and 50 percent are at inputs low, and the devices for testing shall be biased to the worst case condition established during characterization. Devices shall be biased as follows:

a. Inputs tested high, $V_{CC}$ = 5.5 V dc ±5%, $V_{IN}$ = 5.0 V dc +10%, $R_{IN}$ = 1 kΩ ±20%, and all outputs are open.

b. Inputs tested low, $V_{CC}$ = 5.5 V dc ±5%, $V_{IN}$ = 0.0 V dc, $R_{IN}$ = 1 kΩ ±20%, and all outputs are open.

4.4.4.1.1 Accelerated aging test. Accelerated aging shall be performed on classes M, Q, and V devices requiring an RHA level greater than 5K rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

## 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

## 6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

# STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 03-10-01

Approved sources of supply for SMD 5962-87549 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962-8754901CA | 27014<br>01295 | 54AC00DMQB<br>SNJ54AC00J |
| 5962-8754901DA | 27014<br>01295 | 54AC00FMQB<br>SNJ54AC00W |
| 5962-87549012A | 27014<br>01295 | 54AC00LMQB<br>SNJ54AC00FK |
| 5962-8754901XA | 3/ | 54AC00K02Q |
| 5962-8754901XC | 3/ | 54AC00K01Q |
| 5962-8754901VXA | 3/ | 54AC00K02V |
| 5962-8754901VXC | 3/ | 54AC00K01V |
| 5962F8754901XA | F8859 | RHFAC00K02Q |
| 5962F8754901XC | F8859 | RHFAC00K01Q |
| 5962F8754901VXA | F8859 | RHFAC00K02V |
| 5962F8754901VXC | F8859 | RHFAC00K01V |
| 5962-87549022A | 3/ | SNJ54AC11000FK |
| 5962-8754902EA | 3/ | SNJ54AC11000J |
| 5962-8754902FA | 3/ | SNJ54AC11000W |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 27014 | National Semiconductor<br>2900 Semiconductor Drive<br>P.O. Box 58090<br>Santa Clara, CA 95052-8090 |
| F8859 | ST Microelectronics<br>3 rue de Suisse<br>BP4199<br>35041 RENNES cedex2 - FRANCE |
| 01295 | Texas Instruments Incorporated<br>Semiconductor Group<br>8505 Forest Lane<br>P.O. Box 660199<br>Dallas, TX 75243<br>Point of contact: U.S. Highway 75 South<br>P.O. Box 84, M/S 853<br>Sherman, TX 75090-9493 |