



**60A, 500V N-CHANNEL
SUPER-JUNCTION MOSFET**

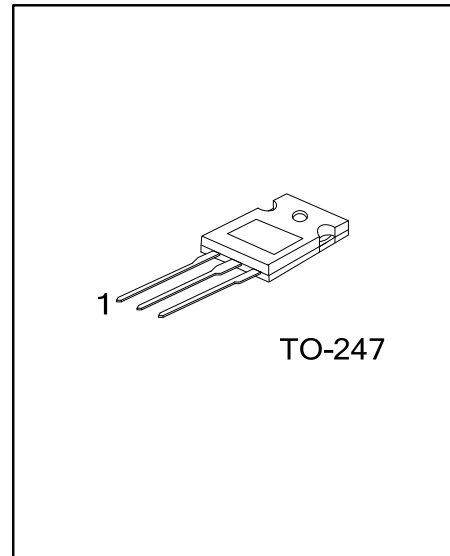
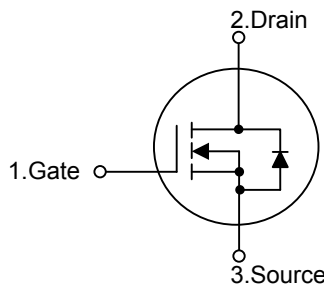
■ **DESCRIPTION**

The **UTC 60NM50** is a Super Junction MOSFET Structure and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and a high rugged avalanche characteristics. This power MOSFET is usually used at DC-DC, AC-DC converters for power applications.

■ **FEATURES**

- * $R_{DS(ON)} < 55m\Omega @ V_{GS}=10V, I_D=30A$
- * High Switching Speed
- * 100% Avalanche Tested

■ **SYMBOL**



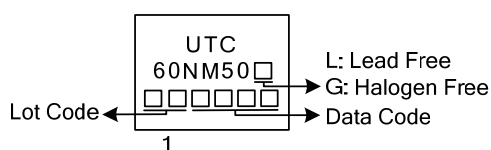
■ **ORDERING INFORMATION**

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
60NM50L-T47-T	60NM50G-T47-T	TO-247	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>60NM50G-T47-T</p>	<p>(1) T: Tube</p> <p>(2) T47: TO-247</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
----------------------	--

■ **MARKING**



■ ABSOLUTE MAXIMUM RATINGS ($T_c=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	500	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous	I_D	60	A
	Pulsed (Note 2)	I_{DM}	240	A
Avalanche Current (Note 2)		I_{AR}	20	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	2400	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	14	V/ns
Power Dissipation		P_D	390	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 12\text{mH}$, $I_{AS} = 20\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq 30\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	0.32	$^\circ\text{C}/\text{W}$

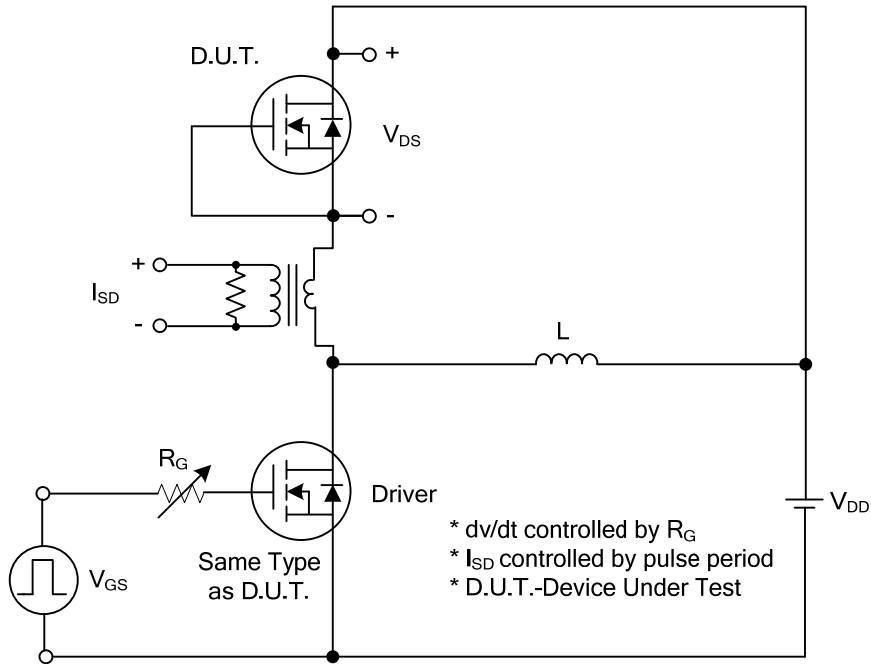
■ ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	500			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=500\text{V}$, $V_{GS}=0\text{V}$			10	μA
Gate- Source Leakage Current	Forward	I_{GSS}			+100	nA
	Reverse				-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.5		4.5	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=30\text{A}$			55	m Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$		4450		pF
Output Capacitance	C_{OSS}			3400		pF
Reverse Transfer Capacitance	C_{RSS}			41		pF
SWITCHING PARAMETERS						
Total Gate Charge (Note 1)	Q_G	$V_{DS}=50\text{V}$, $I_D=1.3\text{A}$, $I_G=100\mu\text{A}$ $V_{GS}=10\text{V}$ (Note 1,2)		498		nC
Gate to Source Charge	Q_{GS}			28		nC
Gate to Drain Charge	Q_{GD}			118		nC
Turn-ON Delay Time (Note 1)	$t_{D(ON)}$	$V_{DD}=30\text{V}$, $I_D=0.5\text{A}$, $R_G=25\Omega$, $V_{GS}=10\text{V}$ (Note 1,2)		176		ns
Rise Time	t_R			600		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			1430		ns
Fall-Time	t_F			1060		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				60	A
Maximum Body-Diode Pulsed Current	I_{SM}				240	A
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	$I_S=30\text{A}$, $V_{GS}=0\text{V}$			1.4	V
Body Diode Reverse Recovery Time (Note 1)	t_{rr}	$I_S=30\text{A}$, $V_{GS}=0\text{V}$, $dI_F/dt=100\text{A}/\mu\text{s}$		600		ns
Body Diode Reverse Recovery Charge	Q_{rr}			12.1		μC

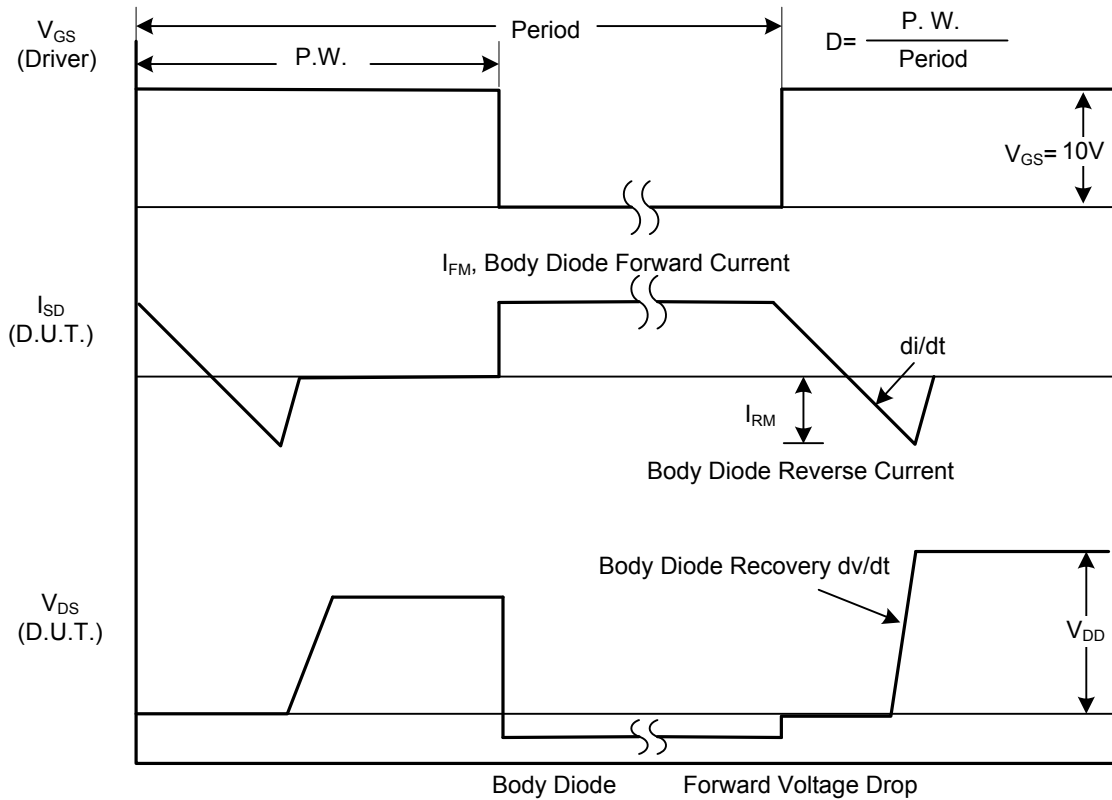
Notes: 1. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating ambient temperature.

■ TEST CIRCUITS AND WAVEFORMS



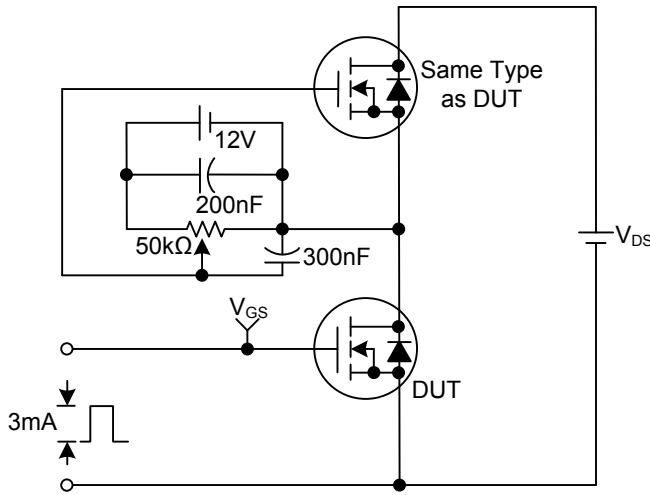
Peak Diode Recovery dv/dt Test Circuit



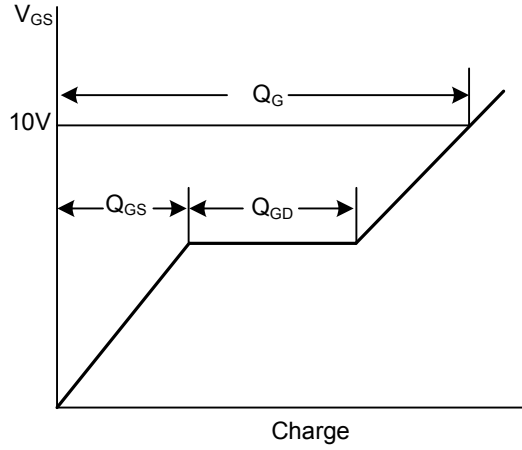
Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

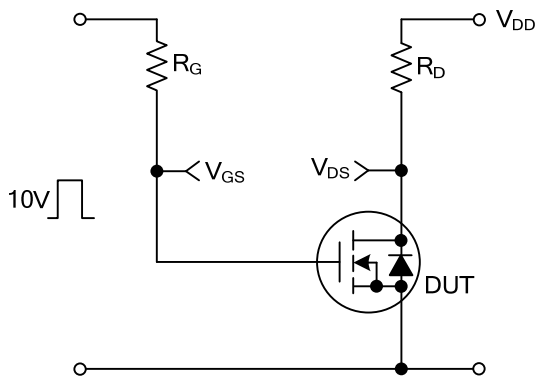
Gate Charge Test Circuit



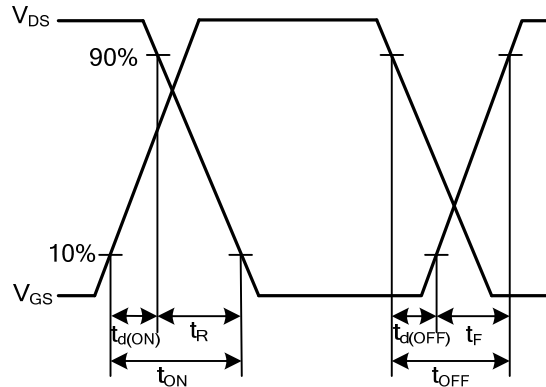
Gate Charge Waveforms



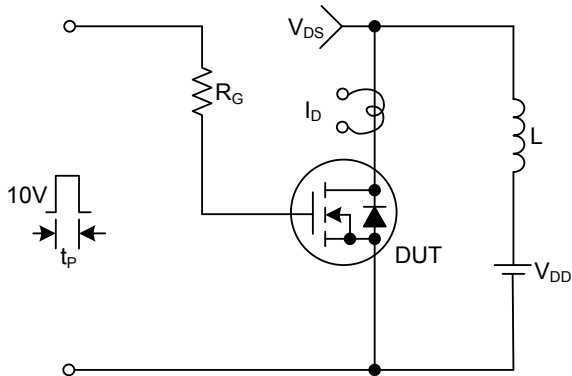
Resistive Switching Test Circuit



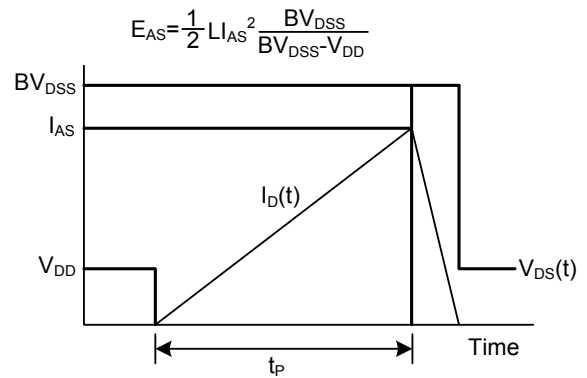
Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms



UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice.