

MPS MICROPROCESSOR WITH I/O

6510 MICROPROCESSOR WITH I/O

DESCRIPTION

The 6510 is a low-cost microcomputer system capable of solving a broad range of small-systems and peripheral-control problems at minimum cost to the user.

An 8-bit Bi-Directional I/O Port is located on-chip with the Output Register at Address 0 0 0 0 and the Data-Direction Register at Address 0 0 0 1. The I/O Port is bit-by-bit programmable.

The Three-State sixteen-bit Address Bus allows Direct Memory Accessing (DMA) and multiprocessor systems sharing a common memory.

The internal processor architecture is identical to the MOS Technology 6502 to provide software compatibility.

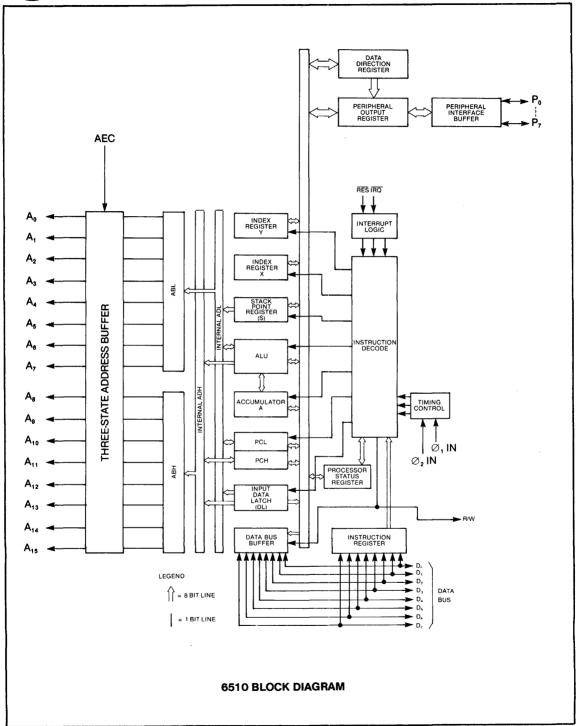
FEATURES OF THE 6510...

- 8-Bit Bi-Directional I/O Port
- Single +5 volt supply
- N channel, silicon gate, depletion load technological
- Eight bit parallel processing
- 56 Instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- 8 Bit Bi-Directional Data Bus
- Addressable memory range of up to 65K bytes
- Direct memory access capability
- Bus compatible with M6800
- · Pipeline architecture
- 1 MHz and 2MHz operation
- Use with any type or speed memory

PIN CONFIGURATION

RES	1		40	Ø ₂ IN
Ø1 IN	2		39	R/W
ĪŔQ	3		38	DB₀
AEC	4		37	DB.
v _{CC}	5		36	DB,
A _n	6		35	DB ₃
Α.	7		34	DB₄
Α,	8		33	DB₃
Α,	9		32	DB,
Α.	10	6510	31	DB,
A٠	11		30	P ₀
A,	12		29	Ρ,
Α.	13		28	P,
A,	14		27	Р,
A۰	15		26	P,
A	16		25	Ρ,
Α.,	17		24	P.
Α.,	18		23	Ρ,
Α.,	19		22	Á.,
VSS	20		21	Α.,







6510 CHARACTERISTICS

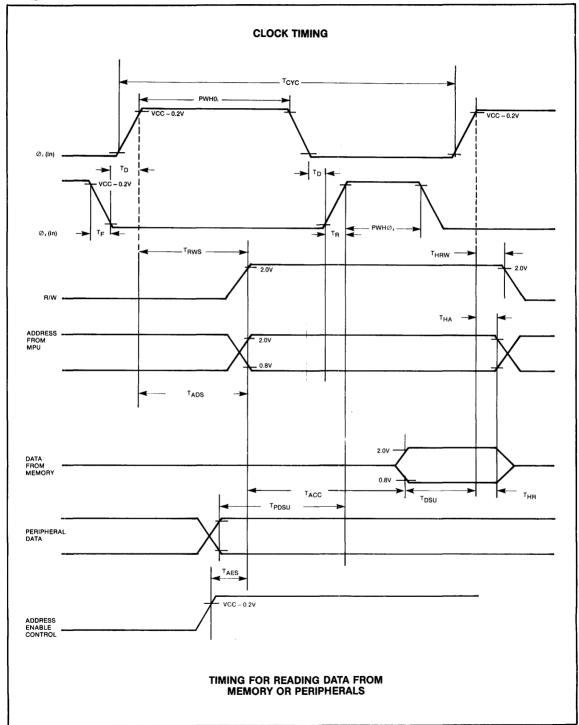
MAXIMUM RATINGS

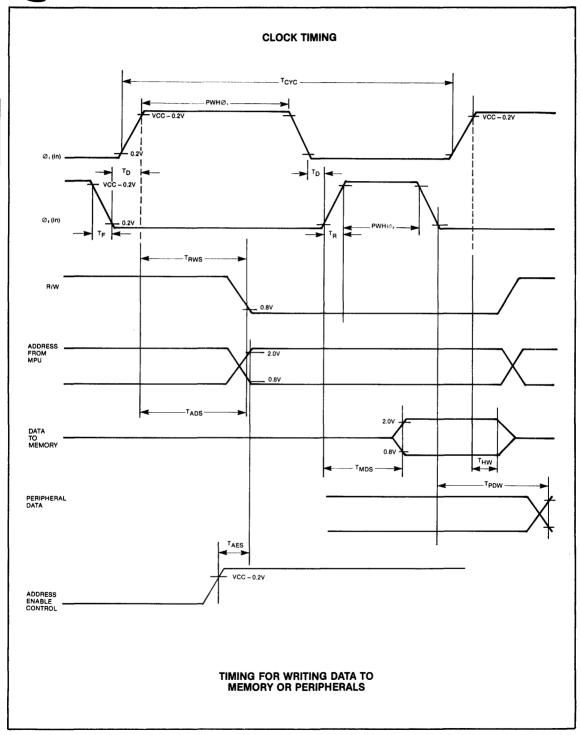
RATING	SYMBOL	VALUE	UNIT
SUPPLY VOLTAGE	Vcc	- 0.3 to + 7.0	Vdc
INPUT VOLTAGE	Vin	- 0.3 to + 7.0	Vdc
OPERATING TEMPERATURE	TA	0 to +70	°C
STORAGE TEMPERATURE	ТSTG	- 55 to + 150	°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 5%, Vss = 0, TA = 0° to + 70°C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input High Voltage					
Ø₁, Ø₂(in)	VIH	Vcc - 0.2	_	Vcc + 1.0V	Vdc
Input High Voltage RES, P ₉ -P,IRQ, Data		Vss + 2.0	_	_	Vdc
Input Low Voltage					
Ø₁, Ø₂(in)	VIL	Vss - 0.3	_	Vss + 0.2	Vdc
RES, P₀-P₁ IRQ, Data		_	_	Vss + 0.8	Vdc
Input Leakage Current (V _{In} = 0 to 5.25V, Vcc = 5.25V) Logic	lin		_	2.5	μΑ
Ø1, Ø2(in)		_	_	100	μΑ
Three State (Off State) Input Current (Vin = 0.4 to 2.4V, Vcc = 5.25V) Data Lines	ITSI	_	_	10	μΑ
Output High Voltage (I _{OH} = -100µAdc, Vcc = 4.75V) Data, AO-A15, R/W, P ₀ -P,	voн	Vss + 2.4	_	-	Vdc
Out Low Voltage (I _{OL} = 1.6mAdc, Vcc = 4.75V) Data, A0-A15, R/W, P ₆ -P,	VOL	_	_	Vss + 0.4	Vdc
Power Supply Current	ICC	_	125		mA
Capacitance V _{In} = O, T _A = 25°C, f = 1MHz)	С				pF
Logic, P ₀ -P ₇	C _{in}	_	_	10	
Data AO-A15, RW	C _{out}		_ _	15 12	
Ø,	c _Ø ,	_	30 50	50 80	
Ø,	C∅,	_	. ~	~	1







AC CHARACTERISTICS

1 MHz TIMING

2 MHz TIMING

ELECTRICAL CHARACTERISTICS (VCC = 5V \pm 5%, VSS = 0V, TA = 0° -70°C) Minimum Clock Frequency = 50 KHz

CLOCK TIMING

Cycle Time	
Clock Pulse Width	Ø1
(Measured at VCC - 0.2V)	Ø2
Fall Time, Rise Time (Measured from 0.2V to VCC	0.2V)
Delay Time between Clocks (Measured at 0.2V)	

SYMBOL	MIN.	TYP.	MAX.
TCYC	1000	_	_
PWHØ1	430	_	_
PWHØ2	470		-
T _F , T _R			25
τ _D	0	_	_

MIN.	TYP.	MAX.	UNITS
500	_	_	ns
215	_	_	ns
235	_	_	ns
_	_	15	ns
0			ns

READ/WRITE TIMING (LOAD = 1TTL)

CHARACTER	ISTIC
Read/Write \$	Setup Time from 6508
Address Set	up Time from 6508
Memory Rea	d Access Time
Data Stabilit	y Time Period
Data Hold T	me-Read
Data Hold T	me-Write
Data Setup	Time from 6510
Address Hol	d Time
R/W Hold Ti	me
Delay Time, Ø2 positive	Address valid to transition
Delay Time, to Periphera	Ø2 negative transition Data valid
Peripheral D	ata Setup Time
Address Ena	ble Setup Time

SYMBOL	MIN.	TYP.	MAX.
TRWS	_	100	300
TADS		100	300
TACC	[- T		575
TDSU	100	_	_
THR			_
THW	10	30	_
TMDS	[150	200
THA	10	30	_
THRW	10	30	_
TAEW	180	_	
T _{PDW}		-	1
T _{PDSU}	300	_	-
TAES			60

MIN.	TYP.	MAX.	UNITS
_	100	150	ns
_	100	150	ns
_	_	300	ns
50			ns
			ns
10	30		ns
_	75	100	ns
10	30		ns
10	30		ns
			ns
		0.5	μS
			ns
		60	ns



SIGNAL DESCRIPTION

Clocks (Ø1, Ø2)

The 6510 requires a two phase non-overlapping clock that runs at the Vcc voltage level.

Address Bus (A.:A..)

The three state outputs are TTL compatible, capable of driving one standard TTL load and 130 pf.

Data Bus (D₀-D₇)

Eight pins are used for the data bus. This is a Bi-Directional bus, transferring data to and from the device and peripherals. The outputs are tri-state buffers capable of driving one standard TTL load and 130 pf.

Reset

This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

After Vcc reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/W signal will become valid.

When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

Interrupt Request (IRQ)

This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses.

Address Enable Control (AEC)

The Address Bus is valid only when the Address Enable Control line is high. When low, the Address Bus is in a high-impedance state. This feature allows easy DMA and multiprocessor systems.

I/O Port (Po-Pz)

Eight pins are used for the peripheral port, which can transfer data to or from peripheral devices. The Output Register is located in RAM at Address 0001, and the Data Direction Register is at Address 0000. The outputs are capable at driving one standard TTL load and 130 pf.

Read/Write (R/W)

This signal is generated by the microprocessor to control the direction of data transfers on the Data Bus. This line is high except when the microprocessor is writing to memory or a peripheral device.



ADDRESSING MODES

ACCUMULATOR ADDRESSING—This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING—In Immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

ABSOLUTE ADDRESSING—In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

ZERO PAGE ADDRESSING—The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

INDEXED ZERO PAGE ADDRESSING—(X, Y indexing)—This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y." The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

INDEXED ABSOLUTE ADDRESSING—(X, Y indexing)—This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X," and "Absolute, Y." The effective address is formed by adding the contents of X and Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

IMPLIED ADDRESSING—In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING—Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is -128 to +127 bytes from the next instruction.

INDEXED INDIRECT ADDRESSING—In indexed indirect addressing (referred to as [Indirect, X]), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

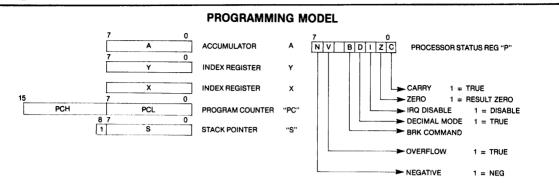
INDIRECT INDEXED ADDRESSING—In indirect indexed addressing (referred to as [Indirect, Y]), the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Yindex register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

ABSOLUTE INDIRECT—The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

INSTRUCTION SET-ALPHABETIC SEQUENCE

	ADC AND ASL	Add Memory to Accumulator with Carry "AND" Memory with Accumulator Shift left One Bit (Memory or Accumulator)	LDA LDX LDY	Load Accumulator with Memory Load Index X with Memory Load Index Y with Memory
	BCC	Branch on Carry Clear	LSR	Shift One Bit Right (Memory or Accumulator)
1	BCS BEQ	Branch on Carry Set Branch on Result Zero	NOP	No Operation
1	BIT BMI	Test Bits in Memory with Accumulator Branch on Result Minus	ORA	"OR" Memory with Accumulator
	BNE	Branch on Result not Zero	PHA	Push Accumulator on Stack
	BPL	Branch on Result Plus	PHP	Push Processor Status on Stack
	BRK	Force Break	PLA	Pull Accumulator from Stack
	BVC BVS	Branch on Overflow Clear Branch on Overflow Set	PLP	Pull Processor Status from Stack
	CLC	01 0 51	ROL	Rotate One Bit Left (Memory or Accumulator)
	CLD	Clear Carry Flag	ROR	Rotate One Bit Right (Memory or Accumulator)
	CLI	Clear Decimal Mode	RTI	Return from Interrupt
	CLV	Clear Interrupt Disable Bit	RTS	Return from Subroutine
	CMP	Clear Overflow Flag		
	CPX	Compare Memory and Accumulator	SBC	Subtract Memory from Accumulator with Borrow
	CPY	Compare Memory and Index X	SEC	Set Carry Flag
,	CPY	Compare Memory and Index Y	SED	Set Decimal Mode
t	DEC	Decrement Memory by One	SEI	Set Interrupt Disable Status
	DEX	Decrement Index X by One	STA	Store Accumulator in Memory
	DEY	Decrement Index Y by One	STX	Store Index X in Memory
E	EOR	"Exclusive-or" Memory with Accumulator	STY	Store Index Y in Memory
	NC	Increment Memory by One	TAX	Transfer Accumulator to Index X
	NX	Increment Index X by One	TAY	Transfer Accumulator to Index Y
	NŶ	Increment Index X by One	TSX	Transfer Stack Pointer to Index X
		•	TXA	Transfer Index X to Accumulator
	JMP	Jump to New Location	TXS	Transfer Index X to Stack Register
J	ISR	Jump to New Location Saving Return Address	TYA	Transfer Index Y to Accumulator



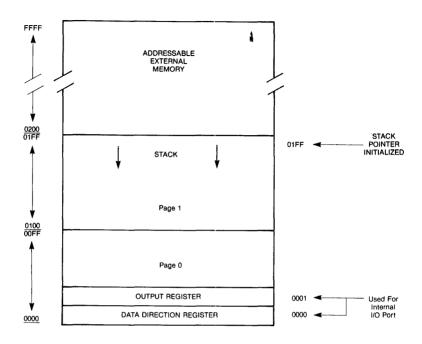


INSTRUCTION SET - OP CODES, Execution Time, Memory Requirements

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Note: Commodore Semiconductor Group cannot assume liability for the use of undefined OP Codes





6510 MEMORY MAP

APPLICATIONS NOTES

Locating the Output Register at the internal I/O Port in Page Zero enhances the powerful Zero Page Addressing instructions of the 6510.

By assigning the I/O Pins as inputs (using the Data Direction Register) the user has the ability to change the contents of address 0001 (the Output Register) using peripheral devices. The ability to change these contents using peripheral inputs, together with Zero Page Indirect Addressing instructions, allows novel and versatile programming techniques not possible earlier.

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