

# 6523 TRI-PORT INTERFACE

## CONCEPT . . .

The 6523 TRI-PORT Interface (TPI) is designed to simplify the implementation of complex I/O operations in microcomputer systems. It has three dedicated 8-bit I/O ports which provide 24 individually programmable I/O lines.

PERIPHERALS

## FEATURES:

- 24 individually programmable I/O lines
- Completely static operation
- Two TTL Drive Capability
- 6 directly addressable registers
- 1 MHz, 2MHz and 3MHz operation

## 6523 REGISTERS

|      |    |                                  |
|------|----|----------------------------------|
| *000 | R0 | PRA — Port Register A            |
| 001  | R1 | PRB — Port Register B            |
| 010  | R2 | PRC — Port Register C            |
| 011  | R3 | DDRA — Data Direction Register A |
| 100  | R4 | DDRB — Data Direction Register B |
| 101  | R5 | DDRC — Data Direction Register   |
| 110  | }  | Illegal States                   |
| 111  |    | Illegal States                   |

\*NOTE: RS2, RS1, RS0 respectively

## ORDER NUMBER:

MXS 6523

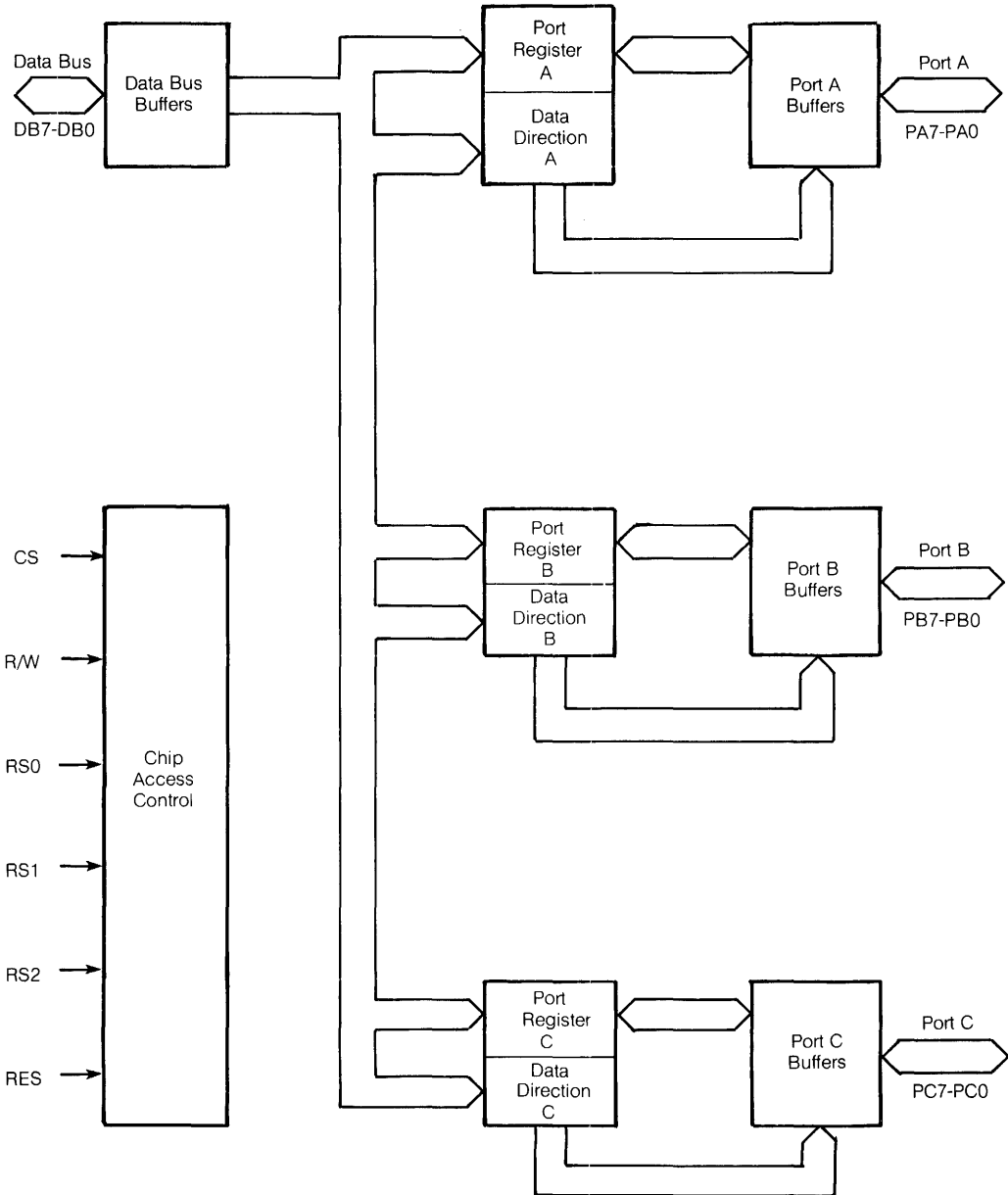
SPEED RANGE  
NO SUFFIX = 450 ns  
A = 225 ns  
B = 165 ns

PACKAGE DESIGNATOR  
C = CERAMIC  
P = PLASTIC

## 6523 PIN CONFIGURATION

|     |    |    |     |
|-----|----|----|-----|
| VSS | 1  | 40 | DB7 |
| PA0 | 2  | 39 | DB6 |
| PA1 | 3  | 38 | DB5 |
| PA2 | 4  | 37 | DB4 |
| PA3 | 5  | 36 | DB3 |
| PA4 | 6  | 35 | DB2 |
| PA5 | 7  | 34 | DB1 |
| PA6 | 8  | 33 | DB0 |
| PA7 | 9  | 32 | PC7 |
| PB0 | 10 | 31 | PC6 |
| PB1 | 11 | 30 | PC5 |
| PB2 | 12 | 29 | PC4 |
| PB3 | 13 | 28 | PC3 |
| PB4 | 14 | 27 | PC2 |
| PB5 | 15 | 26 | PC1 |
| PB6 | 16 | 25 | PC0 |
| PB7 | 17 | 24 | RS0 |
| CS  | 18 | 23 | RS1 |
| R/W | 19 | 22 | RS2 |
| VDD | 20 | 21 | RES |

**6523 INTERNAL ARCHITECTURE**



SOP, DIP, PLCC

**MAXIMUM RATINGS**

|                                 |                |
|---------------------------------|----------------|
| Supply Voltage, $V_{CC}$        | -0.3V to +7.0V |
| Input/Output Voltage, $V_{IH}$  | -0.3V to +7.0V |
| Operating Temperature, $T_{OP}$ | 0°C to 70°C    |
| Storage Temperature, $T_{STG}$  | -55°C to 150°C |

All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

**COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

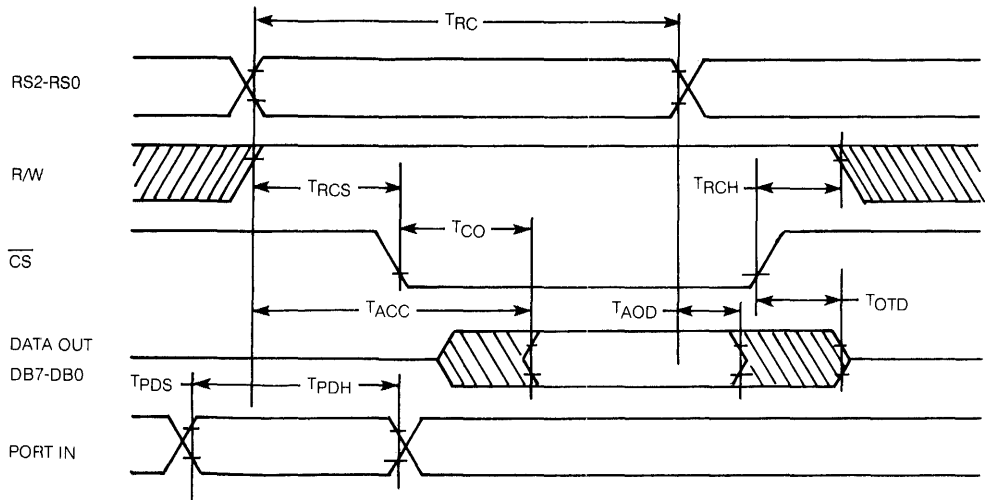
**CHARACTERISTICS ( $V_{CC} = 5.0\text{ V} \pm 5\%$ ,  $V_{SS} = 0\text{V}$ ,  $T_A = 0^\circ$  to  $70^\circ\text{C}$ )**

| CHARACTERISTIC   | SYMBOL    | MIN      | TYP       | MAX       | UNIT          |
|--|-----------|----------|-----------|-----------|---------------|
| Input High Voltage (Normal Operating Levels)   | $V_{IH}$  | + 2.0    |           | $V_{CC}$  | V             |
| Input Low Voltage (Normal Operating Levels)  | $V_{IL}$  | -0.3     |           | +0.8      | V             |
| Input Leakage Current<br>$V_{in} = 0$ to $5.0\text{ V}$<br>WRITE, RES, CS, RS2-RS0   | $I_{IN}$  | 0        | $\pm 1.0$ | $\pm 2.5$ | $\mu\text{A}$ |
| Three-State (Off State) Input Current<br>( $V_{in} = 0.4$ to $2.4\text{ V}$ , $V_{CC} = \text{max}$ )<br>D0-D7, PA0-PA7, PB0-PB7, PC0-PC7                      | $I_{TSI}$ | 0        | $\pm 2.0$ | $\pm 10$  | $\mu\text{A}$ |
| Output High Voltage<br>( $V_{CC} = \text{min}$ , Load = $200\ \mu\text{A}$ )   | $V_{OH}$  | 2.4      | 3.5       | $V_{CC}$  | V             |
| Output Low Voltage<br>( $V_{CC} = \text{min}$ , Load = $3.2\text{ mA}$ )   | $V_{OL}$  | $V_{SS}$ | 0.2       | 0.4       | V             |
| Output High Current (Sourcing)<br>( $V_{OH} = 2.4\text{ V}$ )  | $I_{OH}$  | -200     | -1000     | —         | $\mu\text{A}$ |
| Output Low Current (Sinking)<br>( $V_{OL} = 0.4\text{ V}$ )  | $I_{OL}$  | 3.2      | —         | —         | mA            |
| Supply Current   | $I_{CC}$  | —        | 50        | 100       | mA            |
| Input Capacitance<br>( $V_{in} = 0\text{V}$ , $T_A = 25^\circ\text{C}$ , $f = 1.0\text{ MHz}$ )<br>D0-D7, PA0-PA7, PB0-PB7, PC0-PC7<br>WRITE, RES, RS2-RS0, CS | $C_{in}$  | —        | 7         | 10        | pF            |
| Output Capacitance<br>( $V_{in} = 0\text{V}$ , $T_A = 25^\circ\text{C}$ , $f = 1.0\text{ MHz}$ )   | $C_{out}$ | —        | 7         | 10        | pF            |

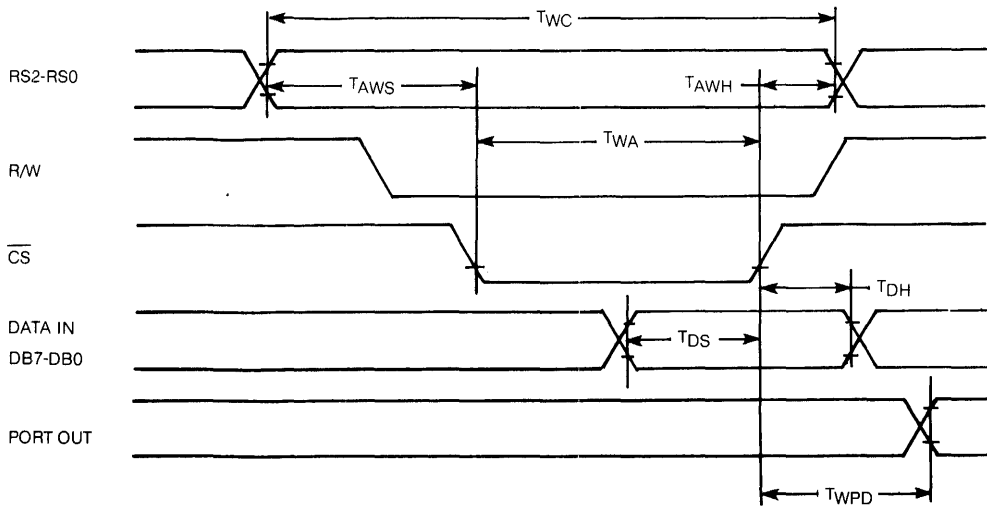
Note: Negative sign indicates outward current flow, positive indicates inward flow.



## READ CYCLE



## WRITE CYCLE



Note: All timings referenced to  $V_{ILmax}$ ,  $V_{IHmin}$  on inputs and  $V_{OLmax}$ ,  $V_{OHmin}$  on outputs.

**READ CYCLE TIMING**

| SYMBOL           | CHARACTERISTIC                      | 6523 |     | 6523A |     | 6523B |     | UNITS |
|------------------|-------------------------------------|------|-----|-------|-----|-------|-----|-------|
|                  |                                     | MIN  | MAX | MIN   | MAX | MIN   | MAX |       |
| T <sub>RC</sub>  | Read Cycle                          | 450  | —   | 225   | —   | 165   | —   | ns    |
| T <sub>ACC</sub> | Access Time <sup>1</sup>            | —    | 450 | —     | 225 | —     | 165 | ns    |
| T <sub>CO</sub>  | $\overline{CS}$ to Output Valid     | —    | 270 | —     | 120 | —     | 70  | ns    |
| T <sub>RCS</sub> | R/W high to $\overline{CS}$ Setup   | 0    | —   | 0     | —   | 0     | —   | ns    |
| T <sub>RCH</sub> | R/W high to $\overline{CS}$ Hold    | 0    | —   | 0     | —   | 0     | —   | ns    |
| T <sub>OTD</sub> | $\overline{CS}$ to Output Off Delay | 20   | 120 | 20    | 120 | 20    | 120 | ns    |
| T <sub>AOD</sub> | Address to Output Delay             | 50   | —   | 50    | —   | 50    | —   | ns    |
| T <sub>PDS</sub> | Port Input Setup                    | 120  | —   | 60    | —   | 40    | —   | ns    |
| T <sub>PDH</sub> | Port Input Hold                     | 150  | —   | 150   | —   | 150   | —   | ns    |

Note 1: Access Time measured from later of  $\overline{WRITE}$  high or RS stable.

**WRITE CYCLE TIMING**

| SYMBOL           | CHARACTERISTIC                 | 6523 |      | 6523A |     | 6523B |     | UNITS |
|------------------|--------------------------------|------|------|-------|-----|-------|-----|-------|
|                  |                                | MIN  | MAX  | MIN   | MAX | MIN   | MAX |       |
| T <sub>WC</sub>  | Write Cycle                    | 450  | —    | 225   | —   | 165   | —   | ns    |
| T <sub>WA</sub>  | Write Active Time <sup>2</sup> | 420  | —    | 200   | —   | 150   | —   | ns    |
| T <sub>AWS</sub> | Address to R/W low Setup       | 0    | —    | 0     | —   | 0     | —   | ns    |
| T <sub>AWH</sub> | Address to R/W low Hold        | 0    | —    | 0     | —   | 0     | —   | ns    |
| T <sub>DS</sub>  | Data bus in Setup              | 150  | —    | 100   | —   | 50    | —   | ns    |
| T <sub>DH</sub>  | Data bus in Hold               | 0    | —    | 0     | —   | 0     | —   | ns    |
| T <sub>WPD</sub> | Write active to Port out Delay | —    | 1000 | —     | 500 | —     | 330 | ns    |

Note 2: T<sub>WA</sub> is the time while both  $\overline{CS}$  and R/W are low.

### 6523 FUNCTIONAL DESCRIPTION

Three 8 bit bi-directional ports (A, B, C) are available on the 6523. Each port has two associated read/write registers:

#### Data Direction Registers (DDRA, DDRB, DDRC)

Each bit of the data direction registers controls the corresponding pin of the associated port as follows:

| DDR bit | Direction of port pin          |
|---------|--------------------------------|
| 0       | Input (Output driver disabled) |
| 1       | Output (Output driver enabled) |

#### Port Registers (PRA, PRB, PRC)

Reading the Port Register returns the logic states of the associated port pins. The pin voltage levels must meet the  $V_{IH}$  and  $V_{IL}$  specification limits to ensure valid data. (Excessive loading of the output driver may cause the data read to differ from the expected output.) If the port pin is programmed as an output by the DDR, the output driver is set to the last data written to the corresponding PR bit.

### 6523 INTERFACE SIGNALS

#### $\overline{CS}$ — Chip Select Input

The  $\overline{CS}$  input controls the activity of the 6523. A low level on  $\overline{CS}$  causes the device to respond to signals on the R/W and address (RS) lines. A high on  $\overline{CS}$  prevents these lines from controlling the 6523. The  $\overline{CS}$  line is normally activated (low) by the appropriate address combination from the processor.

#### R/W — Read/Write Input

The R/W signal is normally supplied by the microprocessor and controls the direction of data transfers of the 6523. A high on R/W indicates a read (data transfer out of the 6523), while a low indicates a write (data transfer into the 6523).

#### RS<sub>2</sub>-RS<sub>0</sub> — Address Inputs

The address inputs select the internal registers (in conjunction with  $\overline{CS}$  and R/W) as indicated by the register table.

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**DB7-DB0 — Data Bus Inputs/Outputs**

The eight data bus pins transfer information between the 6523 and the system data bus. These pins are high impedance inputs unless CS is low and R/W is high, to read the device. During this read, the data bus output buffers are enabled, driving the data from the selected register onto the system data bus.

 **$\overline{\text{RES}}$  — Reset Input**

A low on the RES pin clears internal registers. This sets all three ports as inputs (floating), preventing any conflicts on the bi-directional port lines. For port pins to be used as outputs, the desired output data may be written to the port register before enabling the output driver. This sequence can eliminate undesired output conditions when the outputs are enabled via the DDR.

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