commodore semiconductor group

NMOS

MPS
6529
SINGLE-PORT
INTERFACE

6529 SINGLE PORT INTERFACE

PERIPHERALS

DESCRIPTION

The 6529 is a static microprocessor compatible, 8-bit I/O Port with passive output pull-up devices. Data is written to the port when $\overline{CS}$ and R/W are low. Data is read from the port when $\overline{CS}$ is low and R/W is high. The passive output pull-ups allow a single bit to act as either an input or an output without I/O mode switching.

This device is provided with special circuitry to provide power-on reset. Under normal fast power-on conditions the outputs will initialize in the input high impedance state. With very slow or noisy power-up, there is some possibility the device will initialize with outputs driven low. It is recommended that the 6529 be interfaced to open collector output type devices.

TRUTH TABLE

CS	R/W	D_0-D_7
L	L	DATA BUS TO PORT
L	H	PORT TO DATA BUS
H	X	ISOLATION

L = LOW Level
H = HIGH Level
X = Irrelevant

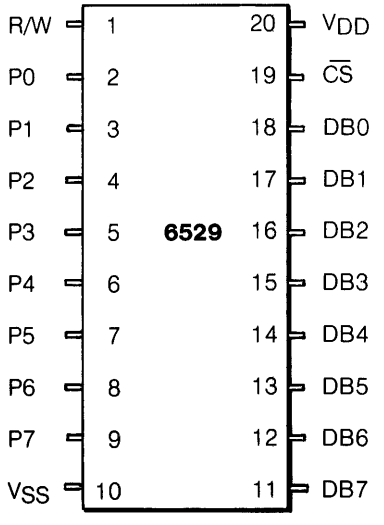
ORDER INFORMATION

MXS 6529 ___

FREQUENCY RANGE
NO SUFFIX = 1 MHz
A = 2 MHz
B = 3 MHz

PACKAGE DESIGNATOR
C = Ceramic
P = Plastic

PIN CONFIGURATION



MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
SUPPLY VOLTAGE	V_{CC}	−0.3 to +7.0	Vdc
INPUT VOLTAGE	V_{in}	−0.3 to +7.0	Vdc
OPERATING TEMPERATURE RANGE	T_A	0 to + 70	°C
STORAGE TEMPERATURE RANGE	T_{stg}	−55 to +150	°C

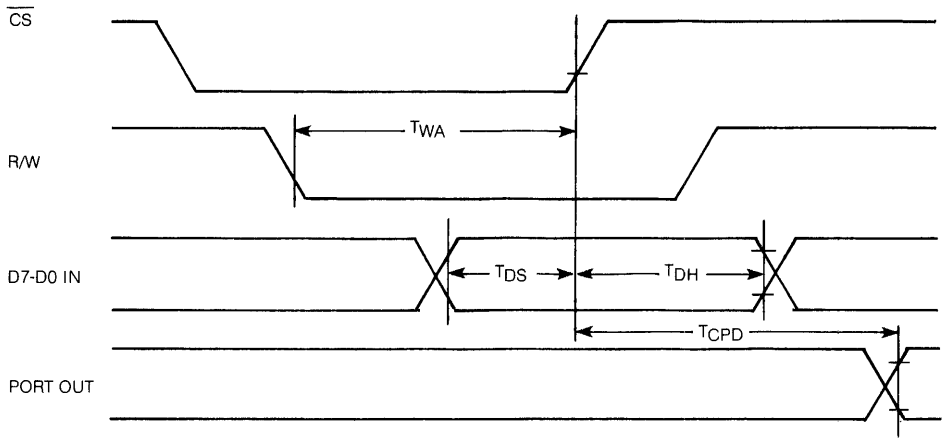
This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

CHARACTERISTICS (V_{CC} = 5.0V ± 5%, V_{SS} = 0V, T_A = 0° to 70°C)

CHARACTERISTIC	SYMBOL	MIN	MAX	UNIT
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.0	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)	V_{IL}	−0.3	+0.8	Vdc
Input Leakage Current V_{in} = 0 to 5.0Vdc $\overline{WRITE}$, $\overline{CS}$	I_{IN}	—	±2.5	μAdc
Three-State (Off State Input Current) (V_{in} = 0.4 to 2.4 Vdc, V_{CC} = Max) D_0-D_7	I_{TSI}	—	±10	μAdc
Output High Voltage (V_{CC} = Min, Load = −600μAdc, P_0-P_7) (V_{CC} = Min, Load = −200μAdc, D_0D_7)	V_{OH}	2.4	—	Vdc
Output Low Voltage (V_{CC} = Max, Load = 6.4mAdc, P_0-P_7) (V_{CC} = Max, Load = 3.2mA, D_0-D_7)	V_{OL}	—	+0.4	Vdc
Output High Current (Sourcing) P_0-P_7 (V_{OH} = 2.4 Vdc) D_0-D_7	I_{OH} I_{OH}	−600 −200	−	μAdc μAdc
Output Low Current (Sinking) P_0-P_7 (V_{OL} = 0.4 Vdc) D_0-D_7	I_{OL} I_{OL}	6.4 3.2	−	mAdc mAdc
Supply Current	I_{CC}	−	80	mA

NOTE: Negative sign indicates outward current flow, positive indicates inward flow.

6529 WRITE CYCLE TIMING DIAGRAM



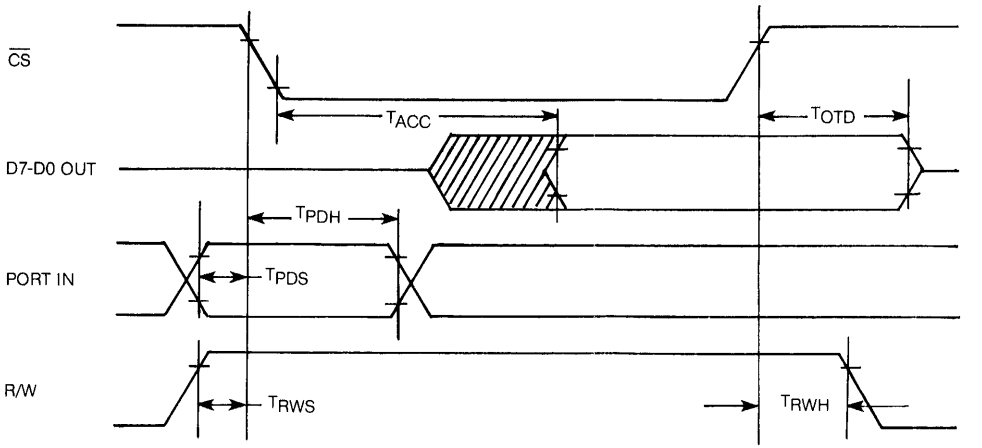
Note: All timings referred to V_{IL}max, V_{IH} min for inputs and V_{OL} max, V_{OH} min for outputs.

6529 WRITE CYCLE CHARACTERISTICS

Symbol	Characteristic	1 MHz		2 MHz		3 MHz		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
T_{WA}*	Write Active	450	—	225	—	160	—	ns
T_{CPD}	$\overline{CS}$ to Port Out Delay	—	1000	—	500	—	330	ns
T_{DS}	Data to $\overline{CS}$ Setup	150	—	100	—	100	—	ns
T_{DH}	Data to $\overline{CS}$ Hold	0	—	0	—	0	—	ns

*T_{WA} is the time while both $\overline{CS}$ and R/W are low

6529 READ CYCLE DIAGRAM



Note: All timings referenced to V_{IL} max, V_{IH} min for inputs and V_{OL} max, V_{OH} min for outputs.

6529 READ CYCLE CHARACTERISTICS

Symbol	Characteristic	1 MHz		2 MHz		3 MHz		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
T_{ACC}	Access Time	—	450	—	225	—	160	ns
T_{PDS}	Port Input Setup	120	—	60	—	40	—	ns
T_{PDH}	Port Input Hold	30	—	30	—	30	—	ns
T_{RCS}	R/W to $\overline{CS}$ Setup	0	—	0	—	0	—	ns
T_{RCH}	R/W to $\overline{CS}$ Setup	0	—	0	—	0	—	ns
T_{OTD}	$\overline{CS}$ to Output Off Delay	20	120	20	120	20	120	ns