commodore semiconductor group

NMOS

MPS

6545-1

CRT CONTROLLER (CRTC)

6545-1 CRT Controller (CRTC)

CONCEPT

The 6545-1 is a CRT Controller intended to provide capability for interfacing the 6500/6800 microprocessor families to CRT or TV-type raster scan displays. A unique feature is the inclusion of several modes of operation, so that the system designer can configure the system with a wide assortment of techniques.

FEATURES:

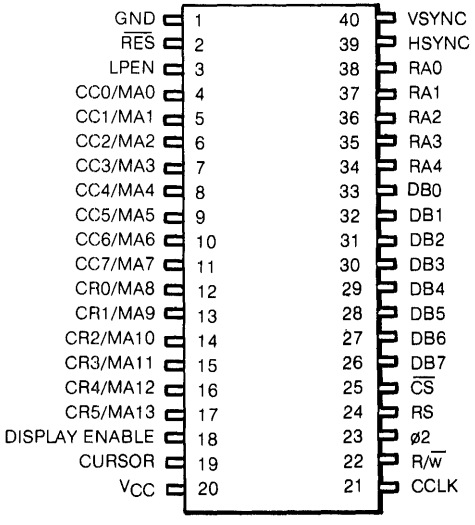
- Single +5 volt (±5%) power supply.
- Alphanumeric and limited graphics capabilities.
- Fully programmable display (rows, columns, blanking, etc.).
- Non-interlaced scan.
- 50/60 Hz operation.
- Fully programmable cursor.
- External light pen capability.
- Capable of addressing up to 16K character video display RAM.
- No DMA required.
- Pin-compatible with MC6845.
- Row/Column or straight-binary addressing for video display RAM.
- Internal 8-bit status register.

ORDERING INFORMATION

MXS 6545-1 1 MHz
MXS 6545A-1 2 MHz

PACKAGE DESIGNATOR
C = CERAMIC
P = PLASTIC

6545-1 PIN DESIGNATION



MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.3V to +7.0V
Input/Output Voltage, V_{IN}	−0.3V to +7.0V
Operating Temperature, T_{OP}	0°C to 70°C
Storage Temperature, T_{STG}	−55°C to 150°C

All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

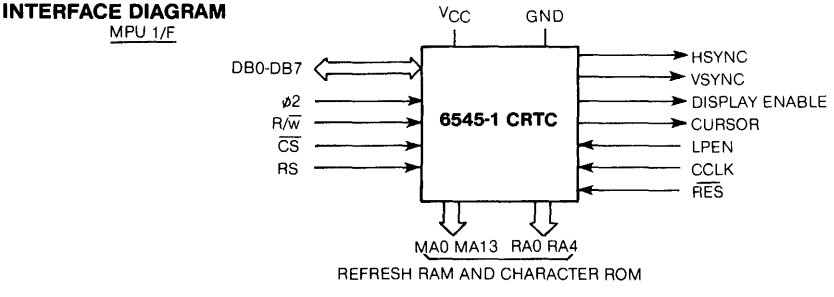
COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

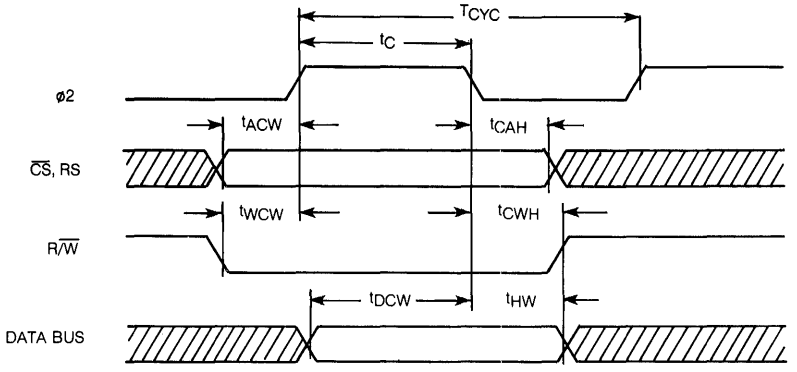
Symbol	Characteristic	Min.	Max.	Unit
V_{IH}	Input High Voltage	2.0	V_{CC}	V
V_{IL}	Input Low Voltage	−0.3	0.8	V
I_{IN}	Input Leakage (ø2, R/$\overline{w}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK)	—	2.5	µA
I_{TSI}	Three-State Input Leakage (DB0-DB7) V_{IN} = 0.4 to 2.4V	—	10.0	µA
V_{OH}	Output High Voltage I_{LOAD} = 205µA (DB0-DB7) I_{LOAD} = 100µA (all others)	2.4	V_{CC}	V
V_{OL}	Output Low Voltage I_{LOAD} = 1.6mA	V_{SS}	0.4	V
P_D	Power Dissipation	—	1000	mW
C_{IN}	Input Capacitance ø2, R/$\overline{w}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK DB0-DB7	— —	10.0 12.5	pF pF
C_{OUT}	Output Capacitance	—	10.0	pF

INTERFACE DIAGRAM



MPU BUS INTERFACE CHARACTERISTICS

WRITE CYCLE



WRITE TIMING CHARACTERISTICS

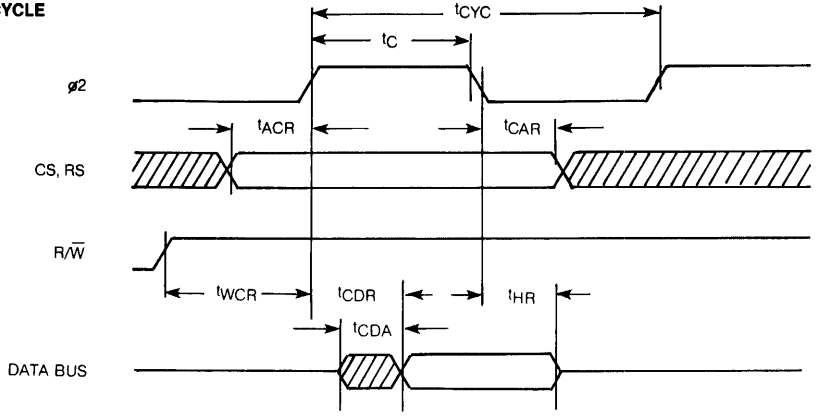
(V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

Symbol	Characteristic	6545-1		6545A-1		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	40	0.5	40	µs
t_C	ø2 Pulse Width	470	—	235	—	ns
t_{ACW}	Address Set-Up Time	180	—	90	—	ns
t_{CAH}	Address Hold Time	0	—	0	—	ns
t_{WCW}	R/$\overline{W}$ Set-Up Time	180	—	90	—	ns
t_{CWH}	R/$\overline{W}$ Hold Time	0	—	0	—	ns
t_{DCW}	Data Bus Set-Up Time	265	—	100	—	ns
t_{HW}	Data Bus Hold Time	10	—	10	—	ns

(t_r and t_f = 10 to 30 ns)

MPU BUS INTERFACE CHARACTERISTICS

READ CYCLE



READ TIMING CHARACTERISTICS

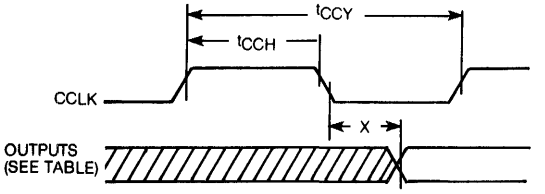
(V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

Symbol	Characteristic	6545-1		6545A-1		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	40	0.5	40	µs
t_C	ø2 Pulse Width	470	—	235	—	ns
t_{ACR}	Address Set-Up Time	180	—	90	—	ns
t_{CAR}	Address Hold Time	0	—	0	—	ns
t_{WCR}	R/$\overline{w}$ Set-Up Time	180	—	90	—	ns
t_{CDR}	Read Access Time	—	340	—	150	ns
t_{HR}	Read Hold Time	10	—	10	—	ns
t_{CDA}	Data Bus Active Time (Invalid Data)	40	—	40	—	ns

(t_r and t_f = 10 to 30 ns)

MEMORY AND VIDEO INTERFACE CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)



SYSTEM TIMING

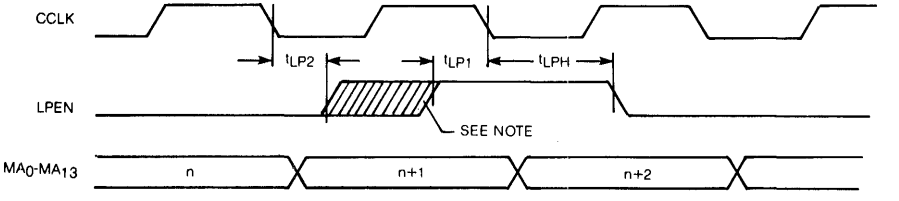
Output	Parameter
MA0-MA13	t_{MAD}
RA0-RA4	t_{RAD}
DISPLAY-ENABLE	t_{DTD}
HSYNC	t_{HSD}
VSYNC	t_{VSD}
CURSOR	t_{CDD}

SYSTEM TIMING PARAMETERS (V_{CC} = 5.0V + 5%, T_A = 0 to 70°C, unless otherwise noted)

Symbol	Characteristics	6545-1		6545A-1		Unit
		Min.	Max.	Min.	Max.	
t_{CCY}	Character Clock Cycle Time	0.40	40	0.40	40	µs
t_{CCH}	Character Clock Pulse Width	200	—	200	—	ns
t_{MAD}	MA0-MA13 Propagation Delay	—	300	—	300	ns
t_{RAD}	RA0-RA4 Propagation Delay	—	300	—	300	ns
t_{DTD}	DISPLAY ENABLE Propagation Delay	—	375	—	375	ns
t_{HSD}	HSYNC Propagation Delay	—	375	—	375	ns
t_{VSD}	VSYNC Propagation Delay	—	375	—	375	ns
t_{CDD}	CURSOR Propagation Delay	—	375	—	375	ns
t_{LPH}	LPEN Hold Time	100	—	100	—	ns
t_{LP1}	LPEN Set-up Time	20	—	20	—	ns
t_{LP2}	CCLK to LPEN Delay	0	—	0	—	ns

t_r, t_f = 20 ns (max)

LIGHT PEN STROBE TIMING DEFINITIONS



NOTE: "Safe" time position for LPEN positive edge to cause address n+2 to load into Light Pen Register. t_{LP2} and t_{LP1} are time positions causing uncertain results.

MPU INTERFACE SIGNAL DESCRIPTION

ø2 (Clock)

The input clock is the system ø2 clock and is used to trigger all data transfers between the system microprocessor and the 6545-1.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ signal is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the 6545-1; a low on the R/$\overline{W}$ pin allows a write to the 6545-1.

$\overline{CS}$ (Chip Select)

The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The 6545-1 is selected when $\overline{CS}$ is low.

RS (Register Select)

The Register Select input is used to access internal registers. A low on this pin permits writes into the Address Register and reads from the Status Register. The contents of the Address Register is the identity of the register accessed when RS is high.

DB_0-DB_7 (Data Bus)

The DB_0-DB_7 pins are the eight data lines used for transfer of data between the processor and the 6545-1. These lines are bi-directional and are normally high-impedance except during read cycles when the chip is selected.

VIDEO INTERFACE SIGNAL DESCRIPTION

HSYNC (Horizontal Sync)

The HSYNC signal is an active-high output used to determine the horizontal position of displayed text. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)

The VSYNC signal is an active-high output used to determine the vertical position of displayed text. Like HSYNC, VSYNC may be used to drive a CRT monitor or composite video generation circuits. VSYNC position and width are both fully programmable.

DISPLAY ENABLE

The DISPLAY ENABLE signal is an active-high output and is used to indicate when the 6545-1 is generating active display information. The number of horizontal displayed characters and the number of vertical displayed characters are both fully programmable and together are used to generate the DISPLAY ENABLE signal. Display Enable can be delayed by one character time by setting bit 4 of R8 to a "1".

CURSOR

The CURSOR signal is an active-high output and is used to indicate when the scan coincides with the programmed cursor position. The cursor position may be programmed to be any character in the address field. Furthermore, within the character, the cursor may be programmed to be any block of scan lines, since the start scan line and the end scan line are both programmable. The CURSOR position may be delayed by one character time by setting bit 5 of R8 to a "1."

LPEN

The LPEN signal is an edge-sensitive input and is used to load the internal Light Pen Register with the contents of the Refresh Scan Counter at the time the active edge occurs. The active edge of LPEN is the low-to-high transition.

CCLK

The CCLK signal is the character timing clock input and is used as the time base for all internal count/control functions.

$\overline{RES}$

The $\overline{RES}$ signal is an active-low input used to initialize all internal scan counter circuits. When $\overline{RES}$ is low, all internal counters are stopped and cleared, all scan and video outputs are low, and control registers are unaffected. $\overline{RES}$ must stay low for at least one CCLK period. All scan timing is initiated when $\overline{RES}$ goes high. In this way, $\overline{RES}$ can be used to synchronize display frame timing with line frequency.

MEMORY ADDRESS SIGNAL DESCRIPTION

MA0-MA13 (Refresh RAM Address Lines)

These signals are active-high outputs and are used to address the Refresh RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

There are two selectable address modes for MA0-MA13:

In the *straight binary* mode, characters are stored in successive memory locations. Thus, the software must be designed so that row and column character co-ordinates are translated into sequentially-numbered addresses. In the *row/column* mode MA0-MA7 become column addresses CC0-CC7 and MA8-MA13 become row addresses CR0-CR5. In this case, the software can manipulate characters in terms of row and column locations, but additional address compression circuits are needed to convert the CC0-CC7 and CR0-CR5 addresses into a memory efficient binary address scheme.

RA0-RA4 (Raster Address Lines)

These signals are active-high outputs and are used to select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

DESCRIPTION OF INTERNAL REGISTERS

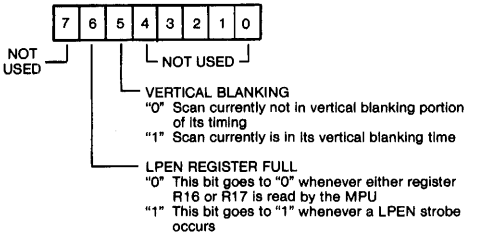
Figure 1 illustrates the format of a typical video display and is necessary to understand the functions of the various 6545-1 internal registers. Figure 2 illustrates vertical and horizontal timing. Figure 3 summarizes the internal registers and indicates their address selection and read/write capabilities.

Address Register

This is a 5-bit register which is used as a "pointer" to direct 6545-1 data transfers to and from the system MPU. Its contents is the number of the desired register (0-31). When RS is low, then this register may be loaded; when RS is high, then the register selected is the one whose identity is stored in this register.

Status Register

This register is used to monitor the status of the CRTC, as follows:



Horizontal Total (R0)

This 8-bit register contains the total of displayed and non-displayed characters, minus one, per horizontal line. The frequency of HSYNC is thus determined by this register.

Horizontal Displayed (R1)

This 8-bit register contains the number of displayed characters per horizontal line.

Horizontal Sync Position (R2)

This 8-bit register contains the position of the HSYNC on the horizontal line, in terms of the character location number on the line. The position of the HSYNC determines the left-to-right location of the displayed text on the video screen. In this way, the side margins are adjusted.

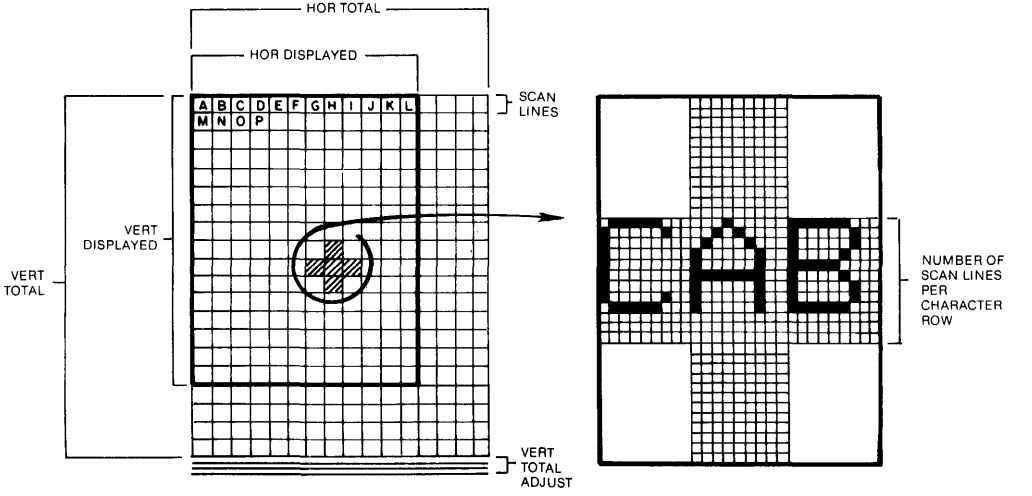


Figure 1. Video Display Format

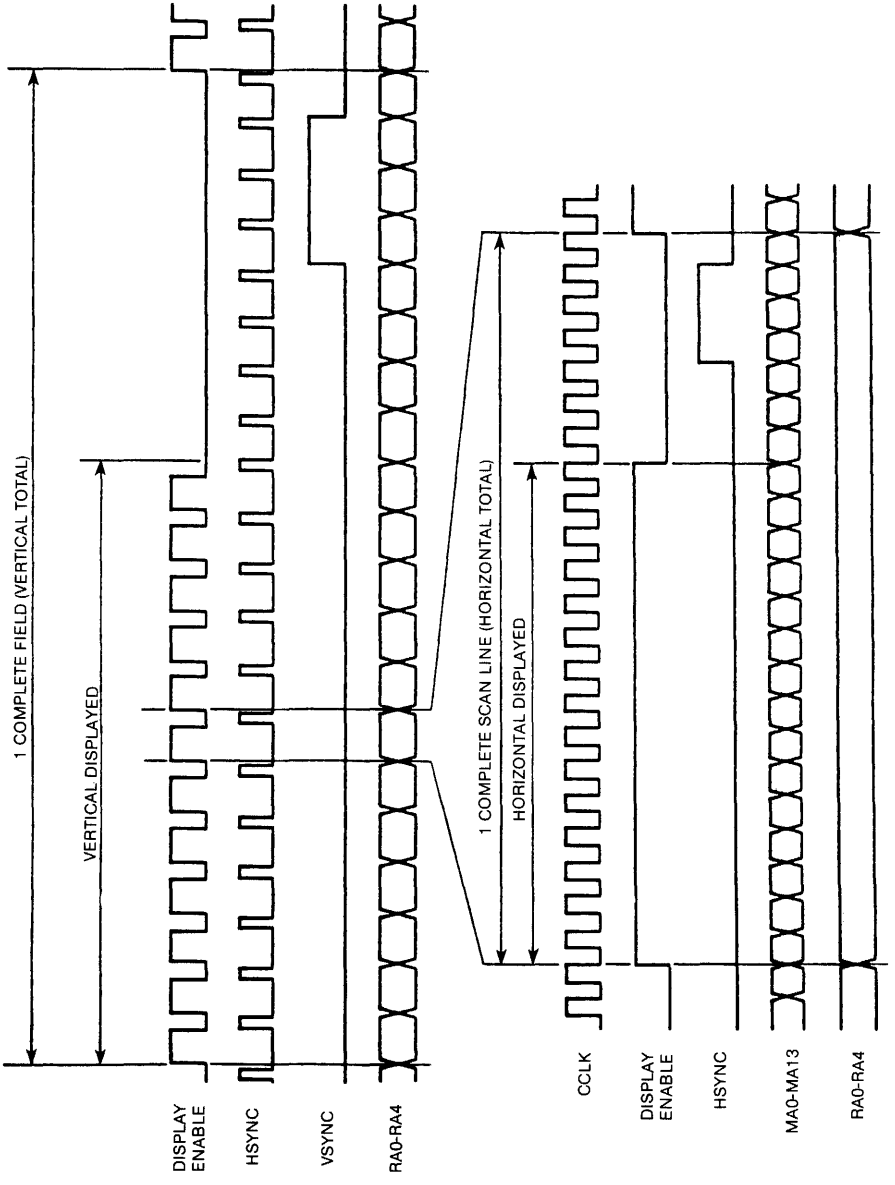
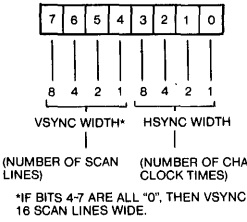


Figure 2. Vertical and Horizontal Timing

Horizontal and Vertical SYNC Widths (R3)

This 8-bit register contains the widths of both HSYNC and VSYNC, as follows:



Control of these parameters allows the 6545-1 to be interfaced to a variety of CRT monitors, since the HSYNC and VSYNC timing signals may be accommodated without the use of external one-shot timing.

Vertical Total (R4)

The Vertical Total Register is a 7-bit register containing the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency, then $\overline{RES}$ may be used to provide absolute synchronism.

$\overline{CS}$	RS	Address Reg 4	3	2	1	0	Reg. No.	Register Name	Stored Info	RD	WR	Register Bit 7	6	5	4	3	2	1	0
1	—	—	—	—	—	—	—				✓	X	X	X	X	X	X	X	X
0	0	—	—	—	—	—	—	Address Reg.	Reg. No.		✓	X	X	X	A_4	A_3	A_2	A_1	A_0
0	0	—	—	—	—	—	—	Status Reg.		✓		U	L	V	X	X	X	X	X
0	1	0	0	0	0	0	R0	Horiz. Total	# Charac.		✓	■	■	■	■	■	■	■	■
0	1	0	0	0	0	1	R1	Horiz. Displayed	# Charac.		✓	■	■	■	■	■	■	■	■
0	1	0	0	0	1	0	R2	Horiz. Sync Position	# Charac.		✓	■	■	■	■	■	■	■	■
0	1	0	0	0	1	1	R3	VSYNC, HSYNC Widths	# Scan Lines & # Char. Times		✓	V_3	V_2	V_1	V_0	H_3	H_2	H_1	H_0
0	1	0	0	1	0	0	R4	Vert. Total	# Charac. Row		✓	X	■	■	■	■	■	■	■
0	1	0	0	1	0	1	R5	Vert. Total Adjust.	# Scan Lines		✓	X	X	X	■	■	■	■	■
0	1	0	0	1	1	0	R6	Vert. Displayed	# Charac. Rows		✓	X	■	■	■	■	■	■	■
0	1	0	0	1	1	1	R7	Vert. Sync Position	# Charac. Rows		✓	X	■	■	■	■	■	■	■
0	1	0	1	0	0	0	R8	Mode Control			✓	■	■	■	■	■	■	■	■
0	1	0	1	0	0	1	R9	Scan Line	# Scan Lines		✓	X	X	X	■	■	■	■	■
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line No.		✓	X	B_1	B_0	■	■	■	■	■
0	1	0	1	0	1	1	R11	Cursor End	Scan Line No.		✓	X	X	X	■	■	■	■	■
0	1	0	1	1	0	0	R12	Display Start Addr (H)			✓	X	X	■	■	■	■	■	■
0	1	0	1	1	0	1	R13	Display Start Addr (L)			✓	■	■	■	■	■	■	■	■
0	1	0	1	1	1	0	R14	Cursor Position (H)		✓	✓	X	X	■	■	■	■	■	■
0	1	0	1	1	1	1	R15	Cursor Position (L)		✓	✓	■	■	■	■	■	■	■	■
0	1	1	0	0	0	0	R16	Light Pen Reg. (H)		✓		X	X	■	■	■	■	■	■
0	1	1	0	0	0	1	R17	Light Pen Reg. (L)		✓		■	■	■	■	■	■	■	■

Notes ■ Designates binary bit
X Designates unusued bit. Reading this bit is always "O", except for R31, which does not drive the data bus at all, and for CS "1" which operates likewise.

Figure 3. Internal Register Summary

Vertical Total Adjust (R5)

The Vertical Total Adjust Register is a 5-bit write only register containing the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

Vertical Displayed (R6)

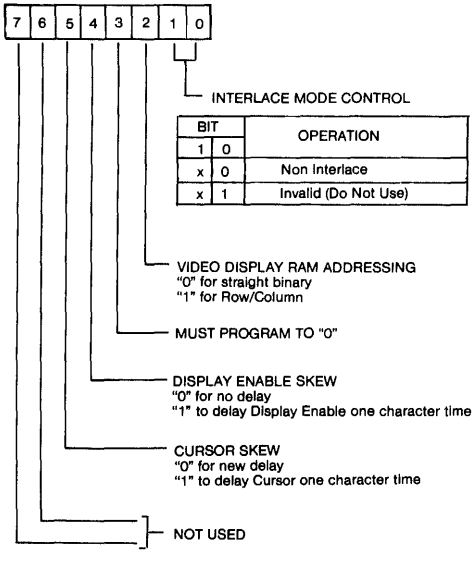
This 7-bit register contains the number of displayed character rows in each frame. In this way, the vertical size of the displayed text is determined.

Vertical Sync Position (R7)

This 7-bit register is used to select the character row time at which the VSYNC pulse is desired to occur and, thus, is used to position the displayed text in the vertical direction.

Mode Control (R8)

This register is used to select the operating modes of the 6545-1 and is outlined as follows:



Scan Line (R9)

This 5-bit register contains the number of scan lines per character row, including spacing.

Cursor Start (R10) and Cursor End (R11)

These 5-bit registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor mode, as follows:

BIT		CURSOR MODE
6	5	
0	0	No Blinking
0	1	No Cursor
1	0	Blink at 1/16 field rate
1	1	Blink at 1/32 field rate

Note that the ability to program both the start and end scan line for the cursor enables either block cursor or underline to be accommodated. Registers R14 and R15 are used to control the character position of the cursor over the entire 16K address field.

Display Start Address High (R12) and Low (R13)

These registers together comprise a 14-bit register whose contents is the memory address of the first character of the displayed scan (the character on the top left of the video display, as in Figure 1). Subsequent memory addresses are generated by the 6545-1 as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled or changed as well via R12 and R13.

Cursor Position High (R14) and Low (R15)

These registers together comprise a 14-bit register whose contents is the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

LPEN High (R16) and Low (R17)

These registers together comprise a 14-bit register whose contents is the light pen strobe position, in terms of the video display address at which the strobe occurred. When the LPEN input changes from low to high, then, on the next negative-going edge of CCLK, the contents of the internal scan counter is stored in registers R16 and R17.

DETAILED DESCRIPTION OF OPERATION

Register Formats

Register pairs R12/R13, R14/R15, and R16/R17 are formatted in one of two ways:

1. Straight binary if register R8, bit 2 is a "0".
2. Row/Column if register R8, bit 2 is a "1". In this case the low byte is the Character Column and the high byte is the Character Row.

Figure 4 illustrates the address sequence for the video display control for each mode.

Note from Figure 4 that the straight-binary mode has the advantage that all display memory addresses are stored in a continuous memory block, starting with address 0 and ending at 1919. The disadvantage with this method is that, if it is desired to change a displayed character location, the row and column identity of the location must be converted to its binary address before the memory may be written. The row/column mode, on the other hand, does not need to undergo this conversion. However, memory is not used as efficiently, since the memory addresses are not continuous, but gaps exist. This requires that the system be equipped with more memory than is actually used and this extra memory is wasted. Alternatively, address compression logic may be employed to translate the row/column format into a continuous address block.

In this way, the user may select whichever mode is best for the given application. The trade-offs between the modes are software versus hardware. Straight-binary mode minimizes hardware requirements and row/column requires minimum software.

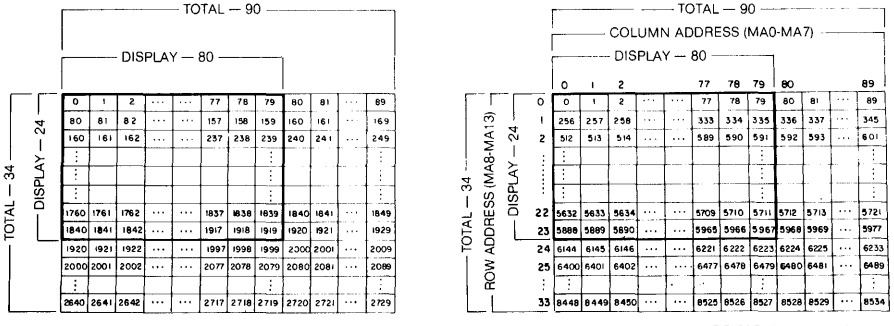
Memory Contention Schemes for Memory Addressing

From the diagram of Figure 4, it is clear that both the 6545-1 and the system MPU must be capable of addressing the video display memory. The 6545-1 repetitively fetches character information to generate the video signals in order to keep the screen display active. The MPU occasionally accesses the memory to change the displayed information or to read out current data characters. Three ways of resolving this dual-contention requirements are apparent:

- MPU Priority

  In this technique, the address lines to the video display memory are normally driven by the 6545-1 unless the MPU needs access, in which case the MPU addresses immediately override those from the 6545-1 and the MPU has immediate access.

- ø1/ø2 Memory Interleaving
  This method permits both the 6545-1 and the MPU access to the video display memory by time-sharing via the system o1 and ø2 clocks. During the ø1 portion of each cycle (the time when ø2 is low), the 6545-1 address



STRAIGHT BINARY ADDRESSING SEQUENCE **ROW/COLUMN ADDRESSING SEQUENCE**

Figure 4. Display Address Sequences (with Start Address = 0) for 80 x 24 Example

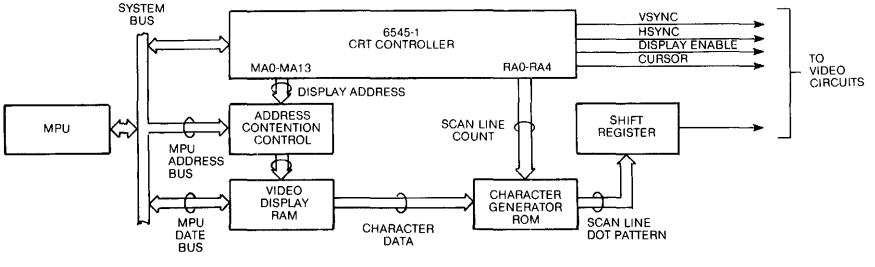


Figure 5. Typical System Configuration

outputs are gated to the video display memory. In the ø2 time, the MPU address lines are switched in. In this way, both the 6545-1 and the MPU have unimpeded access to the memory. Figure 6 illustrates the timings.

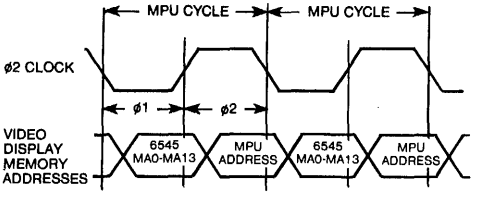


Figure 6. ø1/ø2 Interleaving

- Vertical Blanking

  With this approach, the address circuitry is identical to the case for MPU Priority updates. The only difference is that the Vertical Retrace status bit (bit 5 of the Status Register) is used by the MPU so that access to the video display memory is only made during vertical blanking time (when bit 5 is a "1"). In this way, no visible screen perturbations result.

Cursor and Display Enable Skew Control

Bits 4 and 5 of the Mode Control register (R8) are used to delay the Display Enable and Cursor outputs, respectively. Figure 7 illustrates the effect of the delays.

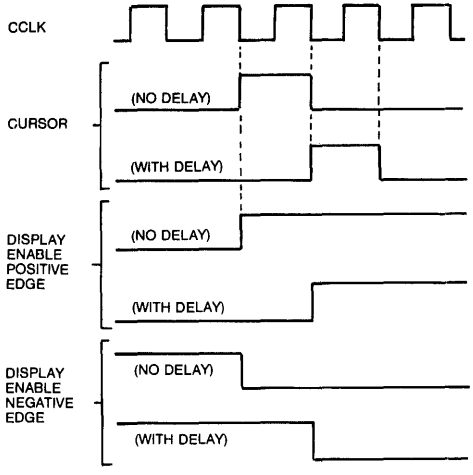


Figure 7. Cursor and Display Enable Skew

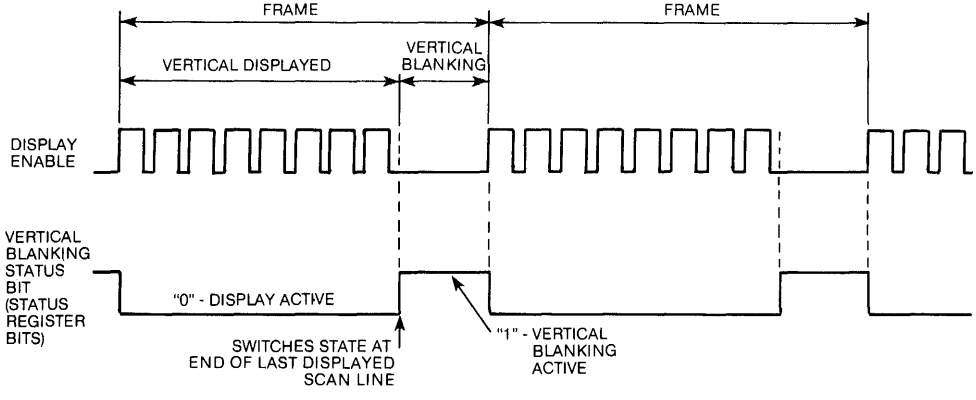


Figure 8. Operation of Vertical Blanking Status Bit