

MOSFET

650V CoolMOS™ CE Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ CE is a price-performance optimized platform enabling to target cost sensitive applications in Consumer and Lighting markets by still meeting highest efficiency standards. The new series provides all benefits of a fast switching Superjunction MOSFET while not sacrificing ease of use and offering the best cost down performance ratio available on the market.

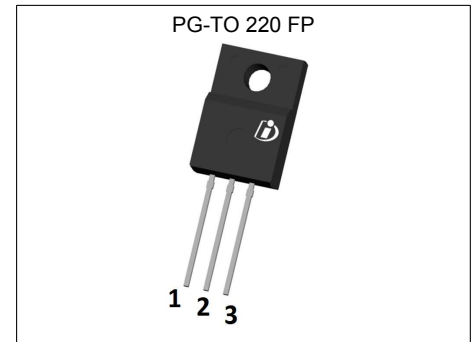
Features

- Extremely low losses due to very low FOM $R_{DS(on)} \cdot Q_g$ and E_{oss}
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for standard grade applications

Applications

PFC stages, hard switching PWM stages and resonant switching stages for e.g. PC Silverbox, Adapter, LCD & PDP TV and indoor lighting.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.



PG-TO 220 FP

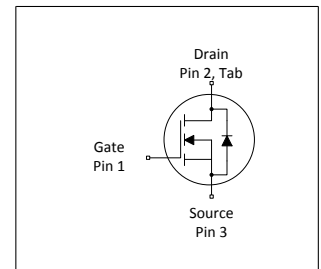


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	700	V
$R_{DS(on),max}$	650	$m\Omega$
I_D	10.1	A
$Q_{g,typ}$	23	nC
$I_{D,pulse}$	18	A
$E_{oss@400V}$	2	μJ

Type / Ordering Code	Package	Marking	Related Links
IPAN65R650CE	PG-TO 220 FullPAK - Narrow Lead	65S650CE	see Appendix A

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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	10.1 6.4	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	18	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	142	mJ	$I_D=1.3\text{A}$; $V_{DD}=50\text{V}$; see table 11
Avalanche energy, repetitive	E_{AR}	-	-	0.21	mJ	$I_D=1.3\text{A}$; $V_{DD}=50\text{V}$; see table 11
Avalanche current, repetitive	I_{AR}	-	-	1.3	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	$V_{DS}=0\dots480\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f>1\text{ Hz}$)
Power dissipation (Non FullPAK) TO-252	P_{tot}	-	-	86	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-40	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-40	-	150	$^\circ\text{C}$	-
Continuous diode forward current	I_S	-	-	7.1	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	18	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	15	V/ns	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 9
Maximum diode commutation speed	di _f /dt	-	-	500	A/ μs	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 9
Power dissipation (FullPAK) TO-220FP	P_{tot}	-	-	28	W	$T_C=25^\circ\text{C}$
Mounting torque (FullPAK) TO-220FP	-	-	-	50	Ncm	M2.5 screws
Insulation withstand voltage for TO-220FP	V_{ISO}	-	-	2500	V	V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{min}$

¹⁾ Limited by $T_{j,max}$. TO252 equivalent, Maximum duty cycle $D=0.50$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch with identical R_θ

2 Thermal characteristics

Table 3 Thermal characteristics (FullPAK) TO-220FP

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	4.5	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	$V_{GS}=0V, I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	2.5	3.0	3.5	V	$V_{DS}=V_{GS}, I_D=0.21mA$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=650, V_{GS}=0V, T_j=25^\circ\text{C}$ $V_{DS}=650, V_{GS}=0V, T_j=150^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.54 1.40	0.65	Ω	$V_{GS}=10V, I_D=2.1A, T_j=25^\circ\text{C}$ $V_{GS}=10V, I_D=2.1A, T_j=150^\circ\text{C}$
Gate resistance	R_G	-	10.5	-	Ω	$f=1\text{MHz}$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	440	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1\text{MHz}$
Output capacitance	C_{oss}	-	30	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1\text{MHz}$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	21	-	pF	$V_{GS}=0V, V_{DS}=0\dots480V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	88	-	pF	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0\dots480V$
Turn-on delay time	$t_{d(on)}$	-	10	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=3.2A,$ $R_G=6.8\Omega$; see table 10
Rise time	t_r	-	8	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=3.2A,$ $R_G=6.8\Omega$; see table 10
Turn-off delay time	$t_{d(off)}$	-	64	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=3.2A,$ $R_G=6.8\Omega$; see table 10
Fall time	t_f	-	11	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=3.2A,$ $R_G=6.8\Omega$; see table 10

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{GS}	-	2.75	-	nC	$V_{DD}=480V, I_D=3.2A, V_{GS}=0$ to 10V
Gate to drain charge	Q_{gd}	-	12	-	nC	$V_{DD}=480V, I_D=3.2A, V_{GS}=0$ to 10V
Gate charge total	Q_g	-	23	-	nC	$V_{DD}=480V, I_D=3.2A, V_{GS}=0$ to 10V
Gate plateau voltage	$V_{plateau}$	-	5.5	-	V	$V_{DD}=480V, I_D=3.2A, V_{GS}=0$ to 10V

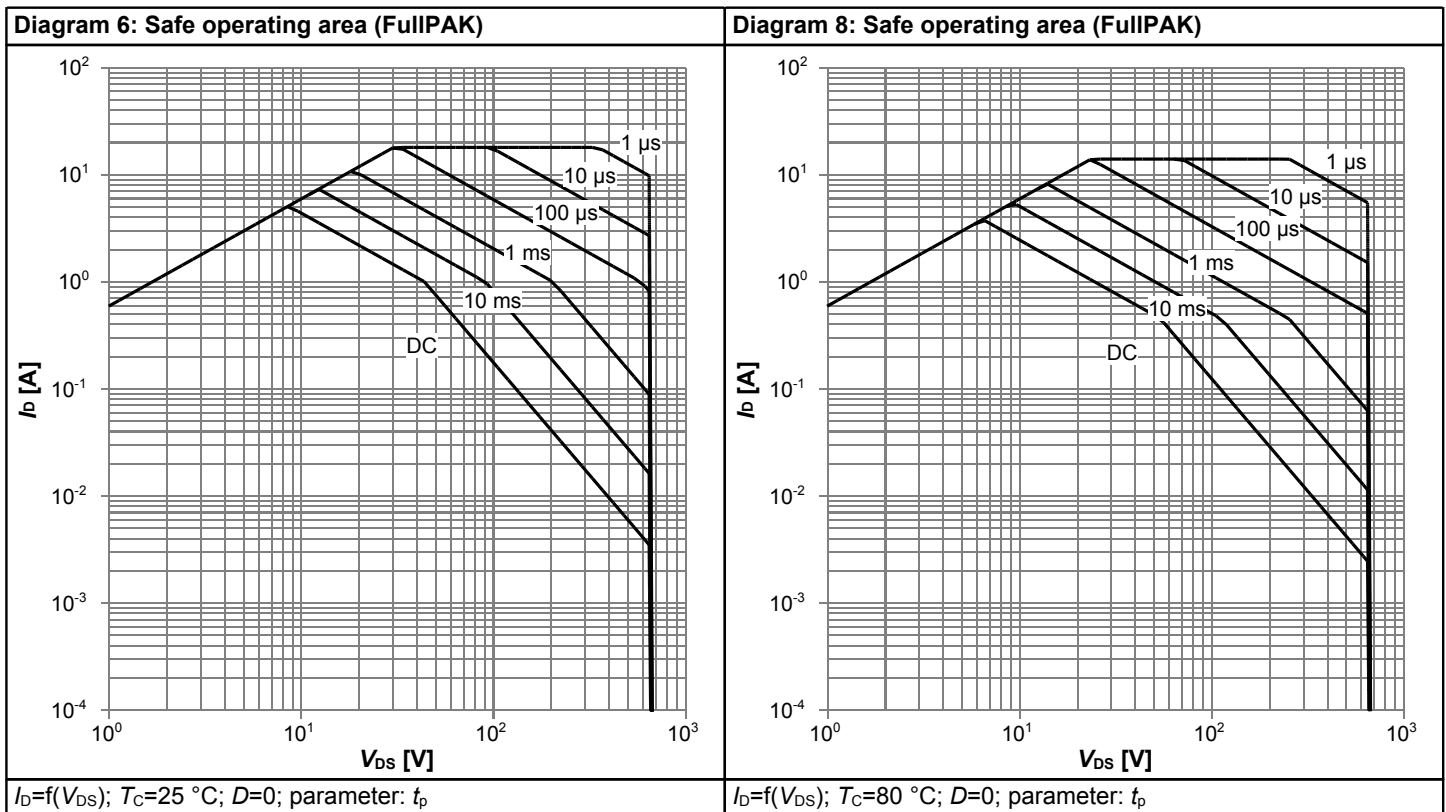
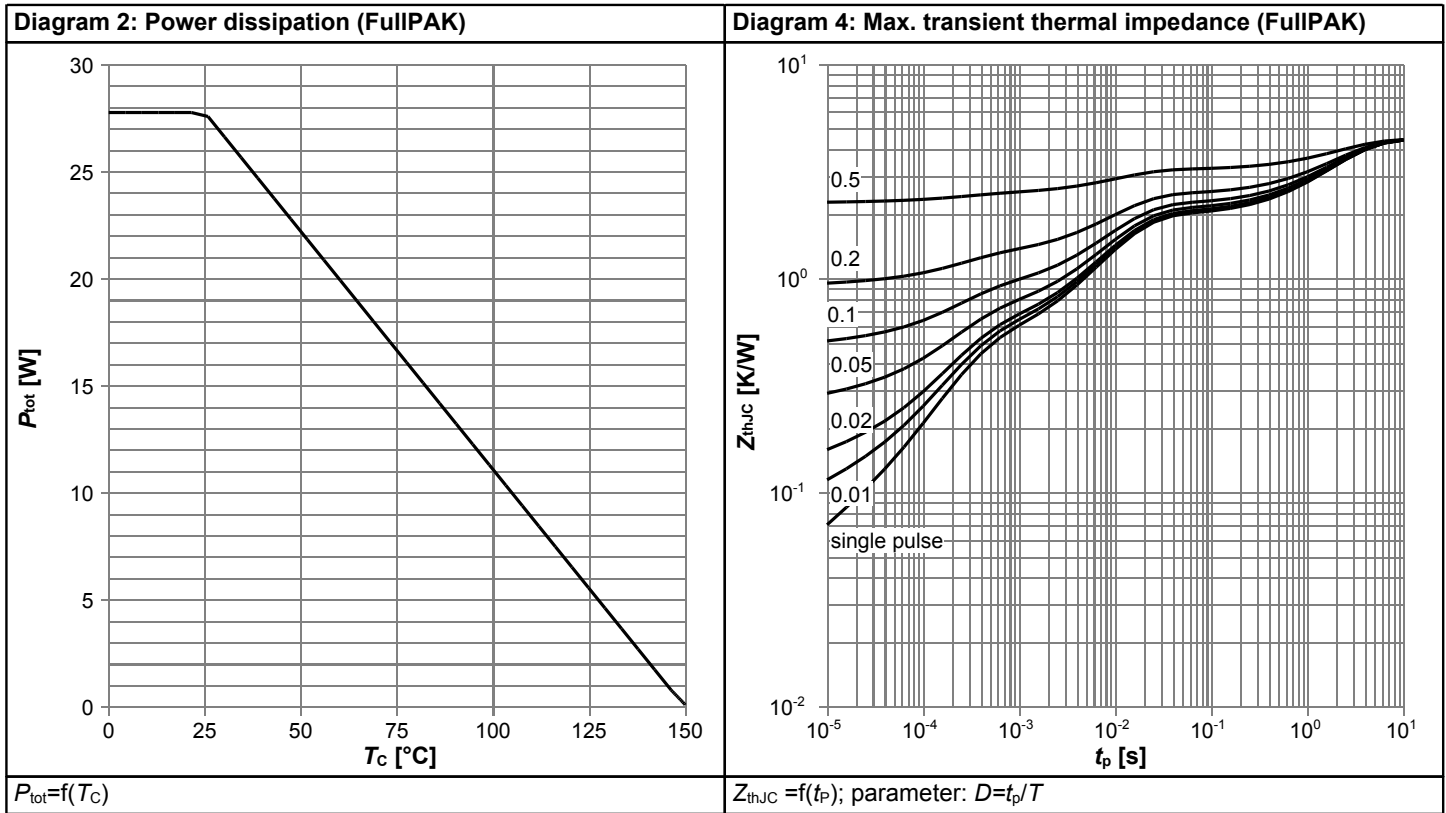
¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

Table 7 Reverse diode characteristics

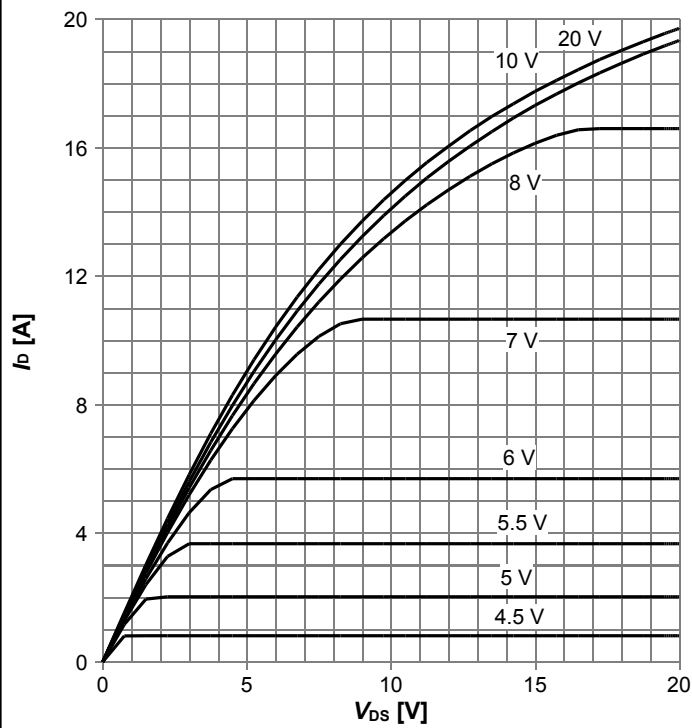
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0V, I_F=3.2A, T_j=25^\circ C$
Reverse recovery time	t_{rr}	-	270	-	ns	$V_R=400V, I_F=3.2A, di_F/dt=100A/\mu s$; see table 9
Reverse recovery charge	Q_{rr}	-	2	-	μC	$V_R=400V, I_F=3.2A, di_F/dt=100A/\mu s$; see table 9
Peak reverse recovery current	I_{rrm}	-	13	-	A	$V_R=400V, I_F=3.2A, di_F/dt=100A/\mu s$; see table 9

4 Electrical characteristics diagrams



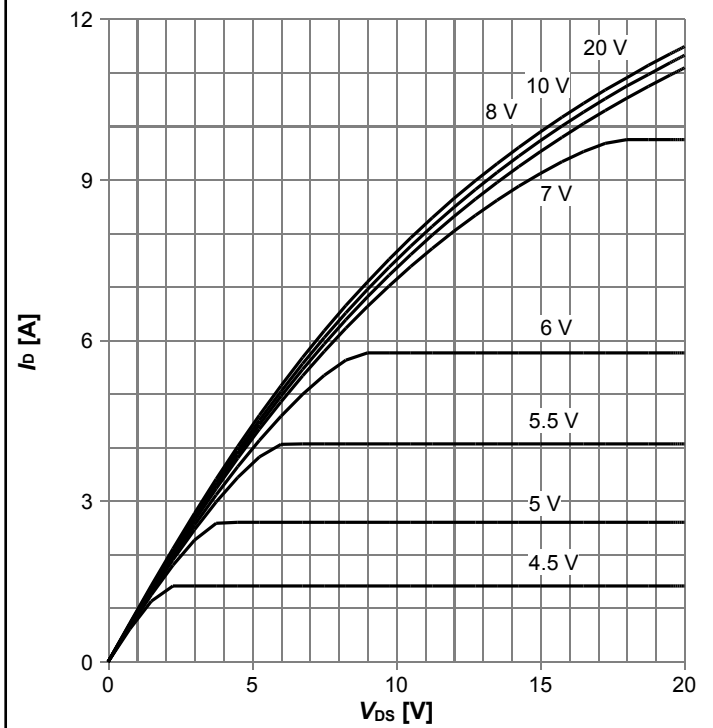
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Diagram 9: Typ. output characteristics



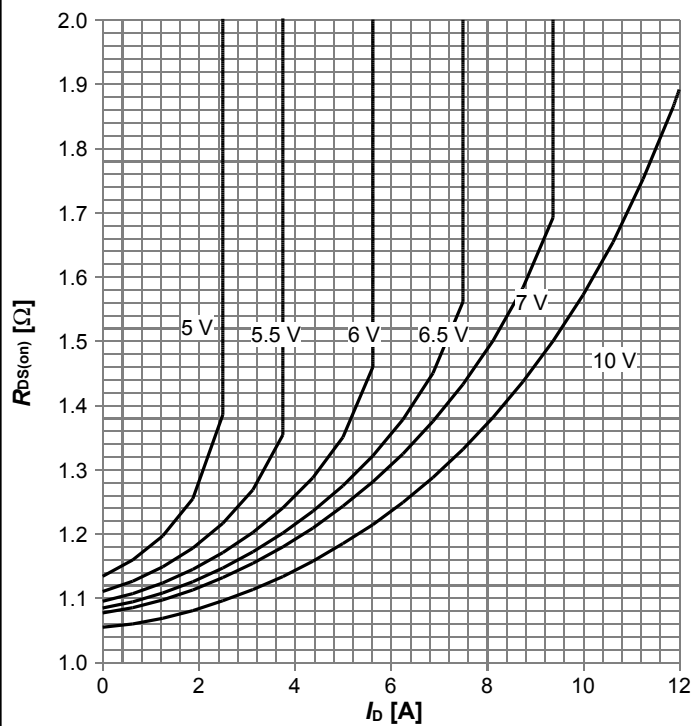
$I_D=f(V_{DS})$; $T_j=25\text{ °C}$; parameter: V_{GS}

Diagram 10: Typ. output characteristics



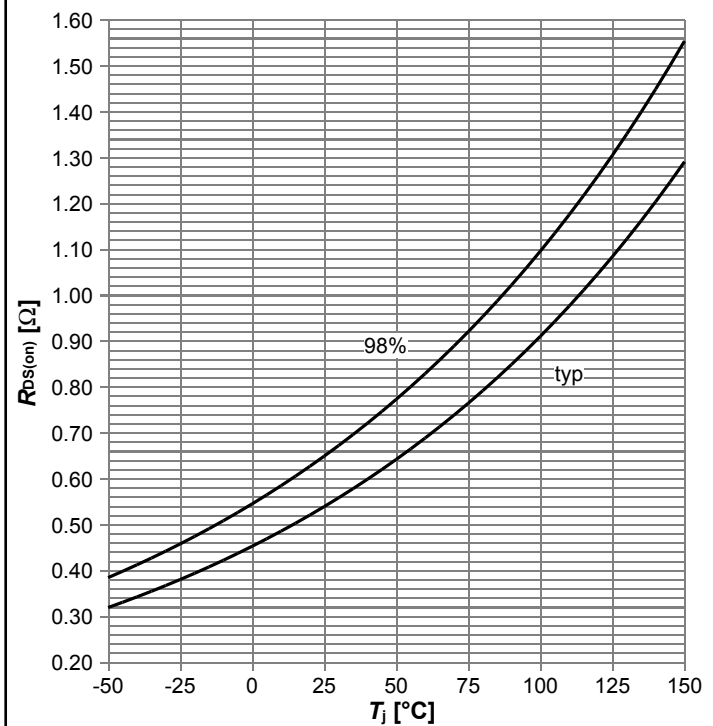
$I_D=f(V_{DS})$; $T_j=125\text{ °C}$; parameter: V_{GS}

Diagram 11: Typ. drain-source on-state resistance



$R_{DS(on)}=f(I_D)$; $T_j=125\text{ °C}$; parameter: V_{GS}

Diagram 12: Drain-source on-state resistance

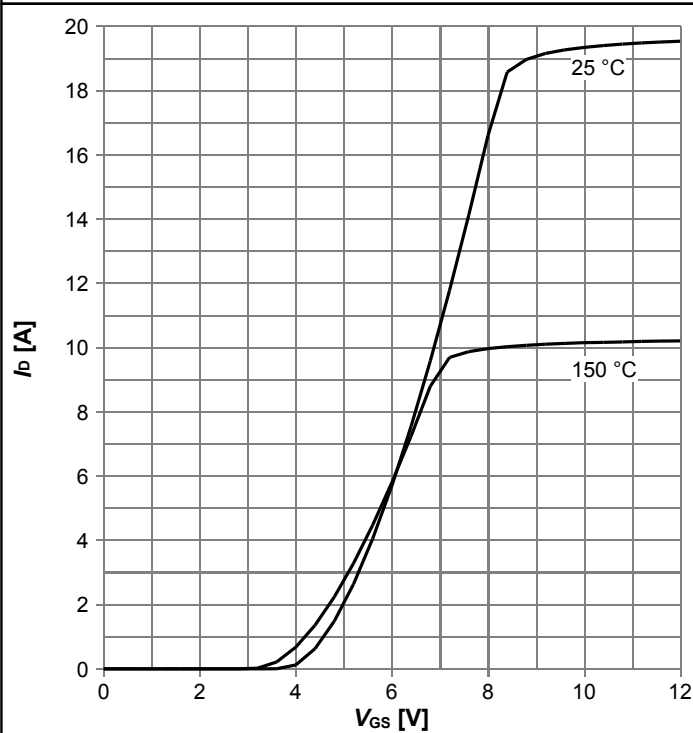


$R_{DS(on)}=f(T_j)$; $I_D=2.1\text{ A}$; $V_{GS}=10\text{ V}$

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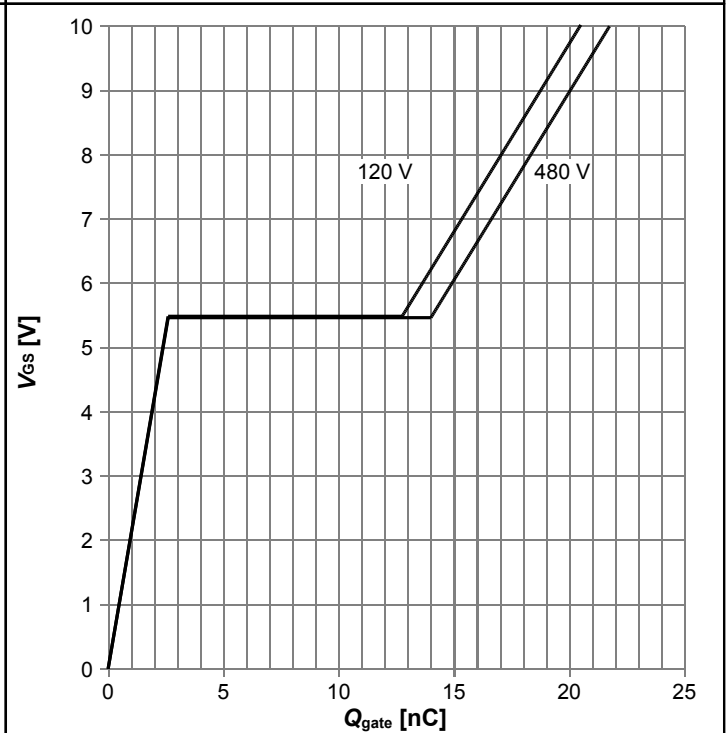
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Diagram 13: Typ. transfer characteristics



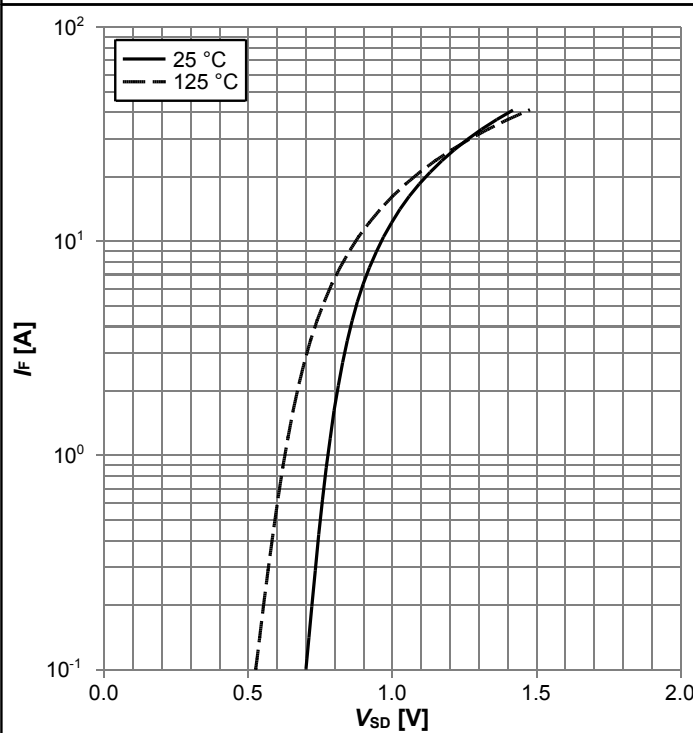
$I_D = f(V_{GS}); V_{DS} = 20V; \text{parameter: } T_j$

Diagram 14: Typ. gate charge



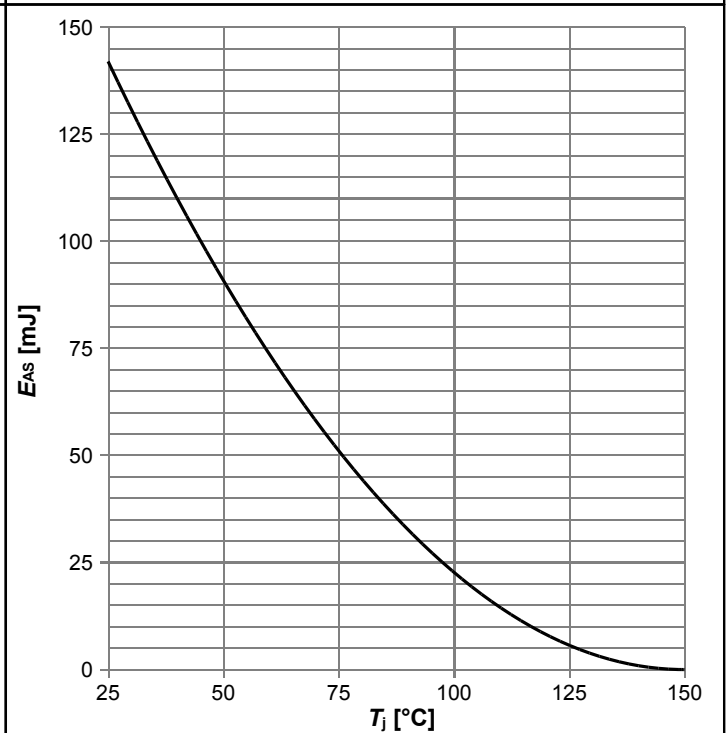
$V_{GS} = f(Q_{gate}); I_D = 3.2 \text{ A pulsed}; \text{parameter: } V_{DD}$

Diagram 15: Forward characteristics of reverse diode



$I_F = f(V_{SD}); \text{parameter: } T_j$

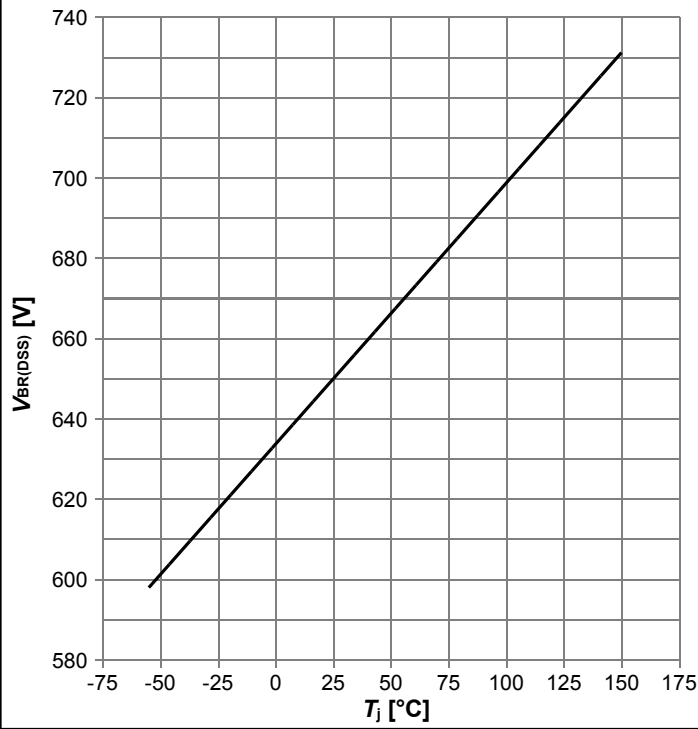
Diagram 16: Avalanche energy



$E_{AS} = f(T_j); I_D = 1.3 \text{ A}; V_{DD} = 50 \text{ V}$

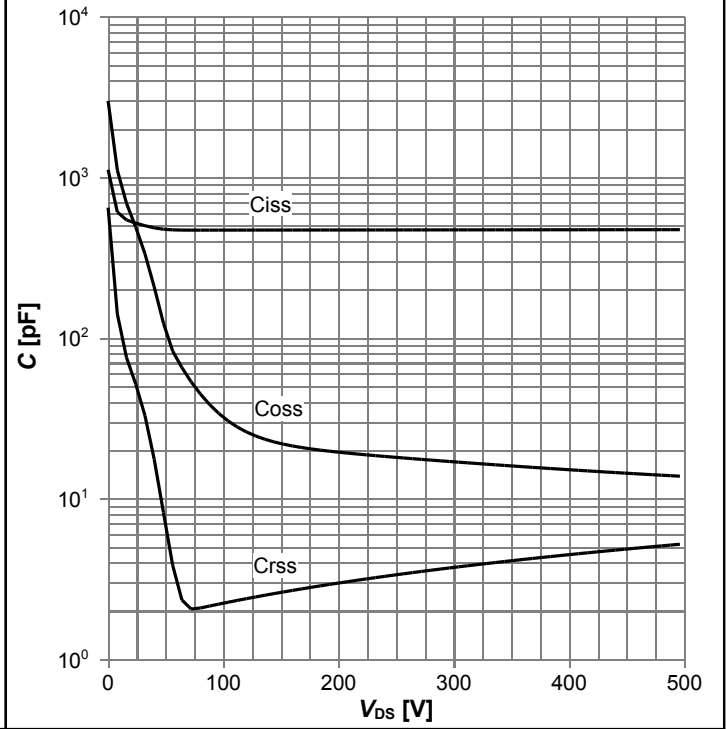
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Diagram 17: Drain-source breakdown voltage



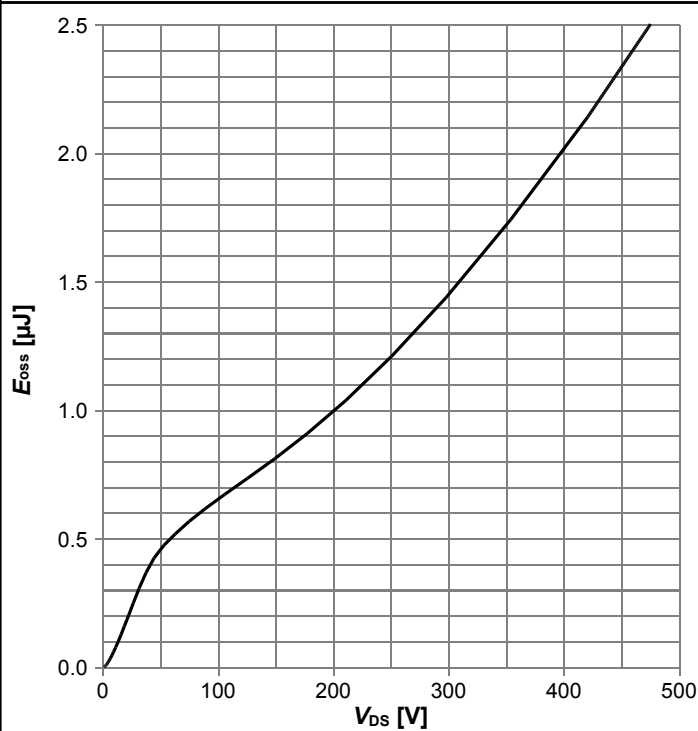
$V_{BR(DSS)}=f(T_j); I_D=1.0 \text{ mA}$

Diagram 18: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=1 \text{ MHz}$

Diagram 19: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

5 Test Circuits

Table 8 Diode characteristics

Test circuit for diode characteristics	Diode recovery waveform
<p>$R_{g1} = R_{g2}$</p>	<p>$t_{tr} = t_F + t_S$ $Q_{tr} = Q_F + Q_S$</p>

Table 9 Switching times

Switching times test circuit for inductive load	Switching times waveform

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform

6 Package Outlines

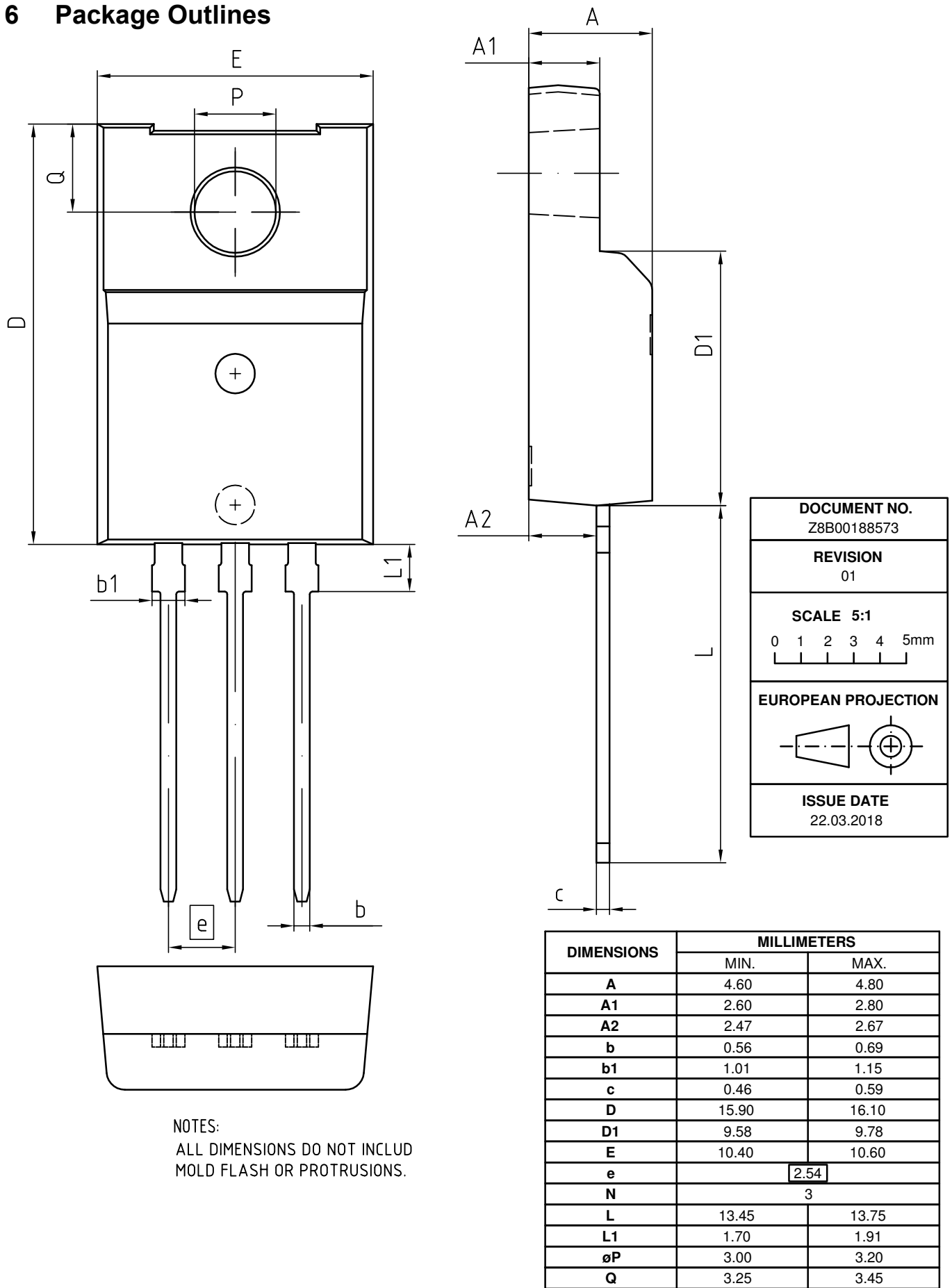


Figure 1 Outline PG-TO 220 FullPAK - Narrow Lead, dimensions in mm

7 Appendix A

Table 11 Related Links

- IFX CoolMOS™ CE Webpage: www.infineon.com
- IFX CoolMOS™ CE application note: www.infineon.com
- IFX CoolMOS™ CE simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPAN65R650CE

Revision: 2018-04-30, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-04-27	Release of final version
2.1	2016-11-28	Revised package drawing on page 11
2.2	2018-04-30	Revised package drawing

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