# A6821

## *DABiC-5 8-Bit Serial Input Latched Sink Drivers*

Package A
16-pin DIP

Package LW
16-pin Wide Body SOIC

A merged combination of bipolar and MOS technology gives these devices an interface flexibility beyond the reach of standard logic buffers and power driver arrays. Typical applications include driving multiplexed LED displays or incandescent lamps.

The A6821 has an eight-bit CMOS shift register and CMOS control circuitry, eight CMOS data latches, and eight bipolar current-sinking Darlington output drivers.

The CMOS inputs are compatible with standard CMOS logic levels. TTL circuits may require the use of appropriate pull-up resistors. By using the serial data output, the drivers can be cascaded for interface applications requiring additional drive lines.

The A6821SA is furnished in a standard 16-pin plastic DIP. The A6821EA is a 16-pin plastic DIP, capable of operation from -40°C to +85°C. The A6821SLW is a 16-lead wide-body SOIC, for surface-mount applications. These devices are lead (Pb) free, with 100% matte tin plated leadframes.

## ABSOLUTE MAXIMUM RATINGS

Output Voltage, $V_{OUT}$ .........................................**50 V**
Logic Supply Voltage, $V_{DD}$...................................**7 V**
Input Voltage Range, $V_{IN}$ ..............**–0.3 V to $V_{DD}$ +0.3 V**
Continuous Output Current (each output), $I_{OUT}$ ... **500 mA**
Package Power Dissipation, $P_D$
    A6821SA/A6821EA.................................**2.1 W**
    A6821SLW............................................ **1.5 W**
Operating Temperature Range
    Ambient Temperature, $T_A$ ............**–20°C to +85°C**
    Storage Temperature, $T_S$ ..........**–55°C to +150°C**

Caution: CMOS devices have input-static protection, but are susceptible to damage when exposed to extremely high static-electrical charges.

## FEATURES

- 3.3 V to 5 V logic supply range
- Power on reset (POR)
- To 10 MHz data input rate
- CMOS, TTL compatible
- –40°C operation available
- Schmitt trigger inputs for improved noise immunity
- Low-power CMOS logic and latches
- High-voltage current-sink outputs
- Internal pull-up/pull down resistors

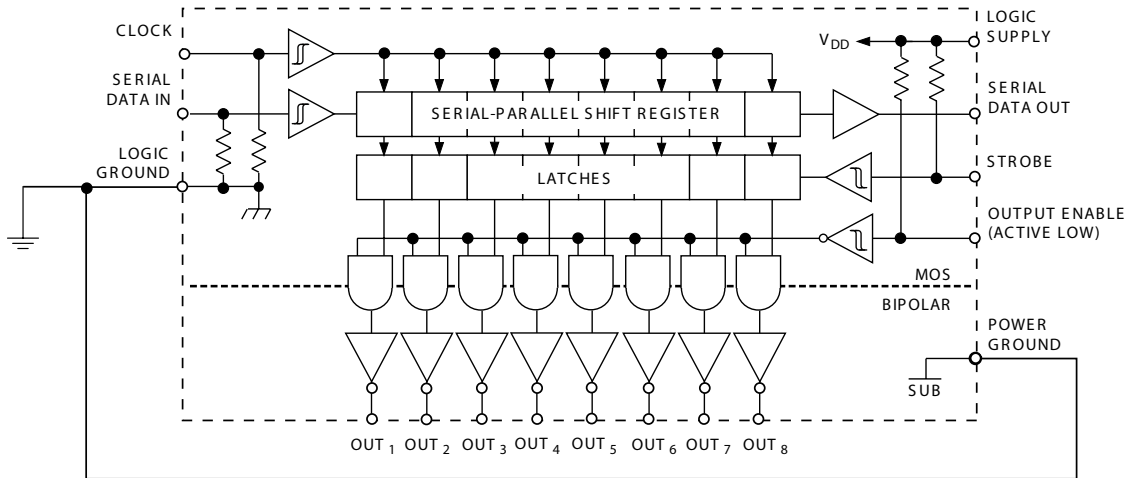## APPLICATIONS

- Multiplexed LED displays
- Incandescent lamps

Use the following complete part numbers when ordering:
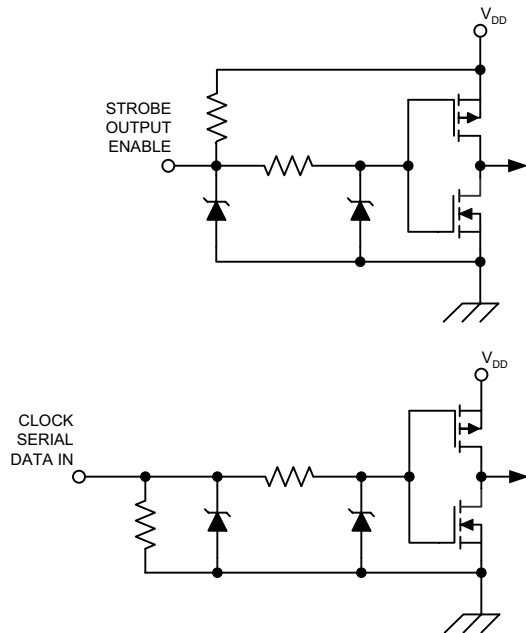
| Part Number | Package | Ambient |
|---|---|---|
| A6821SA-T | 16-pin DIP | −20ºC to +85ºC |
| A6821EA-T | 16-pin DIP | −40ºC to +85ºC |
| A6821SLW-T | 16-pin wide body SOIC | −20ºC to +85ºC |

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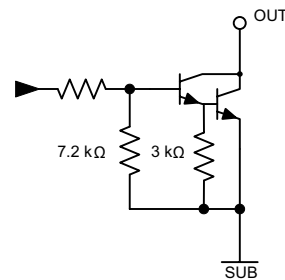MicroSystems, Inc.

Functional Block Diagram



Typical Input Circuits



Typical Output Driver

# A6821
# *DABiC-5 8-Bit Serial Input Latched Sink Drivers*

**ELECTRICAL CHARACTERISTICS**[1] Unless otherwise noted: $T_A$ = 25°C, logic supply operating voltage $V_{dd}$ = 3.0 V to 5.5 V

| Characteristic | Symbol | Test Conditions | $V_{dd}$ = 3.3 V Min. | Typ. | Max. | $V_{dd}$ = 5 V Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| Output Leakage Current | $I_{CEX}$ | $V_{OUT}$ = 50 V | – | – | 10 | – | – | 10 | µA |
| Collector–Emitter Saturation Voltage | $V_{CE(SAT)}$ | $I_{OUT}$ = 100 mA | – | – | 1.1 | – | – | 1.1 | V |
| | | $I_{OUT}$ = 200 mA | – | – | 1.3 | – | – | 1.3 | V |
| | | $I_{OUT}$ = 350 mA | – | – | 1.6 | – | – | 1.6 | V |
| Input Voltage | $V_{IN(1)}$ | | 2.2 | – | – | 3.3 | – | – | V |
| | $V_{IN(0)}$ | | – | – | 1.1 | – | – | 1.7 | V |
| Input Resistance | $R_{IN}$ | | 50 | – | – | 50 | – | – | kΩ |
| Serial Data Output Voltage | $V_{OUT(1)}$ | $I_{OUT}$ = –200 µA | 2.8 | 3.05 | – | 4.5 | 4.75 | – | V |
| | $V_{OUT(0)}$ | $I_{OUT}$ = 200 µA | – | 0.15 | 0.3 | – | 0.15 | 0.3 | V |
| Maximum Clock Frequency[2] | $f_c$ | | 10 | – | – | 10 | – | – | MHz |
| Logic Supply Current | $I_{DD(1)}$ | One output on, OE = L, ST = H | – | – | 2.0 | – | – | 2.0 | mA |
| | $I_{DD(0)}$ | All outputs off, OE = H, ST = H, P1 through P8 = L | – | – | 100 | – | – | 100 | µA |
| Output Enable-to-Output Delay | $t_{dis(BQ)}$ | $V_{CC}$ = 50 V, R1 = 500 Ω, C1 ≤ 30 pF | – | – | 1.0 | – | – | 1.0 | µs |
| | $t_{en(BQ)}$ | $V_{CC}$ = 50 V, R1 = 500 Ω, C1 ≤ 30 pF | – | – | 1.0 | – | – | 1.0 | µs |
| Strobe-to-Output Delay | $t_{p(STH-QL)}$ | $V_{CC}$ = 50 V, R1 = 500 Ω, C1 ≤ 30 pF | – | – | 1.0 | – | – | 1.0 | µs |
| | $t_{p(STH-QH)}$ | $V_{CC}$ = 50 V, R1 = 500 Ω, C1 ≤ 30 pF | – | – | 1.0 | – | – | 1.0 | µs |
| Output Fall Time | $t_f$ | $V_{CC}$ = 50 V, R1 = 500 Ω, C1 ≤ 30 pF | – | – | 1.0 | – | – | 1.0 | µs |
| Output Rise Time | $t_r$ | $V_{CC}$ = 50 V, R1 = 500 Ω, C1 ≤ 30 pF | – | – | 1.0 | – | – | 1.0 | µs |
| Clock-to-Serial Data Out Delay | $t_{p(CH-SQX)}$ | $I_{OUT}$ = ±200 µA | – | 50 | – | – | 50 | – | ns |

[1]Positive (negative) current is defined as conventional current going into (coming out of) the specified device pin.
[2]Operation at a clock frequency greater than the specified minimum value is possible but not warranted.

Truth Table

| Serial Data Input | Clock Input | Shift Register Contents $I_1$ $I_2$ $I_3$ ... $I_8$ | | | | | Serial Data Output | Strobe Input | Latch Contents $I_1$ $I_2$ $I_3$ ... $I_8$ | | | | | Output Enable Input | Output Contents $I_1$ $I_2$ $I_3$ ... $I_8$ | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| H | ⌐ | H | $R_1$ | $R_2$ | ... | $R_7$ | $R_7$ | | | | | | | | | | | |
| L | ⌐ | L | $R_1$ | $R_2$ | ... | $R_7$ | $R_7$ | | | | | | | | | | | |
| X | ⌐| | $R_1$ | $R_2$ | $R_3$ | ... | $R_8$ | $R_8$ | | | | | | | | | | |
| | | X | X | X | ... | X | X | L | $R_1$ | $R_2$ | $R_3$ | ... | $R_8$ | | | | | |
| | | $P_1$ | $P_2$ | $P_3$ | ... | $P_8$ | $P_8$ | H | $P_1$ | $P_2$ | $P_3$ | ... | $P_8$ | L | $P_1$ | $P_2$ | $P_3$ | ... $P_8$ |
| | | | | | | | | | X | X | X | ... | X | H | H | H | H | ... H |

L = Low Logic Level       R = Previous State
H = High Logic Level      OE = Output Enable
X = Irrelevant            ST = Strobe
P = Present State

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## Timing Requirements and Specifications
### (Logic Levels are $V_{DD}$ and Ground)
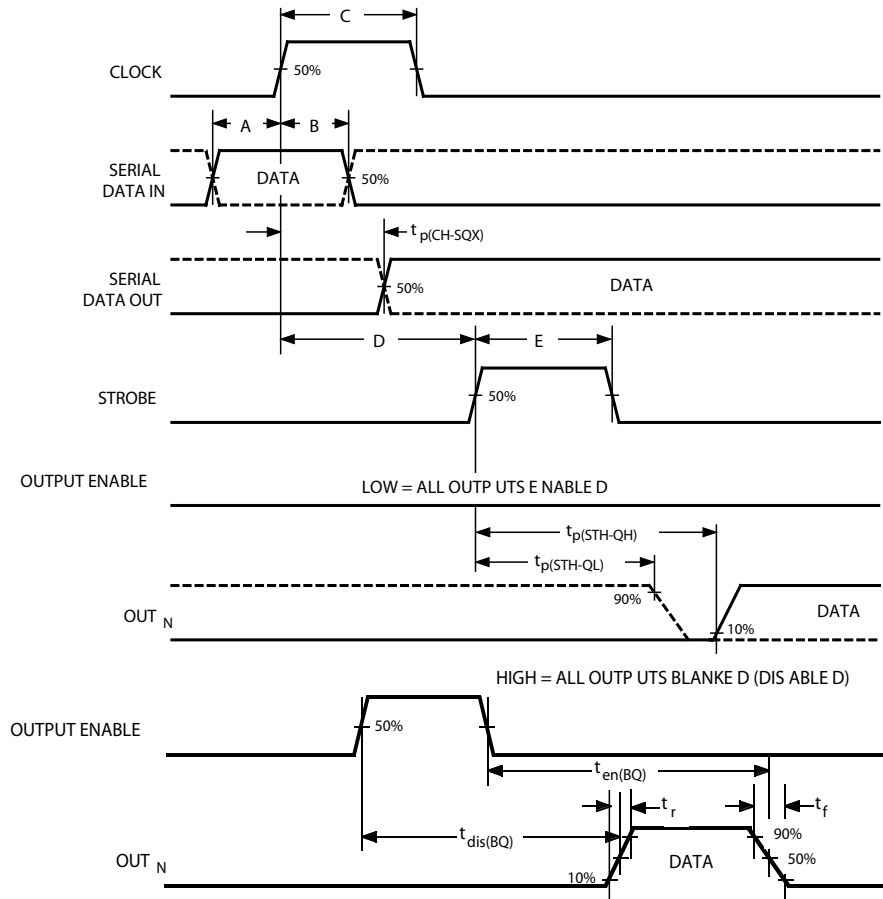


| Key | Description | Symbol | Time (ns) |
|-----|-------------|--------|-----------|
| A | Data Active Time Before Clock Pulse (Data Set-Up Time) | $t_{su(D)}$ | 25 |
| B | Data Active Time After Clock Pulse (Data Hold Time) | $t_{h(D)}$ | 25 |
| C | Clock Pulse Width | $t_{w(CH)}$ | 50 |
| D | Time Between Clock Activation and Strobe | $t_{su(C)}$ | 100 |
| E | Strobe Pulse Width | $t_{w(STH)}$ | 50 |

NOTE: Timing is representative of a 10 MHz clock. Higher speeds may be attainable; operation at high temperatures will reduce the specified maximum clock frequency.

Powering-on with the inputs in the low state ensures that the registers and latches power-on in the low state (POR).

Serial Data present at the input is transferred to the shift register on the logical 0 to logical 1 transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be high during serial data entry.

When the OUTPUT ENABLE input is high, all of the output buffers are disabled (OFF). The information stored in the latches or shift register is not affected by the OUTPUT ENABLE input. With the OUTPUT ENABLE input low, the outputs are controlled by the state of their respective latches.

Maximum Allowable Duty Cycle, $I_{OUT}$ = 200 mA, $V_{DD}$ = 5 V

| Number of Outputs ON | Ambient Temperature | | | | |
|---|---|---|---|---|---|
| | 25°C | 40°C | 50°C | 60°C | 70°C |
| A6821SA/A6821EA | | | | | |
| 8 | 90% | 79% | 72% | 65% | 57% |
| 7 | 100% | 90% | 82% | 74% | 65% |
| 6 | 100% | 100% | 96% | 86% | 76% |
| 5 | 100% | 100% | 100% | 100% | 91% |
| 4 | 100% | 100% | 100% | 100% | 100% |
| 3 | 100% | 100% | 100% | 100% | 100% |
| 2 | 100% | 100% | 100% | 100% | 100% |
| 1 | 100% | 100% | 100% | 100% | 100% |
| A6821SLW | | | | | |
| 8 | 67% | 59% | 54% | 49% | 43% |
| 7 | 77% | 68% | 62% | 56% | 49% |
| 6 | 90% | 79% | 72% | 65% | 57% |
| 5 | 100% | 95% | 86% | 78% | 68% |
| 4 | 100% | 100% | 100% | 98% | 86% |
| 3 | 100% | 100% | 100% | 100% | 100% |
| 2 | 100% | 100% | 100% | 100% | 100% |
| 1 | 100% | 100% | 100% | 100% | 100% |

Terminal List Table

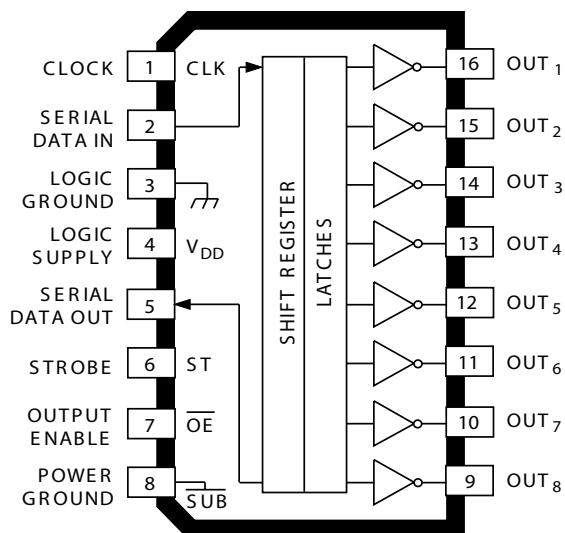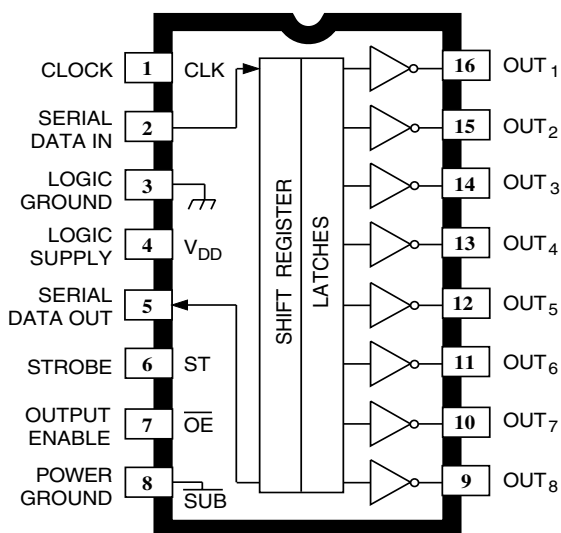| Name | Description | Pin |
|---|---|---|
| CLK | Clock | 1 |
| | Serial Data In | 2 |
| | Logic Ground* | 3 |
| VDD | Logic Supply | 4 |
| | Serial Data Out | 5 |
| ST | Strobe | 6 |
| $\overline{OE}$ | Output Enable (active low) | 7 |
| SUB | Power Ground* | 8 |
| $OUT_8$ | Serial Data Output | 9 |
| $OUT_7$ | Serial Data Output | 10 |
| $OUT_6$ | Serial Data Output | 11 |
| $OUT_5$ | Serial Data Output | 12 |
| $OUT_4$ | Serial Data Output | 13 |
| $OUT_3$ | Serial Data Output | 14 |
| $OUT_2$ | Serial Data Output | 15 |
| $OUT_1$ | Serial Data Output | 16 |

* There is an indeterminate resistance between logic ground and power ground.
For proper operation, these terminals must be externally connected together.

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Package A
16-pin DIP

| | | | |
|---|---|---|---|
| CLOCK | 1 | CLK | |
| SERIAL DATA IN | 2 | | |
| LOGIC GROUND | 3 | | |
| LOGIC SUPPLY | 4 | $V_{DD}$ | |
| SERIAL DATA OUT | 5 | | |
| STROBE | 6 | ST | |
| OUTPUT ENABLE | 7 | $\overline{OE}$ | |
| POWER GROUND | 8 | $\overline{SUB}$ | |

SHIFT REGISTER  LATCHES

| | |
|---|---|
| 16 | OUT$_1$ |
| 15 | OUT$_2$ |
| 14 | OUT$_3$ |
| 13 | OUT$_4$ |
| 12 | OUT$_5$ |
| 11 | OUT$_6$ |
| 10 | OUT$_7$ |
| 9 | OUT$_8$ |

Package LW
16-pin Wide Body SOIC

| | | | |
|---|---|---|---|
| CLOCK | 1 | CLK | |
| SERIAL DATA IN | 2 | | |
| LOGIC GROUND | 3 | | |
| LOGIC SUPPLY | 4 | $V_{DD}$ | |
| SERIAL DATA OUT | 5 | | |
| STROBE | 6 | ST | |
| OUTPUT ENABLE | 7 | $\overline{OE}$ | |
| POWER GROUND | 8 | $\overline{SUB}$ | |

SHIFT REGISTER  LATCHES

| | |
|---|---|
| 16 | OUT$_1$ |
| 15 | OUT$_2$ |
| 14 | OUT$_3$ |
| 13 | OUT$_4$ |
| 12 | OUT$_5$ |
| 11 | OUT$_6$ |
| 10 | OUT$_7$ |
| 9 | OUT$_8$ |

# DABiC-5 8-Bit Serial Input Latched Sink Drivers

## Package A
16-pin DIP

**Dimensions in Inches**
(controlling dimensions)

16         9

0.014
0.008

0.280
0.240

0.430
MAX

0.300
BSC

1
0.070
0.045

0.100
BSC

8

0.005
MIN

0.775
0.735

0.210
MAX

0.015
MIN

0.150
0.115

0.022
0.014

Dwg. MA-001-16A in
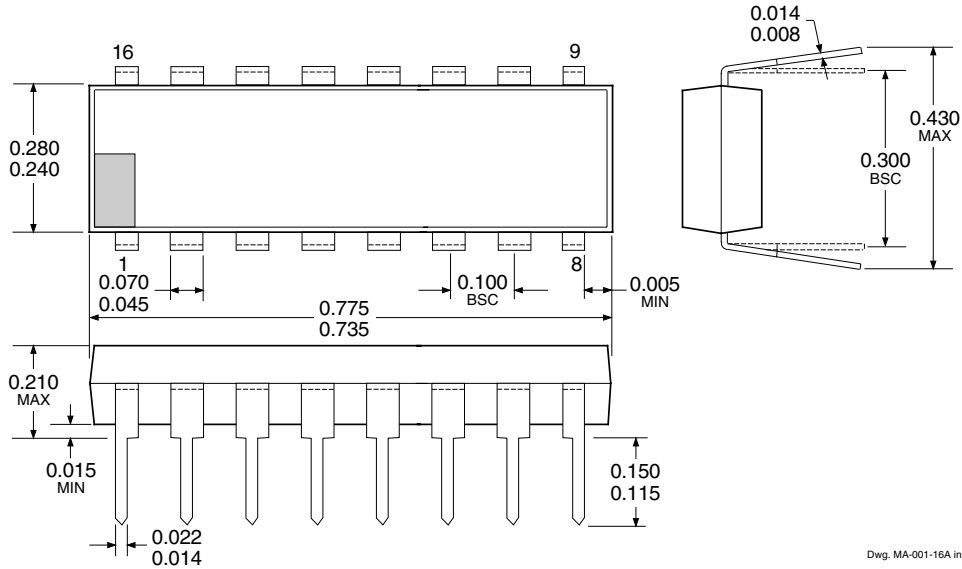
**Dimensions in Millimeters**
(for reference only)

16         9

0.355
0.204

7.11
6.10

10.92
MAX

7.62
BSC

1
1.77
1.15

2.54
BSC

8

0.13
MIN

19.68
18.67

5.33
MAX

0.39
MIN

3.81
2.93

0.558
0.356

Dwg. MA-001-16A mm
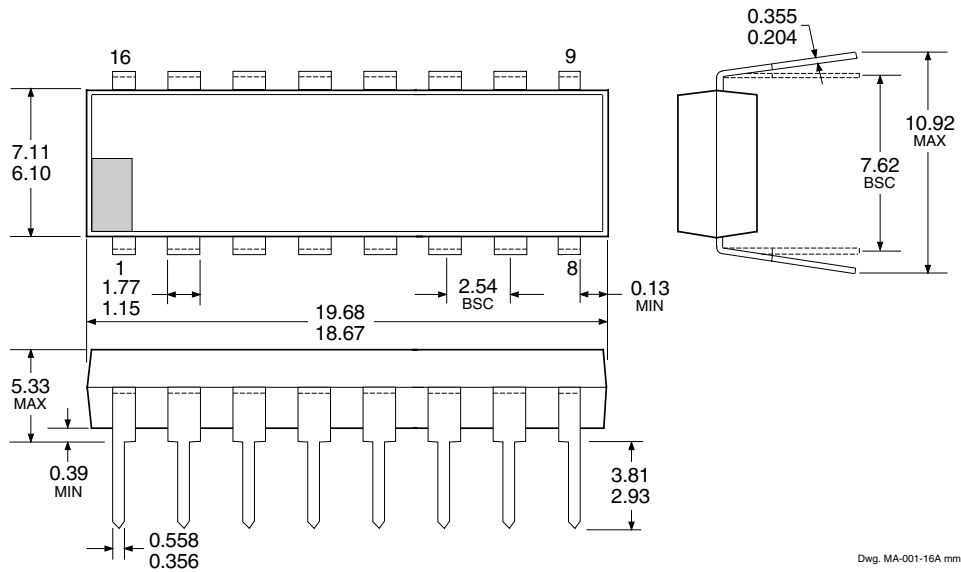
NOTES: 1. Lead thickness is measured at seating plane or below.
2. Lead spacing tolerance is non-cumulative.
3. Exact body and lead configuration at vendor's option within limits shown.

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# A6821
## *DABiC-5 8-Bit Serial Input Latched Sink Drivers*
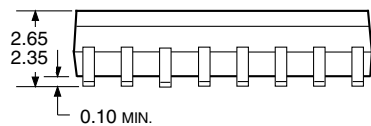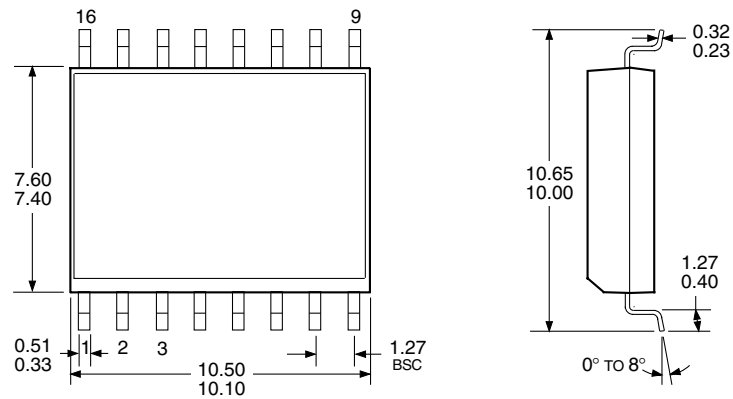
## Package LW
16-pin Wide Body SOIC

**Dimensions in Inches**
(for reference only)
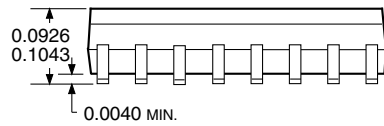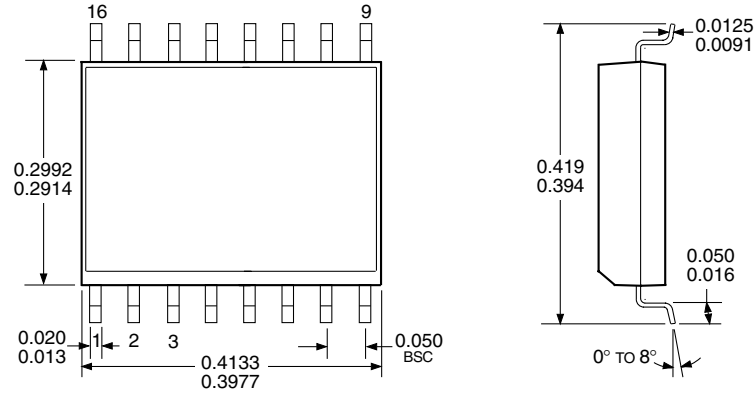


Dwg. MA-008-16A in

**Dimensions in Millimeters**
(controlling dimensions)



Dwg. MA-008-16A mm

NOTES: 1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.

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