Description

The device is a single channel, fixed delay IC. Ultra-compact 2 × 2 mm 8-DFN package with no external reference required with extended temperature operating range.

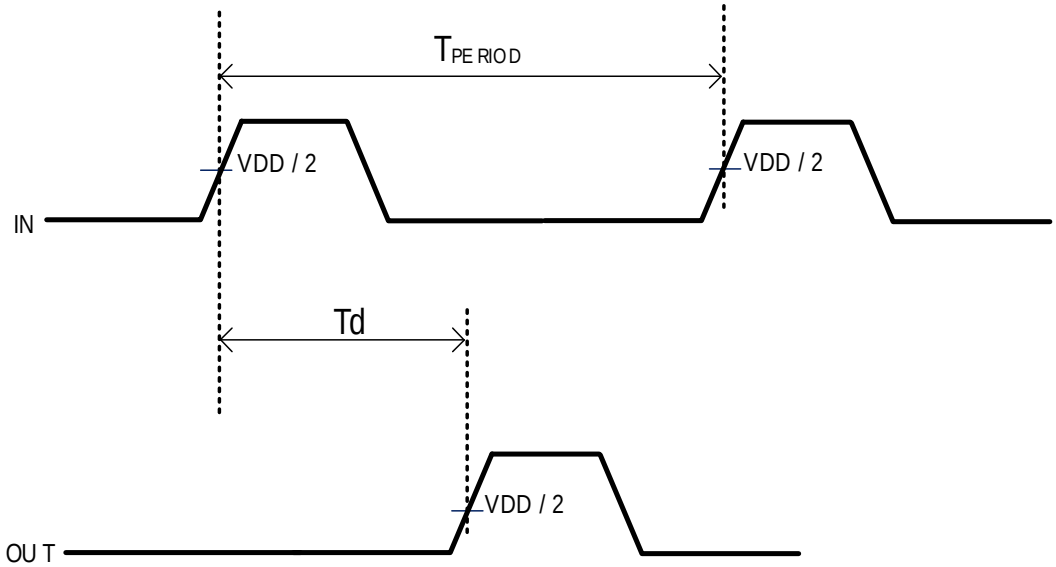
Typical Applications

- Timing control
- Pulse delay

Features

- Supports 2.5V and 3.3V power supplies
- Multiple input to output delay options based on latched status
  - 100ns delay time setting
  - 75ns delay time setting
- Single channel operation
- -40°C to 105°C operating temperature
- Compact 2 × 2 mm 8-DFN package

Functional Diagram



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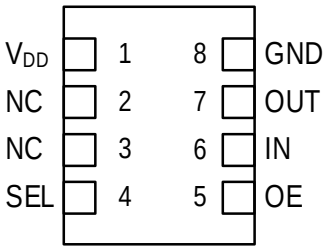
1. Pin Assignments

Figure 1. Pin Assignments for 2 × 2 mm 8-DFN – Top View



2. Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Name	Type	Description
1	VDD	Power	Power supply.
2	NC	–	No Connect.
3	NC	–	No Connect.
4	SEL	Input (Internal Pull-up)	Delay select. When SEL set to high, OUT operates with 75ns T_D setting. When SEL set to low, OUT operates with 100ns T_D setting.
5	OE	Input (Internal Pull-up)	Output Enable for OUT, active high.
6	IN	Input	Input.
7	OUT	Output	Delayed output.
8	GND	Ground	Connect to ground.

3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the device at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Ratings	Units
T_J	Junction Temperature	125	°C
T_S	Storage Temperature	-65 to 150	°C
V_{DD}	Supply Voltage	3.8	V
V_{IN}	Input Voltage (IN, OE, SEL)	V_{DD}	V
	ESD – Charged Device Model	1500	V
	ESD – Human Body Model	2000	V

4. Thermal Characteristics

Table 3. Thermal Characteristics

Symbol	Parameter	Value	Units
θ_{JA}	Theta JA. Junction to air.	88.07	°C/W
θ_{JB}	Theta JB. Junction to board.	15.6	°C/W
θ_{JC}	Theta JC. Junction to case.	175.4	°C/W

.

5. Electrical Characteristics

V_{DD} = 3.3V ±10%, 2.5V ±10%, T_A = -40°C to 105°C

Table 4. Electrical Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
I_{DD}[a]	Power Supply Current	Output enabled.		4		mA
I_{DDS}[a]	Static Supply Current	Output disabled.		3.7		mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		0.7 × V_{DD}			V
I_{IL}	Input Leakage Current Low	IN.	-5		5	µA
I_{IL}	Input Leakage Current Low	OE, SEL.	-25		-6	µA
I_{IH}	Input Leakage Current High	IN, OE, SEL.	-5		5	uA
V_{OL}	Output Low Voltage	+2mA load.			0.4	V
V_{OH}	Output High Voltage	-2mA load.	0.7 × V_{DD}			V
R_{UP}	Internal Pull-up Resistance	OE, SEL.		250		kΩ
T_D	Delay Time		-10		10	%
T_R	Output Rise Time	20% to 80%.		350		ps
T_F	Output Fall Time	80% to 20%.		300		ps
T_{WIDTH}[b]	Pulse Width		17			ns
T_{PERIOD}[c]	Minimum Input Period		T_D/4			ns

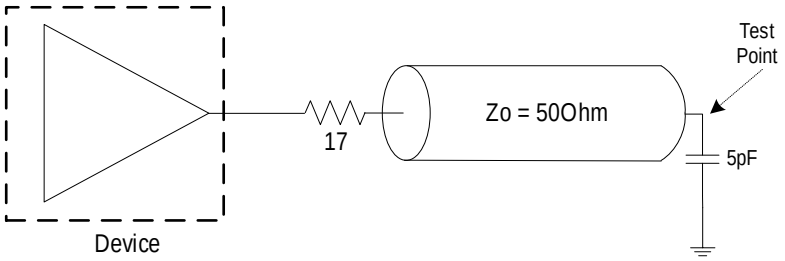
[a] Measured with periodic 1MHz clock signal, rail to rail input.

[b] Measured at 50% of V_{DD} level.

[c] Variation needs to be taken into consideration for different devices across process and temperature. Please refer to parameter T_D specification.

6. Output Load Circuit

Figure 2. Single-ended Output Test Load



7. Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

https://www.renesas.com/us/en/document/psc/8-dfn-package-outline-drawing20-x-20-x-075-mm-body-05mm-pitch-epad-09-x-160-mm-ntg8p1

8. Marking Diagram

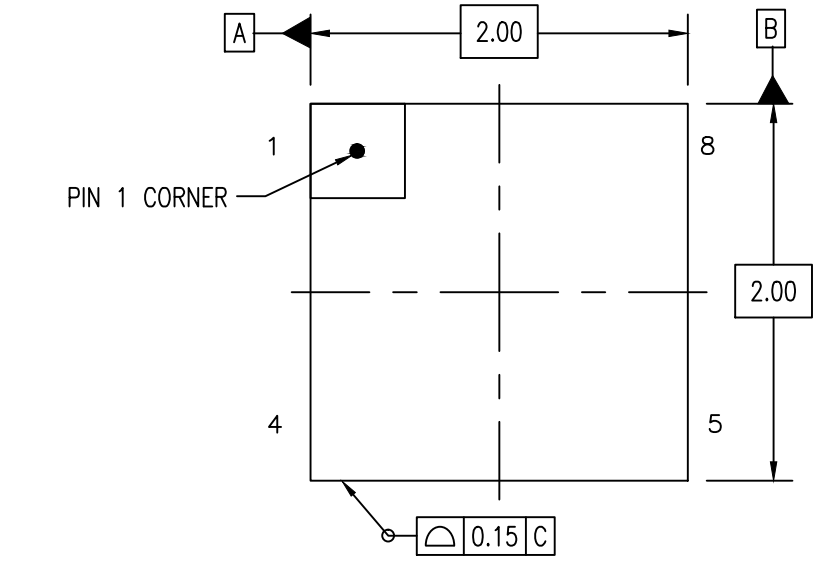
- Line 1 is the truncated part number.
- "YW" is the last digit of the year and work week that the part was assembled.
- "**" denotes sequential lot number.

9. Ordering Information

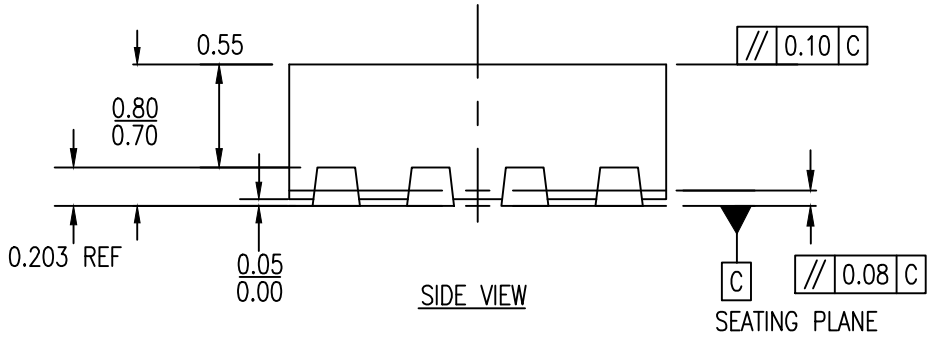
Orderable Part Number	Description and Package	Carrier Type	Temperature
6T80002NTGK	2 × 2 mm, 0.5mm pitch 8-DFN	Tray	-40°C to +105°C
6T80002NTGK8	2 × 2 mm, 0.5mm pitch 8-DFN	Reel	-40°C to +105°C

10. Revision History

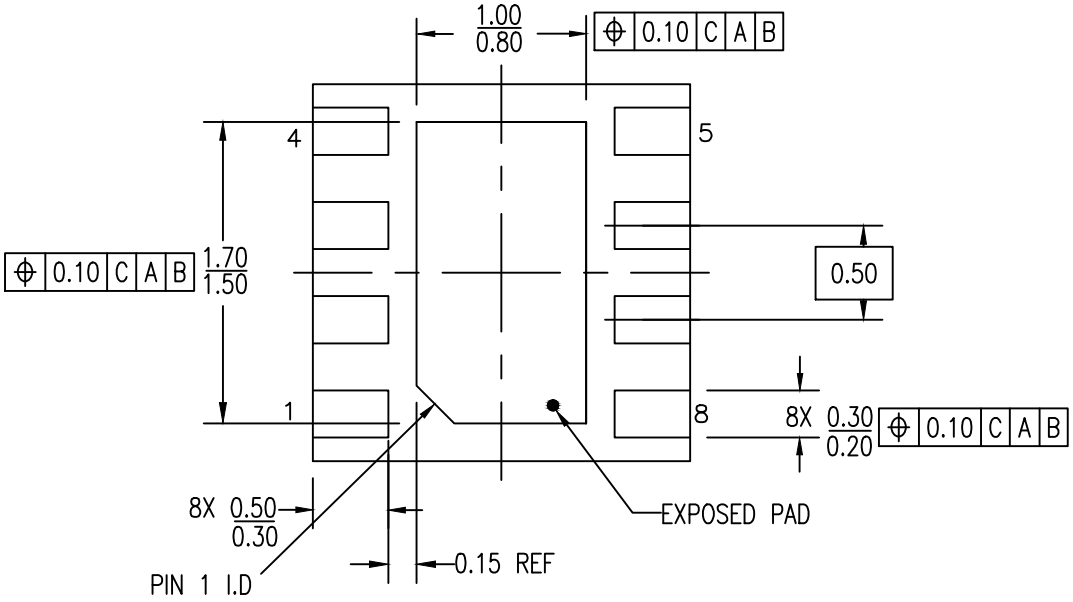
Revision Date	Description of Change
February 7, 2023	Updated POD links and disclaimer.
May 17, 2019	Updated Thermal Characteristics values.
October 3, 2018	Initial release.



TOP VIEW



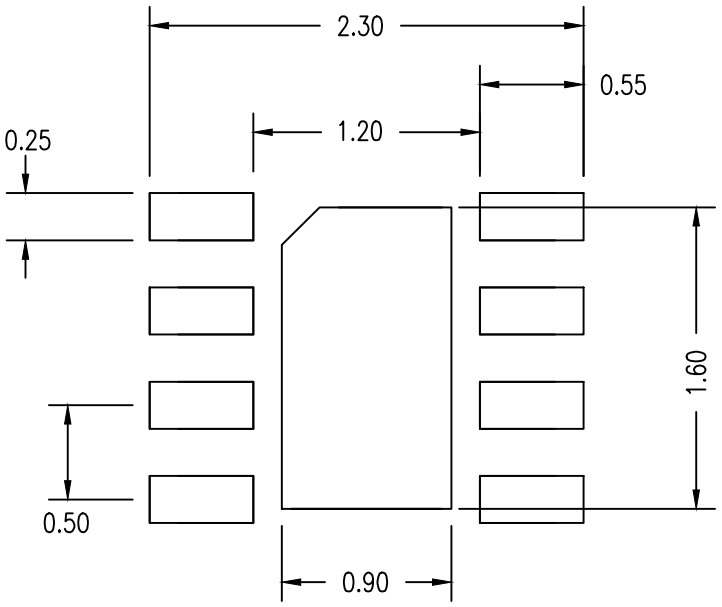
SIDE VIEW



BOTTOM VIEW

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW, AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Feb 12, 2018	Rev 01.	New Format, Change QFN to VFQFPN
April 12, 2018	Rev 02	Change from "VFQFPN" to "DFN"

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