Description

The 6V49R904-167 is a programmable clock generator with fixed ROM code intended for high-performance automotive applications.

There are four internal PLLs, each individually programmed, allowing for four unique non-integer-related frequencies. The frequencies are generated from a single reference clock.

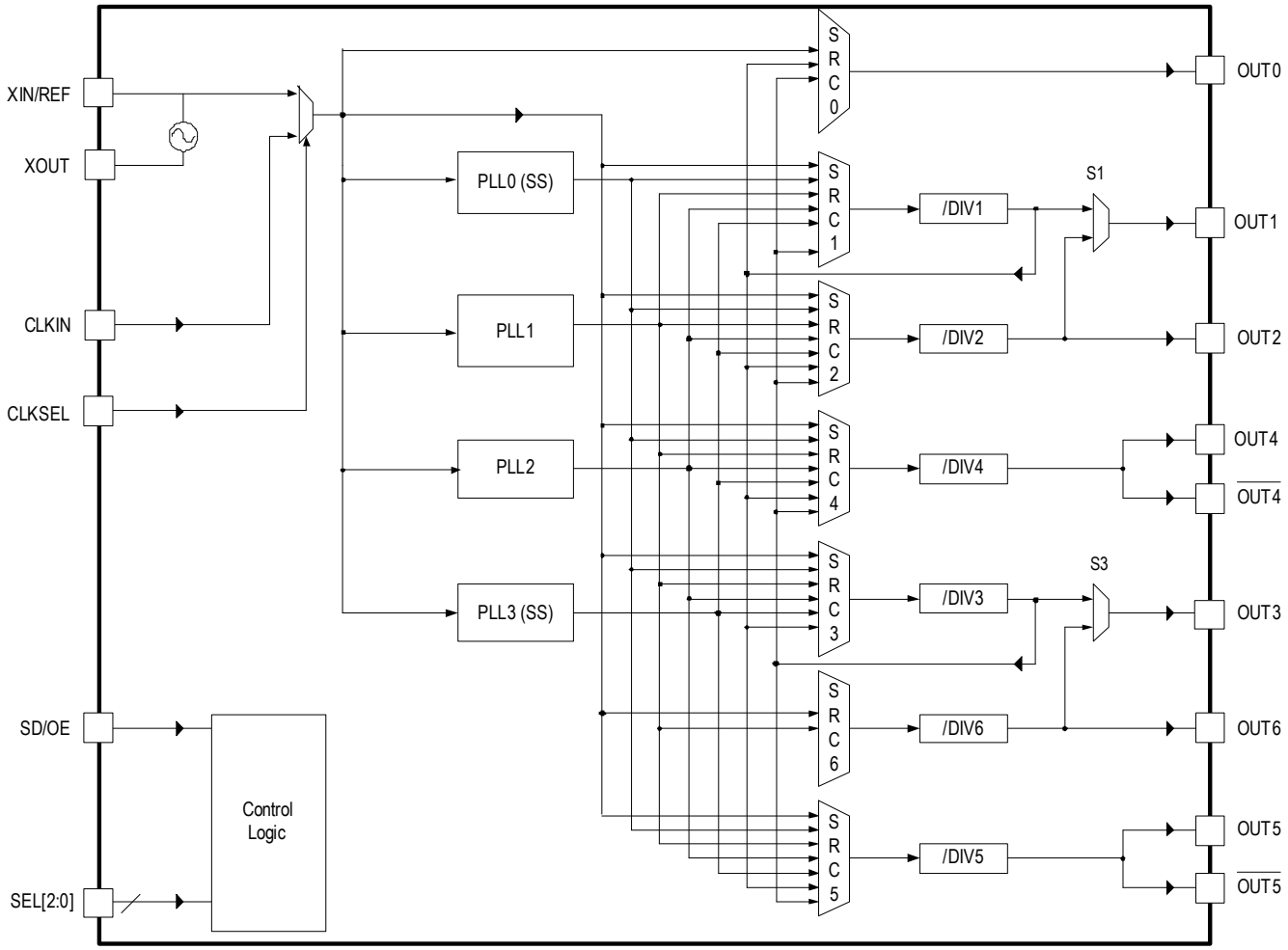
Typical Applications

- Automotive applications

Features

- Factory programmed with “6V49R904-167” programming code
- Nine programmable outputs
- Four internal PLLs
- Two of the PLLs support spread spectrum generation capability
- Four independently controlled V_{DDO} (1.8V–3.3V)
- I/O Standards:
  - Outputs: 3.3V LVTTL / LVCMOS
  - Inputs: 3.3V LVTTL / LVCMOS
- Redundant clock inputs with auto and manual switchover options
- Individual output enable/disable
- Power-down mode
- 3.3V core V_{DD}
- 5 × 5 mm 32-VFQFPN package
- -40° to +85°C industrial temperature operation

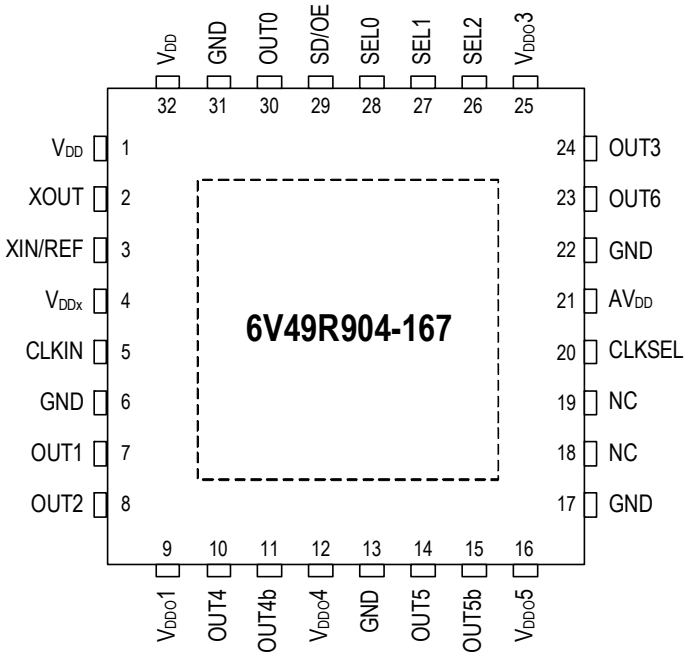
Block Diagram



Contents

Pin Assignments

Figure 1. Pin Assignments for 5 x 5 × 0.90 mm 32-VFQFPN Package – Top View



Pin Descriptions

Table 1. Pin Descriptions

Number	Name	I/O	Type	Description
1	V_{DD}		Power	Device power supply. Connect to 3.3V.
2	XOUT	O	LVTTL	CRYSTAL_OUT – reference crystal feedback.
3	XIN/REF	I	LVTTL	CRYSTAL_IN – reference crystal input or external reference clock input.
4	V_{DDx}		Power	Crystal oscillator power supply. Connect to 3.3V through 5Ω resistor. Use filtered analog power supply if available.
5	CLKIN	I	LVTTL	Input clock. Weak internal pull-down resistor.
6	GND		Power	Connect to ground.
7	OUT1	O	Adjustable	Configurable clock output 1. Output levels controlled by $V_{DDO}1$.
8	OUT2	O	Adjustable	Configurable clock output 2. Output levels controlled by $V_{DDO}1$.
9	$V_{DDO}1$		Power	Device power supply. Connect to 1.8V to 3.3V. Sets output voltage levels for OUT1 and OUT2.
10	OUT4	O	Adjustable [1]	Configurable clock output 4. Output levels controlled by $V_{DDO}4$.
11	OUT4b	O	Adjustable [1]	Configurable clock output 4b. Output levels controlled by $V_{DDO}4$.
12	$V_{DDO}4$		Power	Device power supply. Connect to 1.8V to 3.3V. Sets output voltage levels for OUT4 and OUT4b.
13	GND		Power	Connect to ground.
14	OUT5	O	Adjustable [1]	Configurable clock output 5. Output levels controlled by $V_{DDO}5$.
15	OUT5b	O	Adjustable [1]	Configurable clock output 5b. Output levels controlled by $V_{DDO}5$.
16	$V_{DDO}5$		Power	Device power supply. Connect to 1.8V to 3.3V. Sets output voltage levels for OUT5 and OUT5b.

Table 1. Pin Descriptions (Cont.)

Number	Name	I/O	Type	Description
17	GND		Power	Connect to ground.
18	NC		—	No connect.
19	NC		—	No connect.
20	CLKSEL	I	LVTTL	Input clock selector. Weak internal pull-down resistor.
21	AV_{DD}		Power	Device analog power supply. Connect to 3.3V. Use filtered analog power supply if available.
22	GND		Power	Connect to ground.
23	OUT6	O	Adjustable	Configurable clock output 6. Output levels controlled by $V_{DDO}3$.
24	OUT3	O	Adjustable	Configurable clock output 3. Output levels controlled by $V_{DDO}3$.
25	$V_{DDO}3$		Power	Device power supply. Connect to 1.8V to 3.3V. Sets output voltage levels for OUT3 and OUT6.
26	SEL2	I	LVTTL	Configuration select pin. Weak internal pull-down resistor.
27	SEL1	I	LVTTL	Configuration select pin. Weak internal pull-down resistor.
28	SEL0	I	LVTTL	Configuration select pin. Weak internal pull-down resistor.
29	SD/OE	I	LVTTL	Enables/disables the outputs or powers down the chip. See Output Selection table. Weak internal pull-down resistor.
30	OUT0	O	LVTTL	Configurable clock output 0. 3.3V LVTTL levels.
31	GND		Power	Connect to ground.
32	V_{DD}		Power	Device power supply. Connect to 3.3V.
	EPAD		Power	Connect to ground.

[1] When only an individual single-ended clock output is required, tie OUTx and OUTxb together.

[2] Analog power plane should be isolated from a 3.3V power plane through a ferrite bead.

[3] Each power pin should have a dedicated 0.01µF de-coupling capacitor. Digital V_{DD}s may be tied together.

[4] Unused clock inputs (REFIN or CLKIN) must be pulled high or low – they cannot be left floating. If the crystal oscillator is not used, XOUT must be left floating.

Output Selection

Table 2. Output Selection

SD/OE	SEL Config Setting			Input	Input Frequency (MHz)	OUT0 (MHz)	OUT1 (MHz)	OUT2 (MHz)	OUT3 (MHz)	OUT4 (MHz)	OUT4b (MHz)	OUT5 (MHz)	OUT5b (MHz)	OUT6 (MHz)	Spread %	Modulation Frequency
	2	1	0													
0	0	0	0	Crystal XO	37.007	OFF	OFF	37.007000	OFF	OFF	OFF	OFF	OFF	OFF	Center ±2.0%	36.28kHz
0	0	0	1	Crystal XO	37.007	OFF	OFF	37.007000	OFF	OFF	OFF	OFF	OFF	OFF	Center ±1.5%	36.28kHz
0	0	1	0	Crystal XO	37.007	OFF	OFF	37.007000	OFF	OFF	OFF	OFF	OFF	OFF	Center ±1.0%	36.28kHz
0	0	1	1	Crystal XO	37.007	OFF	OFF	37.007000	OFF	OFF	OFF	OFF	OFF	OFF	Center ±0.5%	36.28kHz
0	1	0	0	Crystal XO	37.007	OFF	OFF	37.007000	OFF	OFF	OFF	OFF	OFF	OFF	Center ±0.25%	36.28kHz
0	1	0	1	Xtal/ XO	37.007	OFF	OFF	37.007000	OFF	OFF	OFF	OFF	OFF	OFF	—	—
1	000–101				37.007	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	—	—
X	110–111			N/A												
Driver Type				N/A	N/A	LVTTL	LVTTL	LVTTL	LVTTL	LVTTL	LVTTL	LVTTL	LVTTL	LVTTL	—	—
V_{DDO} (V)				N/A	N/A	3.3	3.3	3.3	3.3	3.3	3.3	3.3	3.3	3.3	—	—
V_{DDO} Pin				N/A	N/A	V_{DD}	$V_{DDO}1$	$V_{DDO}1$	$V_{DDO}3$	$V_{DDO}4$	$V_{DDO}4$	$V_{DDO}5$	$V_{DDO}5$	$V_{DDO}3$	—	—

Mask ROM

On power-up of the 6V49R904-167, an automatic restore is performed to load the Mask ROM contents into the internal programming registers. The 6V49R904-167 configurations can be selected by hardware select pins SEL[2:0].

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 6V49R904-167 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
V_{DD}	Internal Power Supply Voltage	-0.5	+4.6	V
V_I	Input Voltage [1]	-0.5	+4.6	V
V_O	Output Voltage (not to exceed 4.6V) [1]	-0.5	V_{DD} + 0.5	V
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature	-65	150	°C

[1] Input negative and output voltage ratings may be exceeded if the input and output current ratings are observed.

Thermal Characteristics

Table 4. Thermal Characteristics

Symbol	Parameter	Conditions	Value	Unit
θ_{JA}	Thermal Resistance Junction to Ambient	Still air.	34	°C/W
θ_{JA}		1 m/s air flow.	29	°C/W
θ_{JA}		3 m/s air flow.	27	°C/W
θ_{JC}	Thermal Resistance Junction to Case		32	°C/W

Recommended Operating Conditions

Table 5. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}	Power Supply Voltage for V_{DD} pins supporting core and outputs	3.135	3.3	3.465	V
V_{DDX}	Power Supply Voltage for Crystal Oscillator. Use filtered analog power supply if available.	3.135	3.3	3.465	V
AV_{DD}	Analog Power Supply Voltage. Use filtered analog power supply if available.	3.135	3.3	3.465	V
V_{DDOX}	V_{DDO} Range	3.0	3.3	3.465	V
T_A	Operating Temperature, Ambient	-40		+85	°C
C_{LOAD_OUT}	Maximum Load Capacitance (3.3V LVTTL only)			15	pF
F_{IN}	External Reference Crystal		37.007		MHz
	External Reference Clock CLKIN		37.007		MHz
t_{PU}	Power-up Time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05		5	ms

Capacitance

Table 6. Capacitance

T_A = 25°C

Symbol	Parameter	Minimum	Typical	Maximum	Unit
C_{IN}	Input Capacitance (CLKIN, CLKSEL, SD/OE, SEL[2:0])		3	7	pF
Pull-down Resistor	CLKIN, CLKSEL, SD/OE, SEL[2:0]		180		kΩ
Crystal Specifications					
XTAL_FREQ	Crystal Frequency		37.007		MHz
XTAL_MIN	Minimum Crystal Load Capacitance	3.5			pF
XTAL_MAX	Maximum Crystal Load Capacitance			35.5	pF
XTAL_V_{PP}	Voltage Swing (peak-to-peak, nominal)	1.5	2.3	3.2	V

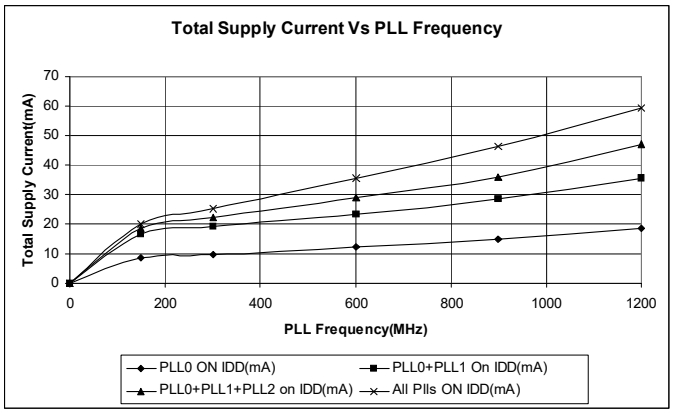
DC Electrical Characteristics

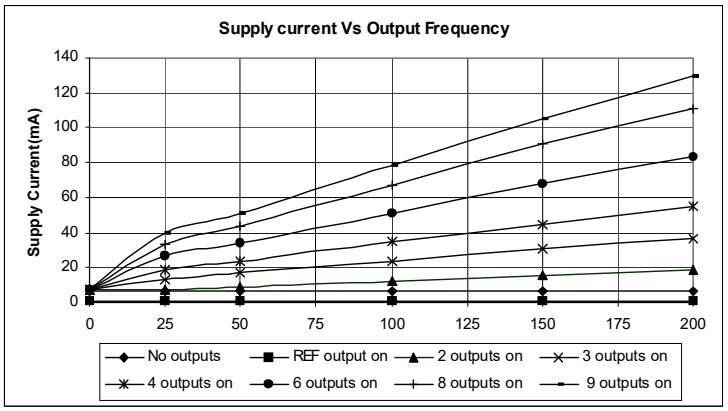
Table 7. DC Electrical Characteristics for 3.3V LVTTL [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	Output HIGH Voltage		2.4		V_{DD}	V
V_{OL}	Output LOW Voltage				0.4	V
V_{IH}	Input HIGH Voltage		2			V
V_{IL}	Input LOW Voltage				0.8	V
I_{OZDD}	Output Leakage Current	3-state outputs. V_O = V_{DD} or GND, V_{DD} = 3.465V.			10	µA

[1] See Recommended Operating Conditions table.

Power Supply Characteristics for PLLs and Outputs





AC Electrical Characteristics

Table 8. AC Timing Electrical Characteristics

(Spread spectrum generation = Off)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
f_{IN} [1]	Input Frequency	Input frequency limit (CLKIN).		37.007		MHz
		Input frequency limit (XIN/REF).		37.007		MHz
t2	Input Duty Cycle	Duty cycle for input.	40		60	%
t3	Output Duty Cycle	Measured at $V_{DD}/2$, all outputs except reference output.	45		55	%
		Measured at $V_{DD}/2$, reference output.	40		60	%
t4 [2]	Slew Rate, SLEW[1:0] = 00	Single-ended 3.3V LVCMOS output clock rise and fall time, 20% to 80% of V_{DD} (output load = 5pF).		2.5		V/ns
t5	Clock Jitter	Peak-to-peak period jitter, 1PLL, multiple output frequencies switching.		80	100	ps
		Peak-to-peak period jitter, LVCMOS, 3.3V ±5%, -40°C to +85°C.		40	300	
t6	Output Skew	Skew between output to output on the same bank.			75	ps
t7	Lock Time	PLL lock time from power-up.		10	20	ms
t8 [3]	Lock Time	PLL lock time from shutdown mode.			2	ms
t_R	Rise Time	Single-ended 3.3V LVTTL rise time, 20% to 80%.		825		ps
t_F	Fall Time	Single-ended 3.3V LVTTL fall time, 80% to 20%.		825		ps

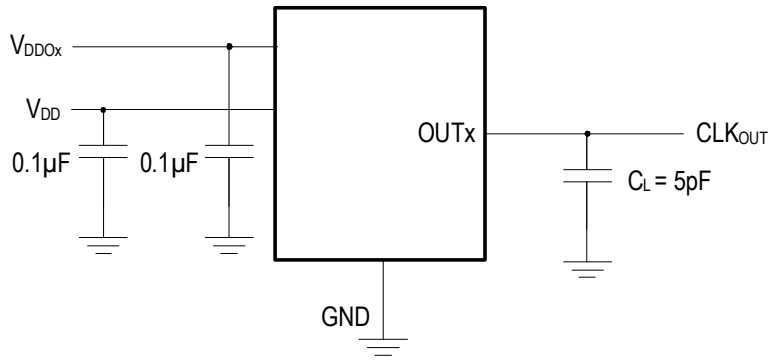
[1] Practical lower frequency is determined by loop filter settings.

[2] A slew rate of 2.75V/ns or greater should be selected for output frequencies of 100MHz or higher.

[3] Actual PLL lock time depends on the loop configuration.

Test Circuits and Conditions

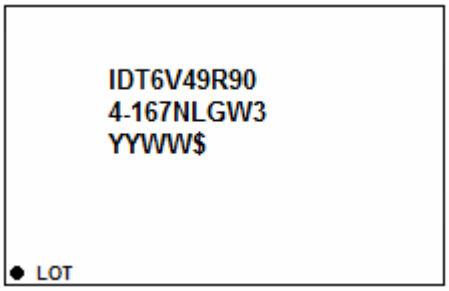
Figure 2. Test Circuits for DC Outputs



Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

Marking Diagram



- Lines 1 and 2 indicate the part number.
- Line 3 indicates the following:
  - "YY" is the last two digits of the year; "WW" is the work week number when the part was assembled.
  - "$" denotes the mark code.
- "LOT" denotes the lot number.

Ordering Information

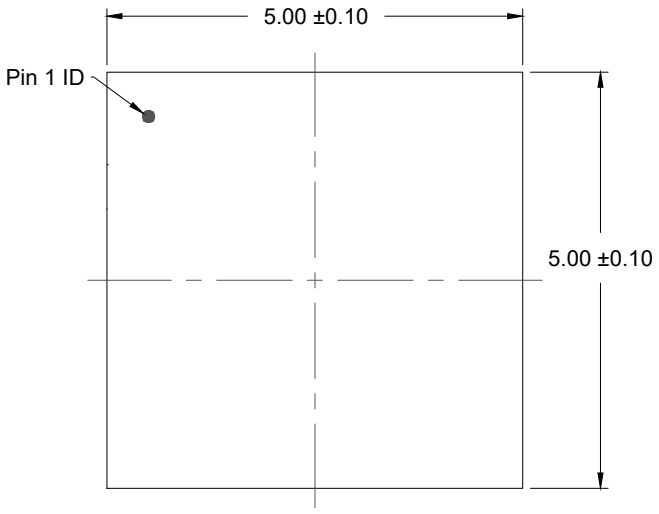
Orderable Part Number	Package	Carrier Type	Temperature Range
6V49R904-167NLGW3	5.0 × 5.0 × 0.9 mm, 0.5mm pitch 32-VFQFPN	Tray	-40° to +85°C
6V49R904-167NLGW38	5.0 × 5.0 × 0.9 mm, 0.5mm pitch 32-VFQFPN	Tape and Reel	-40° to +85°C

Revision History

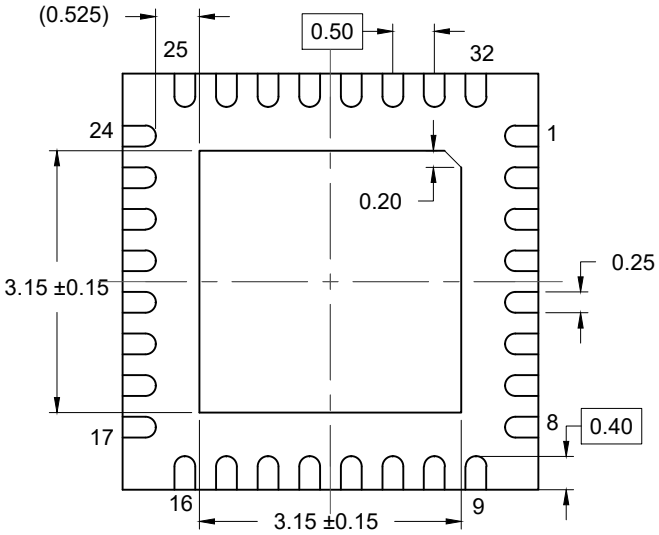
Date	Description
February 7, 2023	Updated POD links and disclaimer.
November 12, 2021	Updated Marking Diagram and Package Outline Drawings sections.
October 4, 2021	Replaced disclaimer with Renesas.
November 9, 2018	Initial release.

Package Outline Drawing

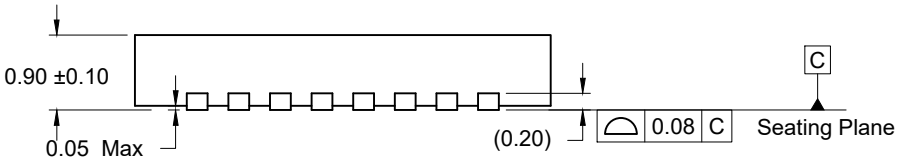
Package Code:NLG32P1
32-VFQFPN 5.0 x 5.0 x 0.9 mm Body, 0.5mm Pitch
PSC-4171-01, Revision: 04, Date Created: Aug 15, 2022



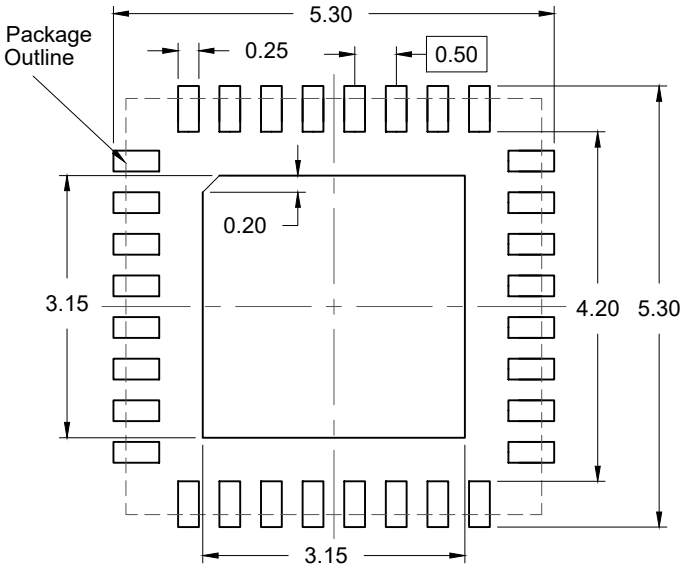
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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