71M6103/71M6113/ 71M6201/71M6203/ 71M6601/71M6603 Isolated Sensor ICs

DATA SHEET

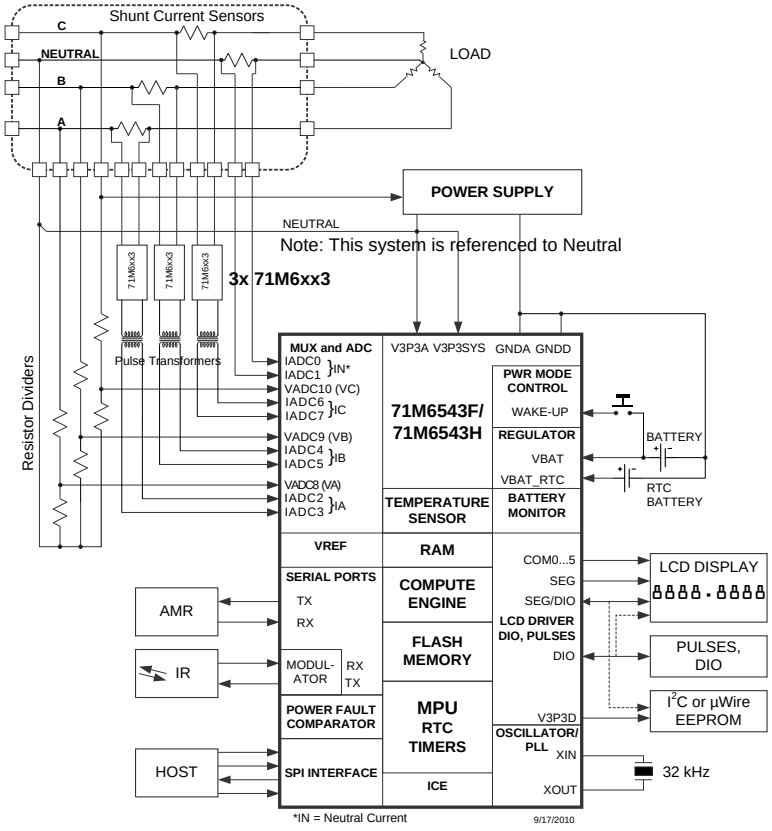
GENERAL DESCRIPTION

The 71M6103, 71M6113, 71M6201, 71M6203, 71M6601, and 71M6603 (71M6xxx) isolated sensor ICs enable Silergy/Teridian single- and polyphase-metering systems-on-chips (SoCs) to use non-isolating sensors such as resistive shunts, eliminating the need for costly isolation transformers or CTs. Isolation is provided by low-cost pulse transformers (PTs) that form a bidirectional digital communication link between the host SoC and the isolated sensor ICs. Power to the isolated sensor ICs is provided via the PTs.

The 71M6xxx isolated sensor ICs contain a 22-bit delta-sigma ADC, an amplifier with differential inputs, a precision voltage reference, a temperature sensor, and a supply voltage generator that is energized by power pulses from the host SoC.

In conjunction with the host metering SoCs, the isolated sensor ICs offer unprecedented BOM cost reduction, immunity to magnetic tampering, and enhanced reliability for single-phase and polyphase applications.

The isolated sensor ICs operate over the industrial temperature range and are available in lead (Pb)-free SOIC-8 packages.



BENEFITS AND FEATURES

- Reduce BOM by Replacing Expensive Current Transformers with Current Shunts
  - Compatible with Shunt Resistors as low as 50µΩ
- Accurate Measurement
  - 22-Bit ADC
  - On-Chip Power Monitoring
  - Exceeds IEC 62053/ANSI C12.20 Standards
- Galvanic Isolation Through Pulse Transformer Provides Power, Bidirectional Data, and Timing Reference
  - 3.3mW Typical Consumption
  - On-Chip Power Monitoring
- Compatible with 71M654x, ZON M3S/P3S, and ZON M5S/P5S SoC Families

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1 HARDWARE DESCRIPTION

The 71M6103/71M6113/71M6201/71M6203/71M6601/71M6603 (71M6xxx) remote sensor ICs integrate all functional blocks required to implement an isolated front-end with digital communication capability. Figure 1 shows the 71M6xxx IC block diagram. The chip includes the following:

- Preamplifier with a fixed gain
- 22-bit delta-sigma ADC
- ADC voltage reference
- Temperature sensor
- VCC monitor
- Power-on reset circuitry
- Bidirectional pulse interface
- Active rectifiers for supply-voltage generation from the power pulses provided by the host SoC
- Digital control section providing control registers for the selection of operation modes

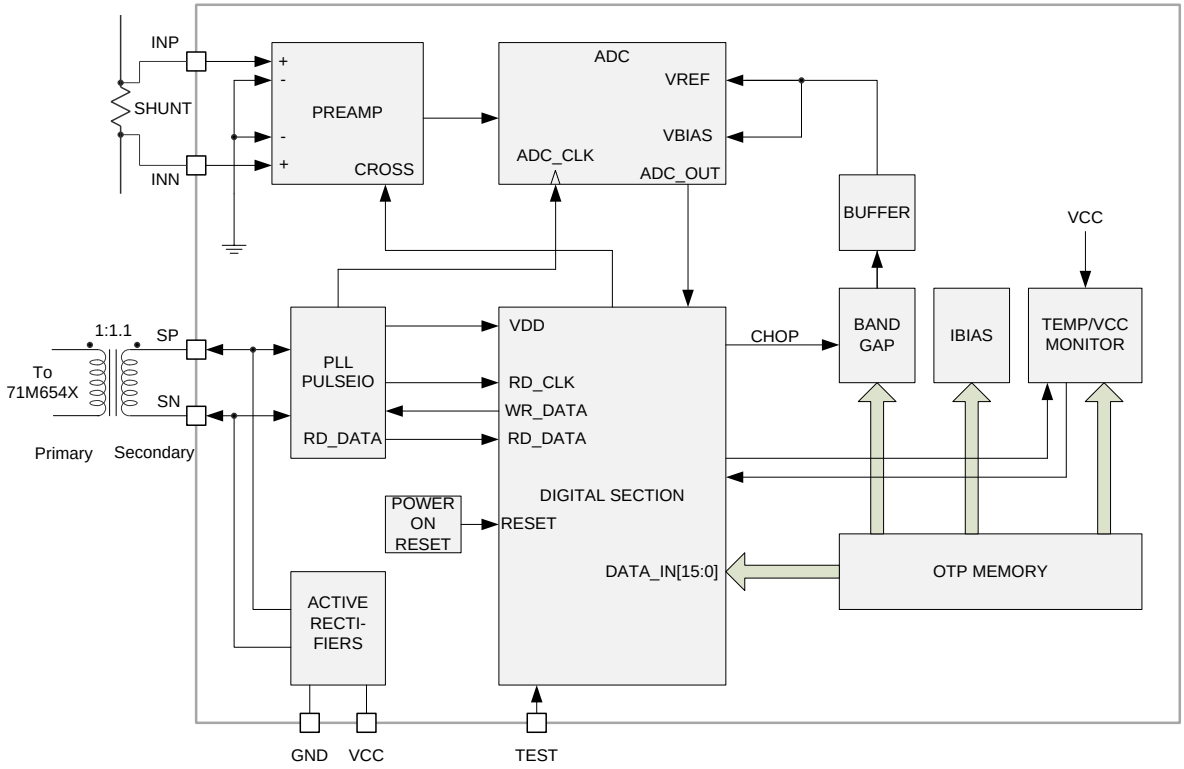


Figure 1: Block Diagram

2 FUNCTIONAL DESCRIPTION

During normal operation, the SP and SN pins of the 71M6xxx are connected to the pulse transformer. In normal operation, power pulses generated by the host SoC arrive every 610.35ns. The PLL in the host SoC locks to these incoming power pulses. The communication between the host SoC and the 71M6xxx is synchronized to the multiplexer frames of the host SoC. The communication protocol is proprietary, and details are not described in this data sheet. All aspects of the communication between the host and the 71M6xxx are managed on the hardware level and they are completely transparent to the user.

For the 71M654x SoC, the communication interface can run at two different data rates. Power pulses are generated every 610.35ns, if the *PLL_FAST* register in the 71M654x is set to 1, and every 1.905µs, if *PLL_FAST* is set to 0. The power pulses are 101.7ns wide with *PLL_FAST* = 1, and 160ns wide with *PLL_FAST* = 0.

The 71M6xxx isolated sensors provide a continuous data stream of ADC data, plus an independent data stream that contains auxiliary information as requested by the host SoC. After decimation in the host, the resulting ADC data are processed by CE Code in the host and stored in CE RAM. Auxiliary information is processed by the MPU of the host using I/O RAM registers.

Basic settings and functions of the 71M6xxx can be controlled by various I/O RAM or SFR registers in the host. For example, for the 71M654x, the command sent towards the 71M6xxx is placed in the *RCMD[4:2]* register, with further specification contained in the *TMUXRn[2:0]* register. Data from the 71M6xxx are placed in the *R6K_RD[15:0]* register. Refer to the data sheet or HRM of the host SoC for details.

Table 1 shows the allowable combinations of values in *RCMD[4:2]* and *TMUXRn[2:0]*, and the achieved operation along with the type and format of data sent back by the 71M6xxx isolated sensors.

Table 1: Remote Interface Commands

RCMD[4:2]	***TMUXRn [2:0]***	**Code**	**Read Operation/Command**	***R6K_RD* [15:0]**
001	00X	0x10	Chip-characteristic temperature data	*TRIMT* (see note), use bits [8:1]
001	01X	0x14		*TRIMBGC* (see note), use bits [15:6]
001	10X	0x18		*TRIMBGA* (see note), use bits [15:8]
001	11X	0x1A		*TRIMBGB* bits [15:8], *TRIMBGD* bits [7:0] (see note)
010	00X	0x20	Temperature	Output of the temperature sensor, bits [10:0]
010	01X	0x24	Supply voltage	Supply voltage measurement, bits [7:0]
010	10X	0x28	Chip version	Chip version code, use bits [15:8]
100	000	0x40	Voltage at NC Pin	Command for floating the NC pin (5)
110	111	0x6E	Reset	—

Note: *TRIMBGA to TRIMBGD and TRIMT are values used for characterizing the individual 71M6xxx over temperature. Availability of TRIMBGA to TRIMBGD and TRIMT depends on the part number (see Table 10 for details).*

The remote interface commands listed in Table 1 enable the host SoC to gather the following information from the 71M6xxx:

- Output of the temperature sensor
- Information on how the device is characterized over temperature
- Supply voltage
- Chip version code

The remote interface commands listed in Table 1 are also used to initiate the following actions in the 71M6xxx:

- Read the 71M6xxx temperature sensor
- Read the 71M6xxx VCC sensor
- Hardware reset

With hardware and temperature characterization information on each connected 71M6xxx isolated sensor available to the host SoC, temperature compensation of the energy measurement can be implemented based on the individual temperature characteristics of the 71M6xxx isolated sensors. For example, when the 71M6xxx SoCs are used in a polyphase meter containing three shunt resistors, the temperature increase in each 71M6xxx can be monitored and used to compensate for the temperature coefficient of the 71M6xxx VREF and the corresponding shunt resistor.

3 APPLICATIONS INFORMATION

3.1 Product Selection

A low-noise differential-input preamplifier applies gain to the signal from the current sensor to the optimal input range of the ADC. The current sensor is connected to the inputs of the preamplifier through INP and INN. The output of the preamplifier connects directly to the input of the ADC. See section 5 Ordering Information for available part types. Shunt resistances from 736μΩ to as low as 50μΩ can be accommodated, depending on desired current range and part type.

The shunt resistance must be balanced with the maximum current range of the part type, as shown in Table 2. Various combinations of current ranges and shunt resistance values are possible. However, the shunt resistance for a given current must be chosen carefully as not to exceed the maximum RMS voltage at the INP/INN pins of the 71M6xxx. The maximum wattage of the shunt resistor is another consideration that applies to the resistance range of the shunt.

Products vary in the magnitude of the internal gain and in the number of internal trim registers that are accessible to the host SoC (see Table 10). Populated trim registers in the higher-grade products allow for more accurate modeling of the internal reference voltage over temperature, and therefore result in a tighter temperature coefficient after compensation in the host SoC (up to ±15PPM/°C for the 71M6201 and 71M6203).

Table 2: Product Variations

Part	Application[1]	Maximum Current (A)	Accuracy Class[2] (%)	Maximum RMS Voltage at INP/INN (mV)	Maximum Shunt Resistance[3] (μΩ)	Shunt Power[4] (W)	Typical Shunt Resistance[5] (μΩ)
71M6601	S	60	1	44	736	1.44	400
71M6603	P		1				
71M6103	P	100	1	19.6	196	1.2	120
71M6113			0.5				
71M6201	S	200	0.2	12.6	63	2.0	50
71M6203	P		0.2				

Note 1: S = single phase, P = polyphase.
Note 2: Accuracy over temperature (-40°C to +85°C for 71M620x parts, -20°C to +60° for all other parts), when combined with accuracy of host SoC.
Note 3: Maximum resistance at maximum current.
Note 4: Power at maximum current and typical shunt resistance.
Note 5: Typical resistance values provide room for overhead while maintaining optimum dynamic range.

The inputs of the preamplifier are referenced to local ground (the GND pin of the 71M6xxx). This means that in an isolated system, the INP and INN pins must be biased towards this local GND. See 3.2.1 Current Sensor Side for details.

3.2 External Components for the 71M6xxx

3.2.1 Current Sensor Side

Figure 2 shows the external components required for the 71M6xxx. It is recommended to use the following components:

- 1.0μF capacitor between the GND and VCC pins. This capacitor minimizes the VCC ripple voltage.
- One 1kΩ resistor each from the sensor output pins to GND. These resistors help to bias the input voltage at the INP and INN pins towards GND.
- In environments where EMC is a concern, ferrite beads can be placed between the sense pins of the shunt resistor and the INP/INN pins of the 71M6xxx.

In-line resistors between shunt and the INP/INN pins of the 71M6xxx are not recommended, since they will reduce the gain.

3.2.2 Pulse Transformer

A low-cost pulse transformer is used for the link between the host SoC and the 71M6xxx. It is the responsibility of the meter system designer to qualify the transformer used in the system over the required operating temperature range, operating voltage, and for suitability for the magnetic environment. The following commercially available transformers are suitable for this application:

- Würth Electronics Midcom Inc. (www.weonline.com), P/N 750-110-056 (ferrite), P/N 750-317-553 (MPP), P/N 750-110-133 (ferrite, double insulation)
- Palnova (www.palpilot.com), P/N PS1695M (MPP), P/N 1694 (Hi-Flux)

Cores with higher saturation flux density, such as MPP or Hi-Flux offer higher resistance to magnetic tampering over regular ferrite cores.

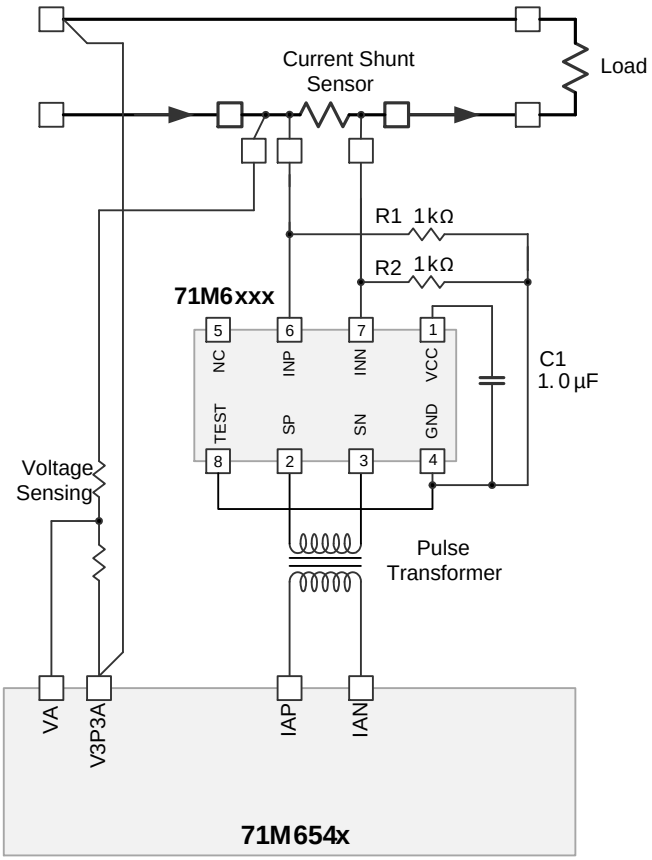


Figure 2: External Components (Host SoC 71M654x)

3.3 Connections to Sensors and to the Host SoC

Figure 3 shows the sensor connections for single-phase meter application using a 71M6541D/F and 71M6x01. This single-phase configuration uses one local shunt and one shunt isolated with a 71M6x01 device. Since the local shunt is connected to the LINE circuit, the meter is also referenced to the LINE circuit.

Figure 4 shows the sensor connections for a polyphase meter application using a 71M6543F/H or 71M6545/H. This polyphase configuration uses three 71M6xx3 to isolate the shunt sensors for the three phases, while a locally connected fourth shunt sensor can be optionally used to sense neutral current. Since the local shunt is connected to the neutral circuit, the meter is also referenced to the neutral circuit.

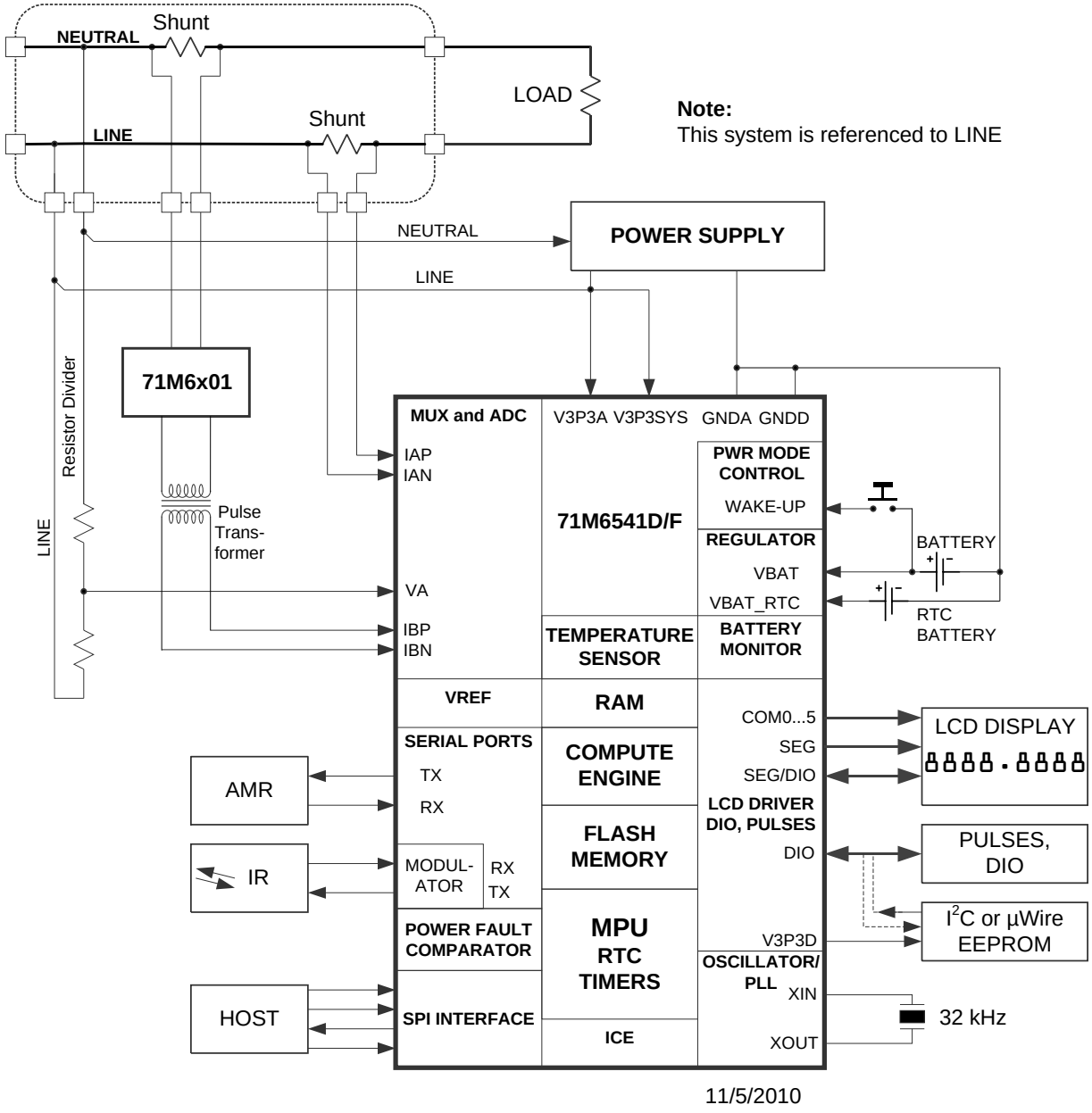


Figure 3: Current Sensors Connected to the 71M6541D/F Using One 71M6x01

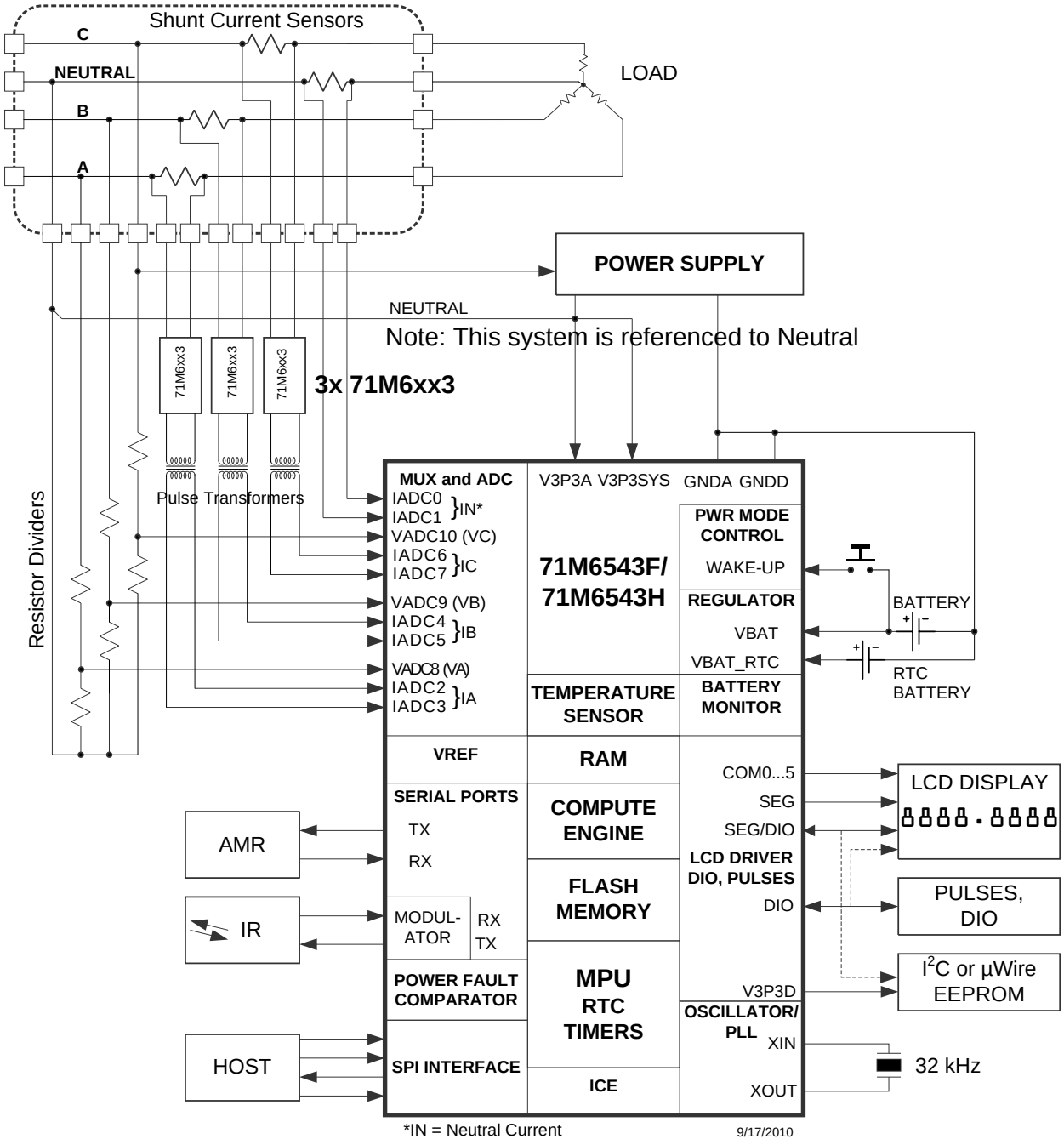


Figure 4: Current Sensors Connected to the 71M6543F/H or 71M6545/H with Three 71M6xx3

3.4 PCB Layout Considerations

To limit emissions and susceptibility to electromagnetic and magnetic fields, the signal wiring between the shunt resistors and the 71M6xxx should be as short as possible and should consist of tightly twisted pair cable. Similarly, the PCB traces between the 71M6xxx and the host SoC should be routed as short as possible and should be surrounded by grounded copper structures. The trace pairs should be routed as close to each other as permitted by the PCB manufacturer.

The copper separation (gap) between the shunt side and the host SoC side of the signal transformer should be as wide as permitted by the footprint of the transformer, as shown in Figure 5.

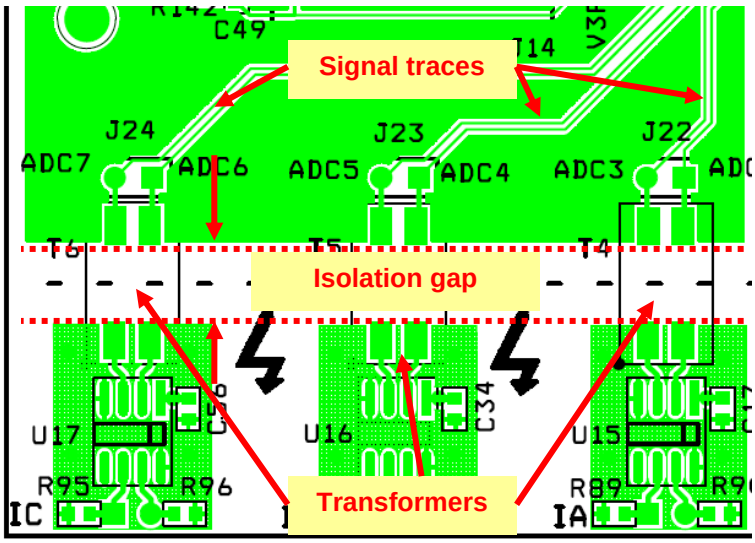


Figure 5: Copper Separation and Signal Traces for a Polyphase PCB

3.5 Compatibility with the Host SoC

The 71M6xxx isolated sensor ICs are designed to be operated in conjunction with the 71M654x, ZON M3S/P3S, or ZON M5S/P5S energy metering ICs. Operation of the 71M6xxx isolated sensor ICs requires a host SoC with CE Code capable of interfacing with the 71M6xxx. Check with your Silergy representative for the applicable CE Code.

The 71M6xxx isolated sensor ICs are not arbitrarily interchangeable. Each type of the 71M6xxx must be matched with its corresponding CE Code in the host SoC per Table 14. A 71M6xxx remote sensor IC generates unpredictable results when paired with a CE Code for a different part number. All 71M6xxx isolated sensor ICs used in a polyphase system must be of the same part number.

4 SPECIFICATIONS

4.1 Absolute Maximum Ratings

Table 3 shows the absolute maximum ranges for the device. Stresses beyond Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation at these or any other conditions beyond those indicated under recommended operating conditions (4.3 Recommended Operating Conditions) is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability. All voltages are with respect to GND.

Table 3: Absolute Maximum Ratings

SUPPLIES AND GROUND PINS:	
VCC	-0.5V to 4.6V
GND	-0.1V to +0.1V
ANALOG INPUT PINS:	
INP, INN, SP, SN	-10mA to +10mA, -0.5V to (VCC + 0.5V)
TEMPERATURE:	
Operating Junction Temperature (Peak, 100ms)	+140°C
Operating Junction Temperature (Continuous)	+125°C
Storage Temperature Range	-45°C to +165°C
Soldering Temperature (10s duration)	+250°C

4.2 Recommended External Components

Table 4: Recommended External Components

NAME	FROM	TO	FUNCTION	VALUE	UNITS
C1	VCC	GND	Bypass capacitor for supply	1.0	µF
R1, R2	Sensor	GND	To establish proper bias for INP/INN pins	1	kΩ

4.3 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCC Supply Voltage		2.5		3.6	V
Operating Temperature Range		-40		+85	ºC

4.4 Performance Specifications

Unless otherwise specified, all parameters listed in this section are valid over the Recommended Operating Conditions provided in Table 5**.**

4.4.1 Supply Current

Table 6: Supply Current Performance Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCC Current, Normal Operation	VCC = 3.3V		0.77	1.05	mA

4.4.2 Power and Data Pulses

Table 7: Timing Specifications for Power and Data Pulses

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Pulse Frequency	Normal operation		1.638		MHz
	Low speed, e.g. 71M654x (*PLL_FAST* = 0)		0.5249		

4.4.3 VCC Voltage Monitor

Table 8: VCC Voltage Monitor Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
BNOM: Nominal Value, T_A = +22°C	VCC = 3.2V		138		LSB
VCC Voltage (**Note:** This is a definition—it is not a measured quantity.)	VCC = 3.195 + (BSENSE - 138) x 0.0246 + STEMP x 0.000104				V
BE: Measurement Error VCC = 3.195 + (BSENSE - 138) x 0.0246 + STEMP x 0.000104	VCC = 2.5V	-5		+5	%
	VCC = 2.8V to 3.6V	-5		+5	

4.4.4 Temperature Sensor

Table 9: Temperature Sensor Specifications

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
TNOM: Nominal Value, T_A = +22°C	VCC = 3.2V			870		LSB
Temperature Equation for: 71M6601, 71M6603, 71M6103 and 71M6113 (*TRIMBGA* = 0) (**Note:** This is a definition—it is not a measured quantity.)	$\boldsymbol{TEMP = STEMP \cdot 0.33 - STEMP^2 \cdot 3 \cdot 10^{-5} + 22}$					ºC
Temperature Equation for: 71M6201 and 71M6203 (*TRIMBGA* accessible) (**Note:** This is a definition—it is not a measured quantity.)	If STEMP < 0: $\boldsymbol{TEMP = STEMP \cdot 0.33 - STEMP^2 \cdot 3 \cdot 10^{-5} + 22}$ If STEMP ≥ 0: $TEMP = \frac{STEMP \cdot 63}{TRIMBGA} + 22$					ºC
Temperature Error (Note 1)	Temperature = -40°C, -10°C, +55°C, +85°C	VCC = 2.8V to 3.6V	-5		+5	ºC
		VCC = 2.5V to 2.79V	-6.5		+6.5	
TETIME: Duration of Temperature Measurement	VCC = 3.0V			15	30	ms

Note 1: Guaranteed by design; not production tested.

4.4.5 VREF Performance Specifications

Table 10 shows the performance specifications for the ADC reference voltage (VREF).

Table 10: VREF Performance Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VREF Output Voltage	71M6201, 71M6203, 71M6113: T_A = +22°C	1.193	1.195	1.197	V
	71M6601, 71M6603, 71M6103: T_A = +22°C	1.180	1.195	1.210	
VREF Output Impedance	I_{LOAD} = 10µA, -10µA on TMUXOUT		8		kΩ
VREF Power-Supply Sensitivity: ΔVREF/ΔVCC	VCC = 2.8V to 3.6V	-1.5		+1.5	mV/V
	VCC = 2.5V to 3.6V	-2		+2	
VREF Chop Step (Trimmed)	VREF(CROSS = 1) - VREF(CROSS = 0)	-22	0	+22	mV
VNOM Definition	VNOM(T) = VREF(22) + (T - 22)TC1 + (T - 22)^{2}TC2				V
71M6201 and 71M6203 (0.2% ACCURACY CLASS) – *TRIMT*, *TRIMBGB*, *TRIMBGD* accessible					
VNOM Temperature Coefficients: TC1, TC2	TC1 = 0.0538 x *TRIMT* + 1.587(*TRIMBGB* - *TRIMBGD*) + 27.279				µV/°C
	TC2 = -0.433 - *TRIMT* x 0.000854				µV/°C^2
VREF(T) Deviation from VNOM(T) (Note 1)	$\frac{VREF(T)-VNOM(T)}{VNOM(T)}\frac{10^6}{62}$	-15		+15	ppm/°C
71M6113 (0.5% ACCURACY CLASS) – *TRIMT* accessible, *TRIMBGB* = *TRIMBGD* = 0					
VNOM Temperature Coefficients: TC1, TC2	TC1 = 251 - *TRIMT* x 4.60				µV/°C
	TC2 = -0.433 - *TRIMT* x 0.000854				µV/°C^2
VREF(T) Deviation from VNOM(T) (Note 1)	$\frac{VREF(T)-VNOM(T)}{VNOM(T)}\frac{10^6}{62}$	-50		+50	ppm/°C
71M6601, 71M6603, and 71M6103 (1% ACCURACY CLASS) – *TRIMT* = 0					
VNOM Temperature Coefficients: TC1, TC2	TC1 = -34.8				µV/°C
	TC2 = -0.599				µV/°C^2
VREF(T) Deviation from VNOM(T) (Note 1)	$\frac{VREF(T)-VNOM(T)}{VNOM(T)}\frac{10^6}{45}$	-100		+100	ppm/°C

Note 1: Guaranteed by design; not production tested.

4.4.6 ADC Converter

Table 11: ADC Converter Specifications

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Current	INP and INN at GND potential	INP		22		µA
		INN		22		
THD (First 10 Harmonics)	VIN = 65Hz, 64kpts FFT, Blackman-Harris window			-85		dB

4.5 Typical Performance Data

Examples for Wh and VARh load lines are shown below. Measurements were taken with a 71M6543 host SoC under realistic metering conditions.

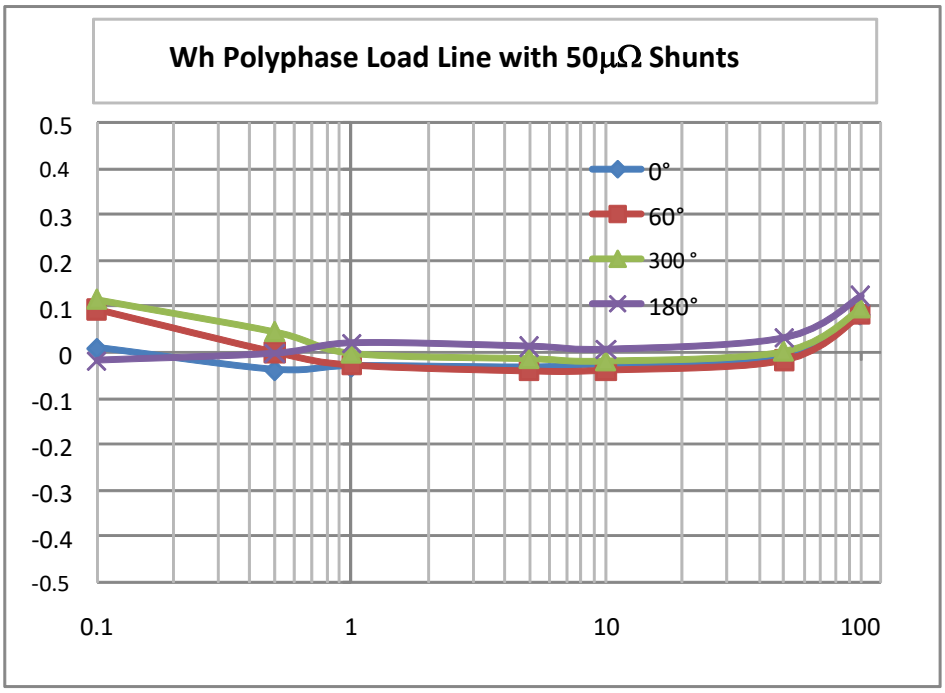


Figure 6: Wh Error at Room Temperature (71M6203, 100A/0.1A, 60Hz/240V AC)

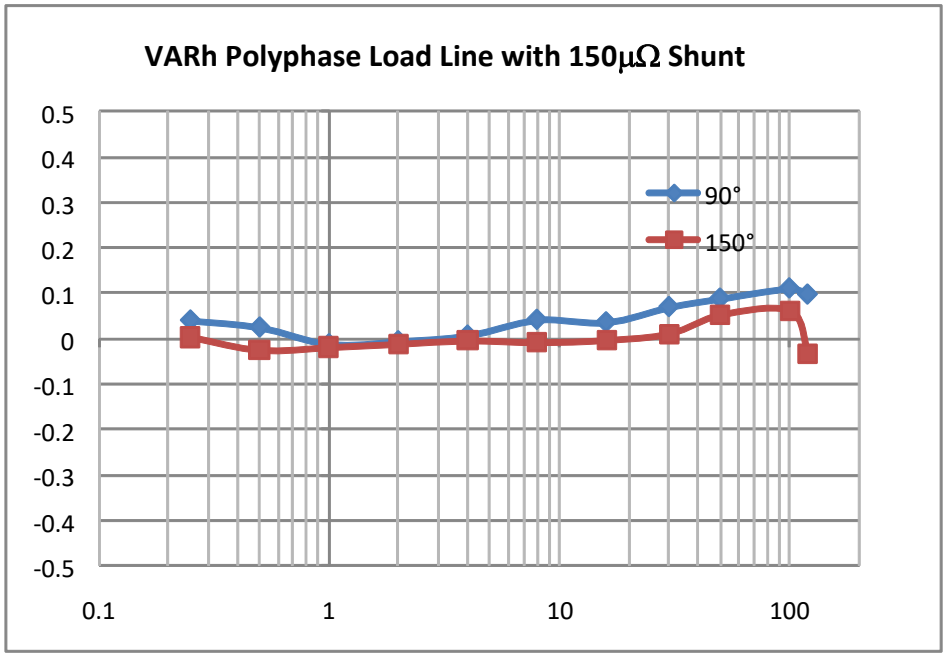
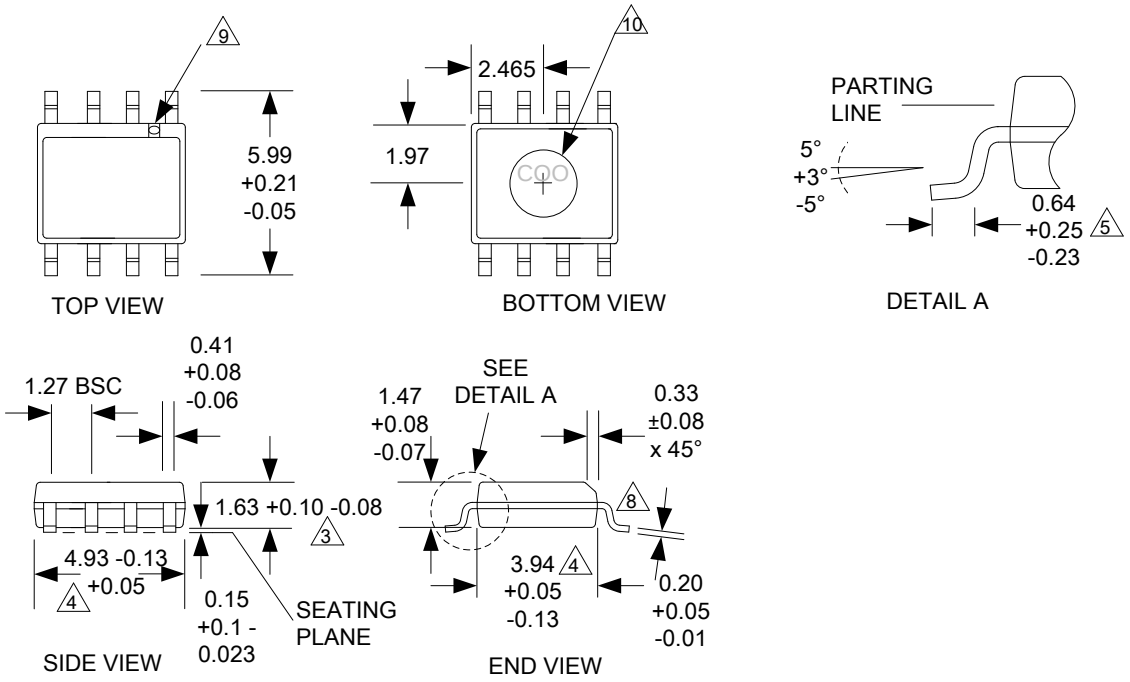


Figure 7: VARh Error at Room Temperature (71M6203, 100A/0.1A, 60Hz/240V AC)

4.6 Package Outline Drawing

Controlling dimensions are in mm.



NOTES:

3 REFERENCE DATUM

4 LENGTH AND WIDTH ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT INCLUDE MOLD MISMATCH. MEASURED AT THE MOLD PARTING LINE. PROTRUSIONS DO NOT EXCEED 0.1524 mm AT END AND 0.254 mm AT WINDOW.

5 LENGTH OF TERMINAL FOR SOLDERING TO SUBSTRATE

8 FORMED LEADS ARE PLANAR WITH RESPECT TO EACH OTHER WITHIN 0.735 mm AT SEATING PLANE.

9 THE APPEARANCE OF PIN #1 I.D. IS OPTIONAL.

10 COUNTRY OF ORIGIN LOCATION ON PACKAGE BOTTOM IS OPTIONAL AND DEPENDS ON ASSEMBLY LOCATION.

PACKAGE IS COMPLIANT WITH JEDEC STANDARD MS-012.
DIMENSIONING AND TOLERANCES PER ANSI Y14.5 M - 1982

Figure 8: SOIC-8 Package Outline

4.7 IC Pinout

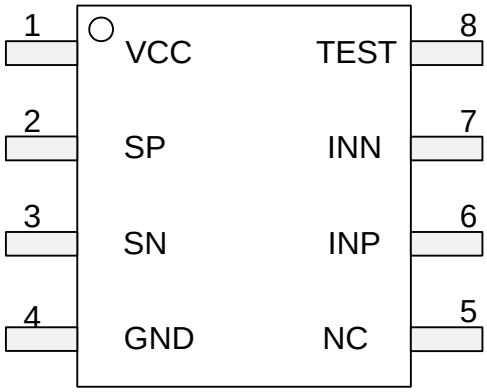


Figure 9: Pinout for SOIC-8 Package

4.8 Pin Description

Table 12: Pin Description

PIN	NAME	FUNCTION
1	VCC	Supply Voltage Output. A 1.0µF capacitor to GND should be provided.
2	SP	Positive Bidirectional Communication Port for the Connection of the Pulse Transformer
3	SN	Negative Bidirectional Communication Port for the Connection of the Pulse Transformer
4	GND	Ground (Local Ground). The voltage at the INP and INN pins references to this pin.
5	NC	No Connection. No connections must be made to this pin. Remote Interface Command 0b100 XXX will apply internal voltages to this pin.
6	INP	Positive Analog Input from Sensor. This input must be biased towards GND with a 1kΩ resistor.
7	INN	Negative Analog Input from Sensor. This input must be biased towards GND with a 1kΩ resistor.
8	TEST	Input Used in Factory for Test Purposes. This pin must be connected to GND.

5 ORDERING INFORMATION

Table 13: Product Variations

PART	APPLICA-TION	RATED CURRENT (A)	MAX INPUT VOLTAGE at INP-INN PINS (mV)	TEMP RANGE (°C)	TYPICAL OPERATING TEMP RANGE (°C)	RECOMMEND-ED METER ACCURACY CLASS (%)	MAX SHUNT RE-SISTANCE (µΩ)
71M6601	1-phase	60	44	-40 to +85	-20 to +60	1	736
71M6603	3-phase						
71M6103	3-phase	100	19.6		-20 to +60	1	196
71M6113	3-phase					0.5	
71M6201	1-phase	200	12.6		-40 to +85	0.2	63
71M6203	3-phase						

Table 14: Packaging Information, Corresponding CE Codes, and Ordering Numbers

PART	TEMP RANGE	PIN-PACKAGE	71M654x CE Code †
71M6601-IL/F	-40°C to +85°C	SOIC-8	EQU0-60
71M6601-ILR/F			EQU0-60
71M6603-IL/F			EQU5-60
71M6603-ILR/F			EQU5-60
71M6103-IL/F			EQU5-100
71M6103-ILR/F			EQU5-100
71M6113-IL/F			EQU5-100
71M6113-ILR/F			EQU5-100
71M6201-IL/F			EQU1-200, EQU2-200
71M6201-ILR/F			EQU1-200, EQU2-200
71M6203-IL/F			EQU5-200
71M6203-ILR/F			EQU5-200

F = Lead(Pb)-free/RoHS-compliant package.
R = Tape and reel (2,500 pcs./reel). Parts without R are bulk parts in tubes (100 pcs./tube).
† Check with Silergy for suitable CE Codes to be used with the ZON M3S/P3S or M5S/P5S

6 RELATED INFORMATION

The following documents related to the 71M6xxx are available from Silergy:

71M6543F/H Data Sheet
71M6541D/F-71M6542F Data Sheet
71M6545/H Data Sheet
ZON M3S/P3S Data Sheet
ZON M5S/P5S Data Sheet

7 CONTACT INFORMATION

For technical support or more information about Silergy products, contact support.metering@silergy.com

REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/2010	Initial release	—
1	3/2011	Figure 1, page 4 (transformer turns ratio 1:1.1) Table 9, page 12 Table 14, page 18	4, 12, 18
2	6/2011	Removed future status from the 71M6113 parts in Table 14	18
3	12/2012	Removed future status from the 71M6201/71M6203 parts in Table 14	18
4	1/2015	Updated the *Benefits and Features* section	1
5	4/2016	Rebranding only	All
6	5/2020	Changed logo on title page (Silergy ®) Extended list of compatible host SoCs Added float NC pin command in Table 1 Added note about in-line resistors in 3.2.1 Updated list of pulse transformers Updated formulae in 4.4.4 Stated relation between trim register accessibility and part type Updated NC pin description in Table 12 Unified package description (SOIC-8) Replaced *71M654x* with host SoC, where applicable Changed company name to Silergy Corp.	1 1 5 6 7 12 12, 13 17 17, 18 All All