73K222AU
Single-Chip Modem with UART

DATA SHEET

JULY 2005

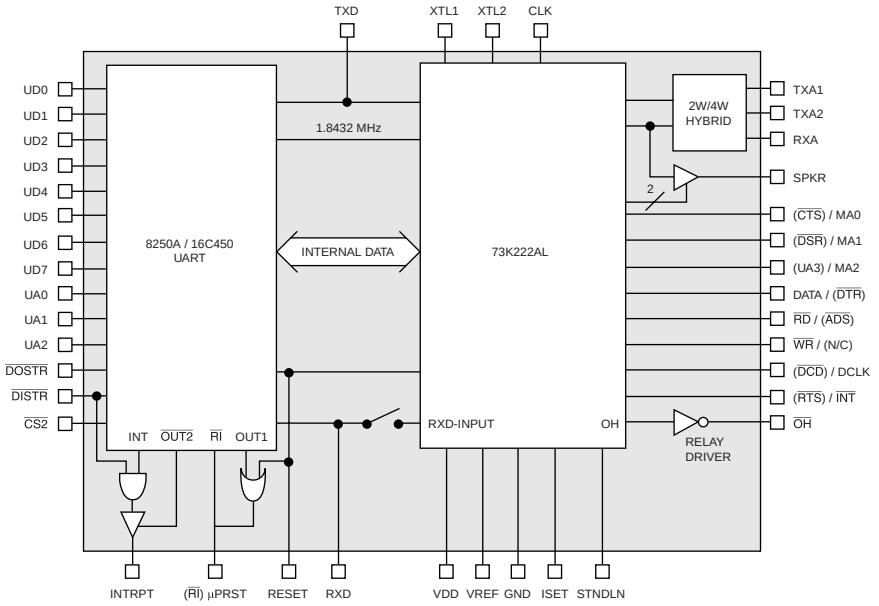
DESCRIPTION

The 73K222AU is a compact, high-performance modem, which includes an 8250A/16C450 compatible UART with the 1200 bit/s modem function on a single chip. Based on the 73K222L 5V low power CMOS modem IC, the 73K222AU is the perfect modem/UART component for integral modem applications. It is ideal for applications such as portable terminals and laptop computers. The 73K222AU is the first fully featured modem IC that can function as an intelligent modem in integral applications without requiring a separate dedicated microcontroller. It provides for data communication at 1200, 600, and 300 bit/s in a multi-mode manner that allows operation compatible with both Bell 212A/103 and CCITT V.22/V.21 standards. The digital interface section contains a high-speed version of the industry standard 8250A/16C450 UART, commonly used in personal computer products. A unique feature of the 73K222AU is that the UART section can be used without the modem function, providing an additional asynchronous port at no added cost. The 73K222AU is designed in CMOS technology and operates from a single +5V supply. Available packaging includes 40-pin DIP or 44-pin PLCC for surface mount applications.

FEATURES

- **Modem/UART combination optimized for integral bus applications**
- **Includes features of 73K222L single-chip modem**
- **Fully compatible 16C450/8250 UART with 8250B or 8250A selectable interrupt emulation**
- **High speed UART will interface directly with high clock rate bus with no wait states**
- **Single-port mode allows full modem and UART control from CPU bus, with no dedicated microprocessor required**
- **Dual-port mode suits conventional designs using local microprocessor for transparent modem operation**
- **Complete modem functions for 1200 bit/s (Bell 212A, V.22) and 0-300 bit/s (Bell 103, V.21)**
- **Includes DTMF generator, carrier, call-progress and precise answer-tone detectors for intelligent dialing capability**
- **On chip 2-wire/4-wire hybrid driver and off-hook relay buffer**
- **Speaker output with four-level software driven volume control**
- **Low power CMOS (40 mW) with power down mode (15 mW)**
- **Operates from single +5V supply**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The 73K222AU integrates an industry standard 8250/16C450 UART function with the modem capability provided by the 73K222L single chip modem IC. The 73K222AU is designed specifically for integral microprocessor bus intelligent modem products. These designs typically require the standard 8250 or higher speed 16450 UART to perform parallel-to-serial and serial-to-parallel conversion process necessary to interface a parallel bus with the inherently serial modem function. The 73K222AU provides a highly integrated design, which can eliminate multiple components in any integral bus modem application, and is ideal for internal PC modem applications.

The 73K222AU includes two possible operating modes. In the dual-port mode, the device is suitable for conventional plug-in modem card designs, which use a separate local microprocessor for command interpretation and control of the modem function. In this mode, a dedicated microcontroller communicates with the 73K222AU using a separate serial command port. In the single-port mode the main CPU can control both the UART and modem function using the parallel data bus. This allows very efficient modem design with no local microprocessor required for dedicated applications such as laptop PC's or specialized terminals.

To make designs more space efficient, the 73K222AU includes the 2-wire to 4-wire hybrid drivers, off-hook relay driver, and an audio monitor output with software volume control for audible call progress monitoring. As an added feature the UART function can be used independent of the modem function, providing an added asynchronous port in a typical PC application with no additional circuitry required.

UART FUNCTION (16C450)

The UART section of the 73K222AU is completely compatible with the industry standard 16C450 and the 8250 UART devices. The bus interface is identical to the 16450, except that only a single polarity for the control signals is supported. The register contents and addresses are also the same as the 16C450. To insure compatibility with all existing releases of the 8250 UART design, external circuitry normally used in PC applications to emulate 8250B or 8250A interrupt operation has been included on the 73K222AU. A select line is then provided to enable the desired interrupt operation.

The UART used in the 73K222AU can be used with faster bus read and write cycles than a conventional 16C450 UART. This allows it to interface directly with higher clock rate microprocessors with no need for external circuitry to generate wait states.

The primary function of the UART is to perform parallel-to-serial conversion on data received from the CPU and serial-to-parallel conversion on data received from the internal modem or an external device. The UART can program the number of bits per character, parity bit generation and checking, and the number of stop bits. The UART also provides break generation and detection, detection of error conditions, and reporting of status at any time. A prioritized maskable interrupt is also provided.

The UART block has a programmable baud rate generator, which divides an internal 1.8432 MHz clock to generate a clock at 16 x the data rate. The data rate for the transmit and receive sections must be the same. For DPSK modulation, the data rate must be 1200 Hz or 600 Hz. For FSK modulation, the data rate must be 300 Hz or less. The baud generator can create a clock that supports digital transfer at up to 115.2 kHz. The output of the baud generator can be made available at the CLK pin under program control.

MODEM FUNCTION (73K222AL)

The modem section of the 73K222AU provides all necessary analog functions required to create a single chip Bell 212A/103 and CCITT V.22/V.21 modem, controlled by the system CPU or a local dedicated microprocessor. Asynchronous 1200 bit/s DPSK (Bell 212A and V.22) and 300 baud FSK (Bell 103 and V.21) modes are supported.

The modem portion acts as a peripheral to the microprocessor. In both modes of operation, control information is stored in register memory at specific address locations. In the single-port mode, the modem section can be controlled through the 16C450 interface, with no external microcontroller required. The primary analog blocks are the DPSK modulator/demodulator, the FSK modulator/ demodulator, the high and low band filters, the AGC, the special detect circuitry, and the DTMF tone generator. The analog functions are performed with switched capacitor technology.

PSK MODULATOR / DEMODULATOR

The 73K222AU modulates a serial bit stream into dibit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A or V.22 standard. The baseband signal is then filtered to reduce intersymbol interference on the band limited 2-wire PSTN line. Transmission occurs using either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into dibits and converted back to a serial bit stream. The demodulator also recovers the clock, which was encoded into the analog signal during modulation. The demodulator decodes either a 1200 Hz carrier (originate carrier) or a 2400 Hz carrier (answer carrier). The 73K222AU uses a phase-locked-loop coherent demodulation technique that offers inherently better performance than typical DPSK demodulators used by other manufacturers.

FSK MODULATOR/DEMODULATOR

The FSK modulator frequency modulates the analog output signal using two discrete frequencies to represent the binary data. In Bell 103, the standard frequencies of 1270 Hz and 1070 Hz (originate mark and space) and 2225Hz and 2025 Hz (answer mark and space) are used. V.21 mode uses 980 Hz and 1180 Hz (originate, mark and space) or 1650 Hz and 1850 Hz (answer, mark and space). Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value.

PASSBAND FILTERS AND EQUALIZERS

A high and low band filter is included to shape the amplitude and phase response of the transmit signal and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization is necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the band limited receive signal. The transmit signal filtering approximates a 75% square root of raised Cosine frequency response characteristic.

AGC

The automatic gain control maintains a signal level at the input to the demodulators, which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping, and provides a total dynamic range of >45 dB.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, call-progress tones, answer tone, and weak received signal (long loop condition). An unscrambled mark signal is also detected when the received data out of the DPSK demodulator before the descrambler has been high for 165.5 ms ±13.5 ms. The appropriate status bit is set when one of these conditions changes and an interrupt is generated for all monitored conditions except long loop. The interrupts are disabled (masked) when the enable interrupt bit is set to a 0.

DTMF GENERATOR

The DTMF generator will output one of 16 standard dual-tones determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Tone generation is initiated when the DTMF mode is selected and the transmit enable (CR0 bit D1) is changed from a 0 to a 1.

TEST FEATURES

Test features such as analog loopback (ALB), remote digital loopback, local digital loopback, and internal pattern generators are also included.

LINE INTERFACE

The line interface of the 73K222AU consists of a two-to-four wire hybrid, and an off-hook relay driver.

The two-to-four wire converter has a differential transmit output and requires only a line transformer and an external impedance matching resistor. Four-wire operation is also available by simply using either of the transmit output signals.

The relay driver output of the 73K222AU is an open drain signal capable of sinking 20 mA, which can control a line closure relay used to take the line off hook and to perform pulse dialing.

AUDIO MONITOR

An audio monitor output is provided which has a software programmable volume control. Its output is the received signal. The audio monitor output can directly drive a high impedance load, but an external power amplifier is necessary to drive a low-impedance speaker.

PIN DESCRIPTION

GENERAL

NAME	DIP	PLCC	TYPE	DESCRIPTION
VDD	40	44	I	+5V Supply ±10%, bypass with a 0.1 and a 22 µF capacitor to GND
GND	20	22	I	System Ground
VREF	19	21	O	VREF is an internally generated reference voltage, which is externally bypassed by a 0.1 µF capacitor to the system ground.
ISET	9	11	I	The analog current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND. Alternatively, an internal bias can be selected by connecting ISET to GND, which will result in a larger worst-case supply current due to the tolerance of on-chip resistors. Bypass with 0.1 µF capacitor if resistor is used.
XTL1 XTL2	25 24	27 26	I I	These pins are connections for the internal crystal oscillator requiring an 11.0592 MHz crystal. XTL2 can also be TTL driven from an external clock. Connect a 10 MΩ resistor from XTL1 to ground and a 1 MΩ resistor from XTL1 to XTL2
CLK	21	23	O	Output Clock. This pin is selectable under processor control to be either the crystal frequency (which might be used as a processor clock) or the output of the baud generator.
RESET	10	12	I	Reset. An active signal (high) on this pin will put the chip into an inactive state. The control register bits (except the Receiver Buffer, Transmitter Holding, and Divisor latches) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull-down resistor permits power-on reset using a 0.1 µF capacitor connected to the 5V supply.
STNDLN	15	17	I	Single-port mode select (active high). In a single-port system there is no local microprocessor and all the modem control is done through the 16C450 parallel bus interface. The local microprocessor interface is replaced with UART control signals, which allow the device to function as a digital UART as well as modem.

UART INTERFACE

NAME	DIP	PLCC	TYPE	DESCRIPTION
UA2-UA0 UA3	37-39 12	41-43 14	I I	UART Address. These pins determine which of the UART registers is being selected during a read or write on the UART data bus. The contents of the DLAB bit in the UART's Line Control Register also control which register is referenced. In single-port mode, UA0-UA3 are latched when $\overline{ADS}$ goes high. In dual-port, only UA0-UA2 are used.
UDO-UD7	27-34	30-37	I/O	(3 state) UART Data. Data or control information to the UART registers is carried over these lines.
$\overline{DISTR}$	35	38	I	Data Input Strobe. A low on this pin requests a read of the internal UART registers. Data is output on the D0-D7 lines if $\overline{DISTR}$ and $\overline{CS2}$ are active.
$\overline{DOSTR}$	36	39	I	Data Output Strobe. A low on this pin requests a write of the internal UART registers. Data on the D0-D7 lines are latched on the rising edge of $\overline{DOSTR}$. Data is only written if both $\overline{DOSTR}$ and $\overline{CS2}$ are active.
$\overline{CS2}$	1	2	I	Chip Select. A low on this pin allows a read or write to the UART registers to occur. In single port mode, $\overline{CS2}$ is latched on $\overline{ADS}$.
INTRPT	5	7	O	(3 state) UART Interrupt. This signal indicates that an interrupt condition on the UART side has occurred. If the Enable 8250A interrupt bit in the interrupt Enable Register is 0 the interrupt is gated by the $\overline{DISTR}$ signal to provide compatibility with the 8250B. The output can be put in a high impedance state with the OUT2 register bit in the Modem Control Register. In single-port mode, INTRPT also becomes valid when a modem interrupt signal is generated by the modem section's Detect Register.
RXD	6	8	I/O	Function is determined by STNDLN pin and bit 7, Tone Control Register:

STNDLN	D7	
0	0	RXD outputs data received by modem.
1	0	RXD is electrically an input but signal is ignored.
X	1	RXD is a serial input to UART.

UART INTERFACE (continued)

NAME	DIP	PLCC	TYPE	DESCRIPTION		
TXD	7	9	O	Function is determined by STNDLN pin and bit 7, Tone Control Register:		
				STNDLN	D7	
				0	0	TXD is a serial output of UART.
				1	0	TXD is forced to a mark.
				X	1	TXD is a serial output of UART.

ANALOG / LINE INTERFACE

TXA1 TXA2	3 4	4 5	O O	(differential) Transmitted Analog. These pins provide the analog output signals to be transmitted to the phone line. The drivers will differentially drive the impedance of the line transformer and the line matching resistor. An external hybrid can also be built using TXA1 as a single ended transmit signal.
RXA	16	18	I	Received Analog. This pin inputs analog information that is being received by the two-to-four wire hybrid. This input can also be taken directly from an external hybrid.
SPKR	17	19	O	Speaker Output. This pin outputs the received signal through a programmable attenuator stage, which can be used for volume control and disabling the speaker.
$\overline{OH}$	18	20	O	Off-hook relay driver. This signal is an open drain output capable of sinking 20 mA and is used for controlling a relay. The output is the complement of the $\overline{OH}$ register bit in CR3.

UART CONTROL INTERFACE (STNDLN = 1)
(See Figure 1: Single-port mode)

NAME	DIP	PLCC	TYPE	DESCRIPTION
$\overline{ADS}$	23	25	I	Address Strobe. $\overline{ADS}$ is used to latch address and chip select to simplify interfacing to a multiplexed Address/Data Bus. UA0-UA3 and $\overline{CS2}$ are latched when the $\overline{ADS}$ signal goes high.
UA3	12	14	I	UART Address Bit 3. UA3 is used in single-port mode to address the modem registers from the 16C450 interface. If UA3 is 0, the normal 16C450 registers are addressed by UA0-UA2 and if UA3 is 1, the modem registers are addressed. UA3 is latched when $\overline{ADS}$ goes high.
$\overline{CTS}$	14	16	I	Clear to Send. This pin is the complement of CTS bit in the Modem Status Register. The signal is used in modem handshake control to signify that communications have been established and that data can be transmitted.
$\overline{DSR}$	13	15	I	Data Set Ready. This pin is the complement of DSR bit in the Modem Status Register. The signal is used in modem handshake to signify that the modem is ready to establish communications.
$\overline{DCD}$	11	13	I	Data Carrier Detect. This pin is the complement of DCD bit in the Modem Status Register. The signal is used in modem control handshake to signify that the modem is receiving a carrier.
$\overline{DTR}$	22	24	O	Data Terminal Ready. The $\overline{DTR}$ output is programmed through a bit in the Modem Control Register. The signal is used in modem handshake to signify that the 16C450 is available to communicate.
$\overline{RTS}$	2	3	O	Request to Send. The $\overline{RTS}$ output is programmed through a bit in the Modem Control Register. The signal is used in modem handshake to signify that the 16C450 has data to transmit.
$\overline{RI}$	8	10	I	Ring Indicator. This Indicates that a telephone ringing signal is being received. This pin is the complement of the RI bit in the Modem Status Register.

PIN DESCRIPTION (continued)

MICROPROCESSOR INTERFACE (STNDLN = 0)
(See Figure 2: Dual-port mode)

NAME	DIP	PLCC	TYPE	DESCRIPTION
MA0-MA2	12-14	14-16	I	Modem Address Control. These lines carry register addresses for the modem registers and should be valid throughout any read or write operation.
DATA	22	24	I/O	Serial Control Data. Serial control data to be read/written is clocked in/out on the falling edge of the DCLK pin. The direction of data transfer is controlled by the state of the $\overline{RD}$ pin. If the $\overline{RD}$ pin is active (low) the DATA line is an output. Conversely, if the $\overline{RD}$ pin is inactive (high) the DATA line is an input.
$\overline{RD}$	23	25	I	Read. A low on this input informs the 73K222AU that control data or status information is being read by the processor from a modem register.
$\overline{WR}$	26	28	I	Write. A low on this input informs the 73K222AU that control data or status information is available for writing into a modem register. The procedure for writing is to shift in data LSB first on the DATA pin for eight consecutive cycles of DCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.
DCLK	11	13	I	Data Clock. The falling edge of this clock is used to strobe control data for the modem registers in or out on the DATA pin. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive cycles of DCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$. The falling edge of the $\overline{RD}$ signal must continue for eight cycles of DCLK in order to read all eight bits of the reference register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{INT}$	2	3	O	(with weak pull-up) Modem Interrupt. This output signal is used to inform the modem processor that a change in a modem detect flag has occurred. The processor must then read the Modem Detect Register to determine which detect triggered the interrupt. $\overline{INT}$ will stay active until the processor reads the Modem Detect Register or does a full reset.
MPRST*	8	10	O	Microprocessor Reset. This output signal is used to provide a hardware reset to the microprocessor. This signal is high if the RESET pin is high or the MCR bit D3 (OUT1) bit is set.
* NOTE: The µPRST pin is an upgraded function, which was not included in the initial definition of the 73K222AU.				

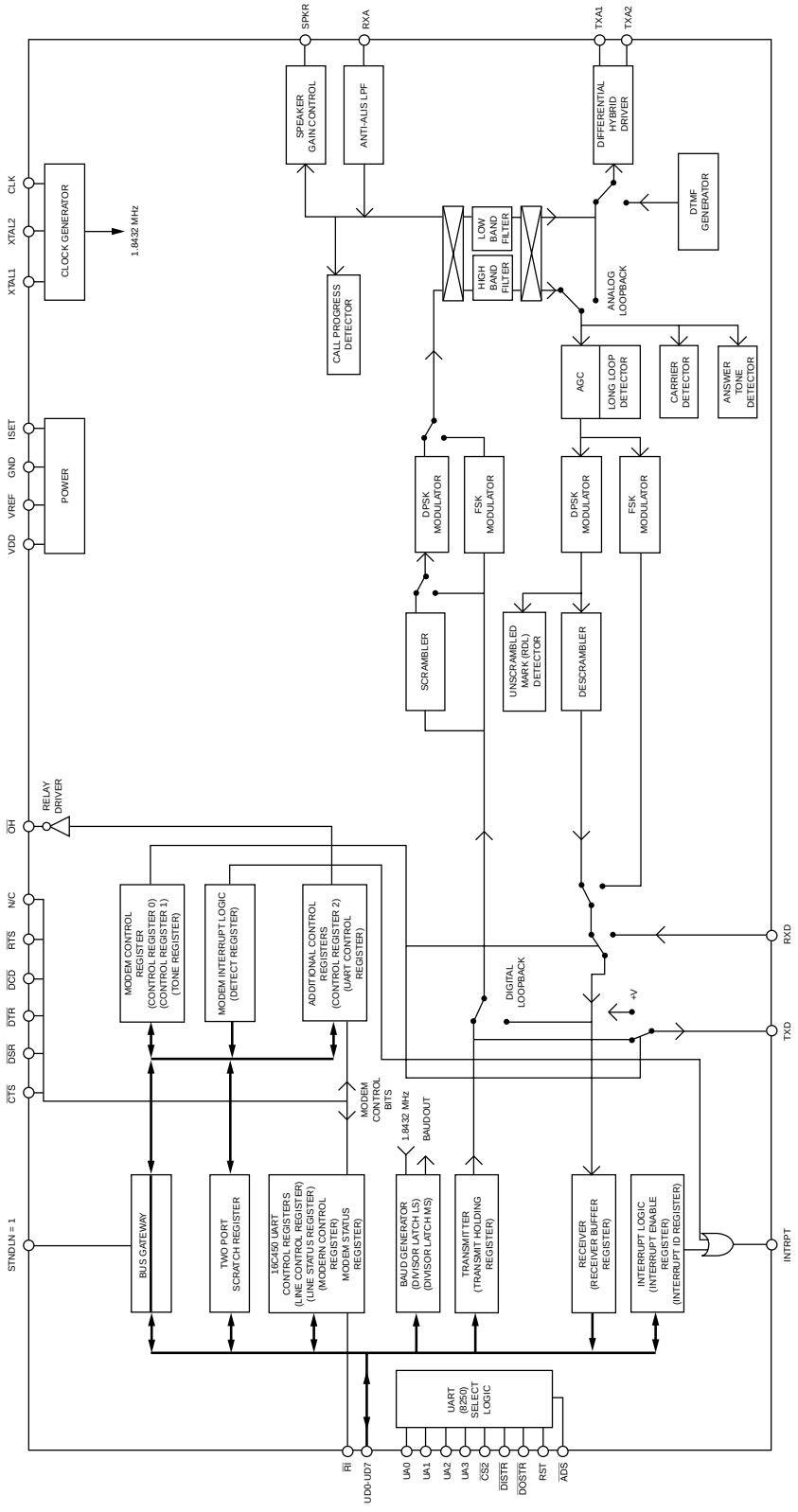


FIGURE 1: Single-Port Mode

In the single-port mode, the 73K222AU is designed to be accessed only by the main CPU using the same parallel bus utilized for data transfer. This mode is enabled when the STNDLN pin is at a logic "1". In the single port mode, internal registers are accessed by the main CPU to configure both the UART section and the modem function, eliminating the need for a separate microcontroller. In this mode, multiplexed pins provide the CTS, DSR, DTR, DED and RI signals normally associated with the UART function. A separate pin, ADS, is used for bus control.

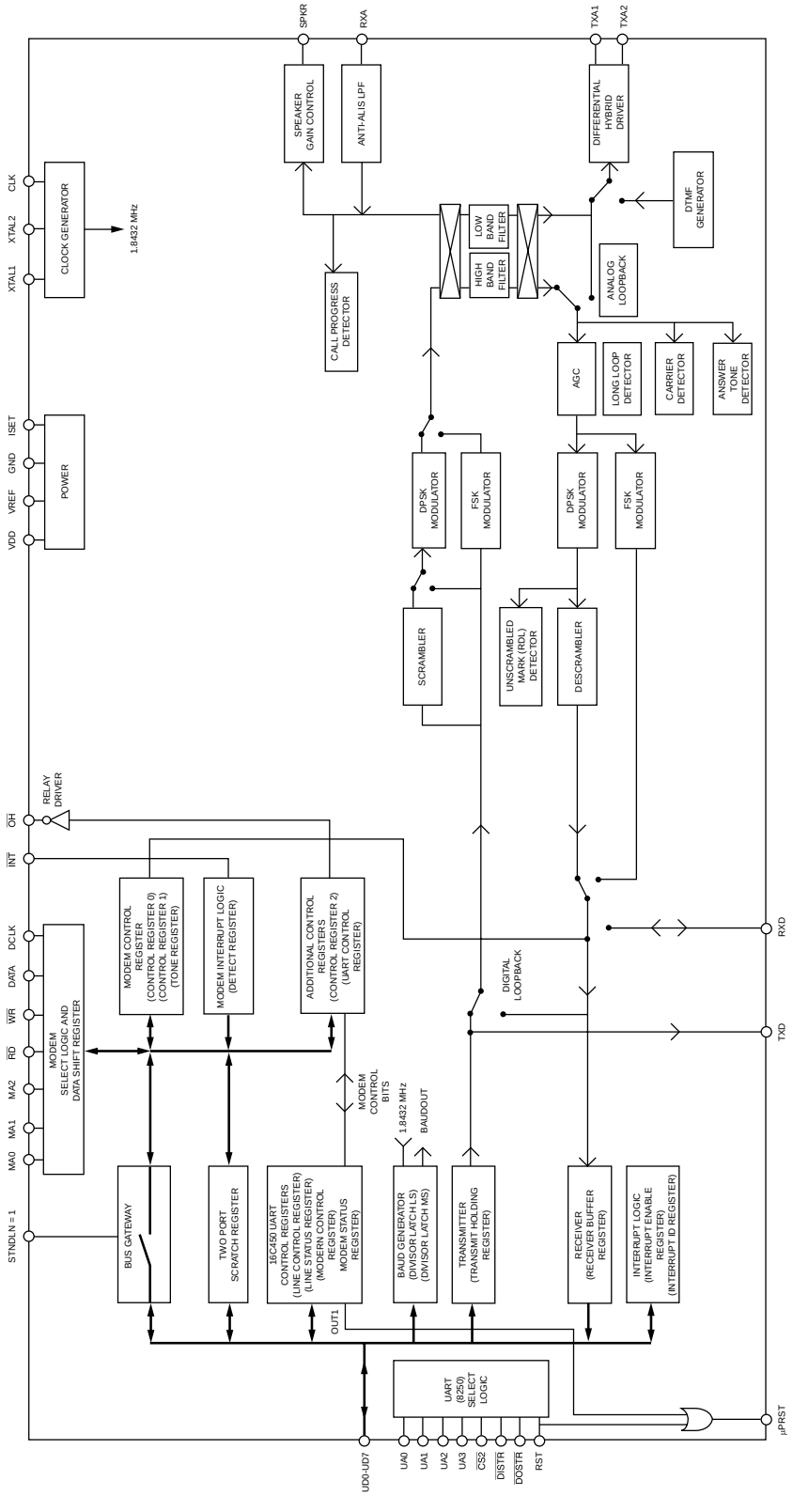


FIGURE 2: Dual-Port Mode

The dual-port mode allows use of a dedicated microprocessor for control of the modem function, and is enabled when the STNDLN pin = "0". This mode is useful for conventional plug-in card modem designs where it is necessary to make the modem function transparent to the main CPU. In this mode, the 73K222AU's multiplexed pins from the serial command bus used to communicate with the external microprocessor. The $\overline{RI}$, $\overline{CTS}$, $\overline{DSR}$, $\overline{DTR}$, and $\overline{DCD}$ logic functions must then be implemented using ports

The serial control interface allows access to the control and status registers via a serial command port. In this mode the MA0, MA1, and MA2 lines provide register addresses for data passed through the DATA pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the RD line is taken low. The next eight cycles of DCLK will then transfer out eight bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of DCLK. $\overline{WR}$ is then pulsed low and data transfer into the selected register occurs on the rising edge of $\overline{WR}$.

UART CONTROL REGISTER OVERVIEW

			DATA BIT NUMBER							
REGISTER		UART ADDRESS UA3-UA0*	D7	D6	D5	D4	D3	D2	D1	D0
RECEIVER BUFFER REGISTER (READ ONLY)	RBR	0000 DLAB = 0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TRANSMIT HOLDING REGISTER (WRITE ONLY)	THR	0000 DLAB = 0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INTERRUPT ENABLE REGISTER	IER	0001 DLAB = 0	0	0	0	ENABLE 8250A/ 16C450 INTERRUPT	ENABLE MODEM STATUS INTERRUPT	ENABLE REC. LINE STATUS INTERRUPT	ENABLE THR EMPTY INTERRUPT	ENABLE REC. DATA AVAILABLE INTERRUPT
INTERRUPT ID REGISTER (READ ONLY)	IIR	0010	0	0	0	0	0	INTERRUPT ID BIT 1	INTERRUPT ID BIT 0	"0" IF INTERRUPT PENDING
LINE CONTROL REGISTER	LCR	0011	DIVISOR LATCH ACCESS (DLAB)	SET BREAK	STICK PARITY	EVEN PARITY SELECT (EPS)	PARITY ENABLE (PEN)	NUMBER OF STOP BITS (STB)	WORD LENGTH SELECT 1 (WLS1)	WORD LENGTH SELECT 0 (WLS0)
MODEM CONTROL REGISTER	MCR	0100	0	0	0	LOOP	ENABLE INTERRUPT (OUT2 IN 16C450)	µPRST (OUT1 IN 16C450)	REQUEST TO SEND (RTS)	DATA TERMINAL READY (DTR)
LINE STATUS REGISTER	LSR	0101	0	TRANSMIT SHIFT REG EMPTY (TSRE)	TRANSMIT HOLDING REGISTER EMPTY(THRE)	BREAK INTERRUPT (BI)	FRAMING ERROR (FE)	PARITY ERROR (PE)	OVERRUN ERROR (OE)	DATA READY (DR)
MODEM STATUS REGISTER (READ ONLY)	MSR	0110	DATA CARRIER DETECT (DCD)	RING INDICATOR (RI)	DATA SET READY (DSR)	CLEAR TO SEND (CTS)	DELTA DATA CARR. DETECT (DDCD)	TRAILING EDGE RING INDICATOR (TERI)	DELTA DATA SET READY (DDSR)	DELTA CLEAR TO SEND (DCTS)
SCRATCH REGISTER	SCR	0111	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (LS)	DLL	0000 DLAB = 1	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (MS)	DLM	0001 DLAB = 1	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8

* In single-port mode (STNDLN pin = 1), all four address lines UA3-UA0 are used to address the UART Control Registers.

* In dual-port mode (STNDLN pin = 0), only three address lines UA2-UA0 are used to address the UART Control Registers, the UA3 pin becomes the MA2 pin in this mode.

MODEM CONTROL REGISTER OVERVIEW

REGISTER		ADDRESS STNDLN 0 MA2-MA0	ADDRESS STNDLN 1 UA3-UA0	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0	CR0	000	1000	MODULATION OPTION	0	MODULATION MODE	POWER ON	CHARACTER SIZE 1 (READ ONLY)	CHARACTER SIZE 0 (READ ONLY)	TRANSMIT ENABLE	ORIGINATE/ ANSWER
CONTROL REGISTER 1	CR1	001	1001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER	DR	010	1010	DEVICE SIGNATURE 1	DEVICE SIGNATURE 0	RECEIVE DATA	UNSCR. MARK DETECT	CARRIER DETECT	ANSWER TONE DETECT	CALL PROGRESS DETECT	LONG LOOP DETECT
TONE CONTROL REGISTER	TONE	011	1011	RXD/TXD CONTROL	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1	DTMF 0 GUARD/ANS. TONE
CONTROL REGISTER 2	CR2	100	1100	RESERVED FOR FUTURE USE							
CONTROL REGISTER 3	CR3	101	1101	SPEAKER VOLUME 1	SPEAKER VOLUME 0	OFF-HOOK	X	X	X	X	X
SCRATCH REGISTER	SCR	110	1110	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UART CONTROL REGISTER	UCR	111	1111	TXCLK (READ ONLY)	X	REQUEST TO SEND (RTS) (READ ONLY)	DATA TERM. READY (DTR) (READ ONLY)	RING INDICATOR (RI)	DATA CARRIER DETECT (DCD)	DATA SET READY (DSR)	CLEAR TO SEND (CTS)

X = Undefined, mask in software
0 = Only write zero to this location

UART REGISTER BIT DESCRIPTIONS

UART SECTION

RECEIVER BUFFER REGISTER (RBR) (READ ONLY)

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 000, DLAB = 0**	**UA3 - UA0 = 0000, DLAB = 0**

This read only register contains the parallel received data with start, stop, and parity bits (if any) removed. The high order bits for less than 8 data bits/character will be set to 0.

TRANSMIT HOLDING REGISTER (THR) (WRITE ONLY)

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 000, DLAB = 0**	**UA3 - UA0 = 0000, DLAB = 0**

This write only register contains the parallel data to be transmitted. The data is sent LSB first with start, stop, and parity bits (if any) added to the serial bit stream as the data is transferred.

INTERRUPT ENABLE REGISTER (IER)

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 001, DLAB = 0**	**UA3 - UA0 = 0001, DLAB = 0**

This 8-bit register enables the four types of interrupts of the UART to separately activate the chip Interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Received Data	1	This bit enables the Received Data Available Interrupt when set to logic 1.
D1	Transmitter Holding Register Empty	1	This bit enables the Transmitter Holding Register Empty Interrupt, when set to logic 1.
D2	Receiver Line Status Interrupt	1	This bit enables the Receiver Line Status Interrupt, when set to logic 1.
D3	Modem Status	1	This bit enables the Modem Status Register Interrupt when set to interrupt logic 1.
D4	8250A/16450	1/0	Set for compatibility with 8250A/16C450 UARTS. Reset this bit to disable the gating of the INTRPT interrupt line with the DISTR signal, which is needed for 8250B compatibility.
D5 - D7	Not Used	0	These three bits are always logic 0.

INTERRUPT ID REGISTER (IIR) (READ ONLY)

UART SECTION

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 010**	**UA3 - UA0 = 0010**

The IIR register gives prioritized information as to the status of interrupt conditions. When accessed, the IIR freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Interrupt Pending	0	This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine.
		1	When bit 0 is a logic 1, no interrupt is pending.
D1, D2	Interrupt ID bits 0, 1	Table below	These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in the following table.
D3 - D7	Not Used	0	These five bits of the IIR are always logic 0.

INTERRUPT PRIORITY TABLE

D2	D1	D0	PRIORITY	TYPE	SOURCE	RESET
0	0	1	-	None	None	-
1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Receive Data Available	Receive Data Available	Reading the Rcvr. Buffer Register
0	1	0	Third	Transmit Holding Register Empty	Transmit Holding Register Empty	Reading IIR Register (if source of interrupt) or Writing to Transmit Holding Register
0	0	0	Fourth	Modem Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Det.	Reading the Modem Status Register

LINE CONTROL REGISTER (LCR)
STNDLN: 0 1
ADDRESS: UA2 - UA0 = 011 UA3 - UA0 = 0011

UART SECTION

The user specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the user may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics.

BIT NO.	NAME	CONDITION		DESCRIPTION
D0	Word Length Select 0			Bits D0 and D1 select the number of data bits per character as shown:
D1	Word Length Select 1	D1	D0	Word Length
		0	0	5 bits
		0	1	6 bits
		1	0	7 bits
		1	1	8 bits
D2	Number of Stop Bits	0 or 1		This bit specifies the number of stop bits in each transmitted character. If bit 2 is a logic 0, one stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one-and-a-half stop bits are generated. If bit 2 is a logic 1 when either a 6, 7, or 8-bit word length is selected, two stop bits are generated. The receiver checks the first stop bit only, regardless of the number of stop bits selected.
D3	Parity Enable	1		This bit is the Parity Enable bit. When bit 3 is a logic 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data. (The parity bit is used to produce an even or odd number of 1's when the data word bits and the parity bit are summed).
D4	Even Parity Select	1 or 0		This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1's are transmitted or checked in the data word bits and parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1's are transmitted or checked.

LINE CONTROL REGISTER (LCR) (continued)

UART SECTION

BIT NO.	NAME	CONDITION		DESCRIPTION
D5	Stick Parity	1 or 0		This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the parity bit is transmitted and checked by the receiver as a logic 0 if bit 4 is a logic 1 or as a logic 1 if bit 4 is a logic 0.
		D5	D4	Parity
		0	0	ODD Parity
		0	1	EVEN Parity
		1	0	MARK Parity
		1	1	SPACE Parity
D6	Set Break	1		Output of modem is set to a spacing state. When the modem is transmitting DPSK data if the Set Break bit is held for one full character (start, data, parity, stop) the break will be extended to 2 N + 3 space bits (where N = # data bits + parity bit + 1 start + 1 stop). Any data bits generated during this time will be ignored. See note below.
D7	Divisor Latch Access Bit (DLAB)	1		This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the baud generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

NOTE: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0's pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the Transmitter to be idle. (TSRE = 1), and clear break when normal transmission has to be restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

MODEM CONTROL REGISTER (MCR)

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 100**	**UA3 - UA0 = 0100**

The MCR register controls the interface with the modem. Bits D1 and D0 are also available as read only bits in the UART Control Register in the Modem Registers. In single-port mode, bits D1 and D0 are available inverted at the $\overline{RTS}$ and $\overline{DTR}$ pins.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTR	1	This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.
D1	RTS	1	This bit controls the Request to Send ($\overline{RTS}$) output. When bit 1 is set to a logic 1, the $\overline{RTS}$ output is forced to a logic 0. When bit 1 is reset to a logic 0, the $\overline{RTS}$ output is forced to a logic 1.
D2	µPRST* (OUT1 in 16C450)	1	In single-port mode inactive unless loop = 1, then functions as below (D4). In dual-port mode the µPRST pin is the logical OR of this bit and the RESET pin.
D3	Enable Interrupt (OUT2 in 16C450)	0	Sets INTRPT pin to high impedance if STNDLN = 1.
		1	INTRPT output enabled.
D4	LOOP	1	This bit provides a local loopback feature for diagnostic testing of the UART portion of the 73K222AU. When bit D4 is set to logic 1, the following occurs: 1. TXD is forced to mark, RXD is ignored. 2. The output of the Transmitter is looped to the Receiver. 3. The four modem control inputs to the UART ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are ignored and the UART signals $\overline{RTS}$, $\overline{DTR}$, Enable Interrupt, and µPRST are forced inactive. 4. The UART signals RTS, DTR, Enable Interrupt, and µPRST are internally connected to the four control signals CTS, DSR, DCD and RI respectively. Note that the Modem Status Register Interrupts are now controlled by the lower four bits of the Modem Control Register. The interrupts are still controlled by the Interrupt Enable Register.
D5 - D7		0	These bits are permanently set to logic 0.

* Note: The µPRST bit has an upgraded function, which was not included in the initial definition of the 73K222AU.

LINE STATUS REGISTER (LSR)
STNDLN: 0 1
ADDRESS: UA2 - UA0 = 101 UA3 - UA0 = 0101

This register provides status information to the CPU concerning the data transfer.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DR	1	The Data Ready (DR) bit is set to a 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Data Ready is reset to 0 by reading the data in the Receiver Buffer Register or by writing a 0 into it from the processor.
D1	OE	1	The Overrun Error (OE) bit indicates that the data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.
D2	PE	1	The Parity Error (PE) bit indicates that the received character did not have the correct parity. The bit is reset to 0 whenever the CPU reads the Line Status Register.
D3	FE	1	The Framing Error (FE) bit indicates that the received character did not have a valid stop bit. The FE indicator is reset whenever the CPU reads the contents of the Line Status Register. A framing error will not occur in DPSK receive from the modem due to the fact that missing stop bits are reinserted.
D4	BI	1	The Break Interrupt (BI) bit indicates that a break has been received. A break occurs whenever the received data is held to 0 for a full data word (start + data + stop) or for two full data words when receiving in DPSK mode from the modem. The BI bit is reset to 0 whenever the CPU reads the Line Status Register.
D5	THRE	1	The Transmit Holding Register Empty (THRE) indicates that the Transmitter is ready to accept a new character for transmission. The THRE bit is reset when the CPU loads a character into the Transmit Holding Register.
D6	TSRE	1	The Transmit Shift Empty (TSRE) indicates that both the Transmit Holding Register and the Transmit Shift Registers are empty.
D7	-	0	Always zero.

UART SECTION

MODEM STATUS REGISTER (MSR) (READ ONLY)

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 110**	**UA3 - UA0 = 0110**

This register provides the current state of the control signals from the modem. In addition, four bits provide change information. The CTS, DSR, DCD, and RI signals come from the UART Control Register if STNDLN = 0 and from the $\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$ and $\overline{RI}$ pins (inverted) if STNDLN = 1. This register is READ ONLY. The delta bits indicate whether the inputs have changed since the last time the Modem Status Register has been read. In Loop Mode CTS, DSR, RI and DCD are taken from RTS, DTR, µPRST, and Enable Interrupt in the Modem Control Register respectively.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DCTS	1	This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.
D1	DDSR	1	This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.
D2	TERI	1	This bit is the Trailing Edge of the Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed state.
D3	DDCD	1	This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state.
D4	CTS	1	This bit is the complement of the Clear To Send ($\overline{CTS}$) input. If STNDLN = 0, this reflects the status of the UART Control Register bit. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.
D5	DSR	1	This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If STNDLN = 0, this reflects the status of the UART Control Register bit. If bit 4 of the MCR is set to a 1, this bit is the equivalent of DTR in the MCR.
D6	RI	1	This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If STNDLN = 0, this reflects the status of the UART Control Register bit. If bit 4 of the MCR is set to a 1, this bit is equivalent to µPRST in the MCR.
D7	DCD	1	This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) If STNDLN = 0, this reflects the status of the UART Control Register bit. If bit 4 of the MCR is set to a 1, this bit is equivalent to Enable Interrupt in the MCR.

SCRATCH REGISTER (SCR)

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 111**	**UA3 - UA0 = 0111**

The Scratch Register is a dual port register, which can be simultaneously accessed through both the UART bus and the modem bus. This provides the possibility for the modem controller to communicate directly with the central CPU. Note that if both processors write the Scratch Register, the data stored will be from whichever processor last wrote the register.

DIVISOR LATCH (Least significant byte) (DLL)

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 000, DLAB = 1**	**UA3 - UA0 = 0000, DLAB = 1**

DIVISOR LATCH (Most significant byte) (DLM)

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 001, DLAB = 1**	**UA3 - UA0 = 0001, DLAB = 1**

DIVISOR LATCH VALUE VS. DATA RATE

The Divisor Latch is two 8-bit write only registers, which control the rate of the programmable baud generator. The programmable baud generator generates an output clock by dividing an internal 1.8432 MHz clock by the value stored in the divisor latch. This output clock has a value of 16X the data rate at which the modem will operate. This output clock is available at pin 21 under the control of bit 3 (D3) of the Modem Control Register 1. Upon loading either of the Divisor Latches the 16-bit device counter is immediately loaded, preventing long counts on initial load. The following table shows divisor values for common data rates.

DESIRED DATA RATE	DIVISOR USED FOR 16 x DATA RATE CLOCK	% ERROR GENERATED	DESIRED DATA RATE	DIVISOR USED FOR 16 x DATA RATE CLOCK	% ERROR GENERATED
50 [1]	2304		4800	24	
75 [1]	1536		7200	16	
110 [1]	1047		9600	12	
134.5 [1]	857	0.058	19200	6	
159 [1]	768		38400	3	
300 [1]	384		56000	2	2.86
600 [2]	192		1. Data Rate valid for FSK transmission.		
1200 [3]	96		2. Data Rate valid for half speed DPSK transmission.		
1800	64		3. Data Rate valid for normal 1200 bit/s DPSK transmission.		
2000	58	0.69			
2400	48				
3600	32				

MODEM REGISTER BIT DESCRIPTIONS

CONTROL REGISTER (CR0)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 000 UA3 - UA0 = 1000

BIT NO.	NAME	CONDITION		DESCRIPTION
D0	Answer/Originate	0		Selects Answer Mode (transmit in high band, receive in low band).
		1		Selects Originate Mode (transmit in low band, receive in high band).
D1	Transmit Enable	0		Disables transmit output at TXA.
		1		Enables transmit output at TXA. NOTE: Answer tone and DTMF TX control require Transmit Enable. If Transmit Enable is on, call progress and answer tone detector interrupts are masked.
D2, D3	Character Size 0, 1			These bits are read only. These bits represent the character size. The character size is determined by the UART Line Control Register and includes data, parity (if used), one start bit, and one stop bit.
		D3	D2	Character length
		0	0	8-bit character
		0	1	9-bit character
		1	0	10-bit character
		1	1	11-bit character
D4	Power ON			This bit controls the power down mode of the 73K222AU, the analog, and most digital portions of the chip. The digital interface is active during power down.
		0		Power down mode.
		1		Normal operation.
D5	Modulation Mode	0		DPSK
		1		FSK
D6	Reserved	0		Must be written as zero.
D7	Modulation Option	0		DPSK: 1200 bit/s
		1		600 bit/s
		0		FSK: 103 mode
		1		V.21 mode

CONTROL REGISTER (CR1)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 001 UA3 - UA0 = 1001

BIT NO.	NAME	CONDITION		DESCRIPTION
D0, D1	Test Mode	D1	D0	
		0	0	Selects normal operating mode.
		0	1	Analog Loopback Mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the Transmitter. To squelch the TXA pin, transmit enable bit must be forced low.
		1	0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data in TXD is ignored.
		1	1	Selects half-duplex. Internally performs a logical AND of TXD and RXD to send to the UART receiver. Both transmit and receive characters will occur at the Receiver Buffer Register.
D2	Reset	0		Selects normal operation.
		1		Resets modem to power down state. All Control Register bits (CR0, CR1, TONE) are reset to zero. The output of the clock pin will be set to the crystal frequency.
D3	CLK Control (Clock Control)	0		CLK pin output is selected to be an 11.0592 MHz crystal echo output.
		1		CLK pin output is selected to be 16 x the Data Rate set by the UART divisor latch.
D4	Bypass Scrambler	0		Selects normal operation. DPSK data is passed through scrambler.
		1		Selects Scrambler Bypass. DPSK data is routed around scrambler in the transmit path.

CONTROL REGISTER (CR1) (continued)

BIT NO.	NAME	CONDITION		DESCRIPTION
D5	Enable Detect Interrupt	0		Disables interrupts generated by Detect Register bits D1 - D4 at INT pin in dual-port mode, or at INTRPT pin in single-port mode. All interrupts normally disabled in power down modes.
		1		Enables interrupts generated by Detect Register bits D1 - D4 at $\overline{\text{INT}}$ pin in dual-port mode, or at INTRPT pin in single-port mode. An interrupt will be generated with a change in status of DR bits D1 - D4. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode. The interrupt is reset when the DR register is read.
D6, D7	Transmit Pattern	D7	D6	
		0	0	Selects normal data transmission as controlled by the state of the TXD pin.
		0	1	Selects an alternating mark/space transmit pattern for modem testing.
		1	0	Selects a constant mark transmit pattern.
		1	1	Selects a constant space transmit pattern.

DETECT REGISTER (DR)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 010 UA3 - UA0 = 1010

BIT NO.	NAME	CONDITION		DESCRIPTION
D0	Long Loop	0		Indicates normal received signal.
		1		Indicates low received signal level (< -38 dBm).
D1	Call Progress Detect	0		No call progress tone detected.
		1		Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress bandwidth.
D2	Answer Tone Received	0		No answer tone detected.
		1		Indicates detection of 2225 Hz answer tone in Bell mode or 2100 Hz in CCITT mode. The device must be in Originate Mode for detection of answer tone for normal operation. For CCITT answer tone detection, bit D0 of the Tone Register must be set.
D3	Carrier Detect	0		No carrier detected in the receive channel.
		1		Carrier has been detected in the receive channel.
D4	Unscrambled Marks	0		No unscrambled mark detected.
		1		Indicates detection of unscrambled marks in the received data. A valid indication requires that unscrambled marks be received for > 165.5 ± 13.5 ms.
D5	Receive Data			Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7	Device Signature 0, 1	D7	D6	Product Identified
		0	0	73K212U (special order only)
		0	1	73K221U (special order only)
		1	0	73K222AU

TONE CONTROL REGISTER (TONE)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 011 UA3 - UA0 = 1011

The Tone Control Register contains information on the tones that are transmitted. Tones are transmitted only if the Transmit Enable bit is set. The priority of the transmit tones are: 1) DTMF, 2) Answer, 3) FSK, 4) Guard.

BIT NO.	NAME	CONDITION				DESCRIPTION
D0	DTMF 0 / Answer/ Guard Tone	D6	D5	D4	D0	D0 interacts with bits D6, D5, and D4 as shown:
		X	X	1	X	Transmit DTMF tones.
		X	1	0	0	Select 2225 Hz answer tone (Bell).
		X	1	0	1	Select 2100 Hz answer tone (CCITT).
		1	0	0	0	Select 1800 Hz guard tone.
		1	0	0	1	Select 550 Hz guard tone.
D0, D1, D2, D3	DTMF	Table below:				Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) is set. Tone encoding is shown below.

KEYBOARD EQUIVALENT	DTMF CODE D3	D2	D1	D0	TONES LOW	HIGH
1	0	0	0	1	697	1209
2	0	0	1	0	697	1336
3	0	0	1	1	697	1477
4	0	1	0	0	770	1209
5	0	1	0	1	770	1336
6	0	1	1	0	770	1477
7	0	1	1	1	852	1209
8	1	0	0	0	852	1336
9	1	0	0	1	852	1477
0	1	0	1	0	941	1336
*	1	0	1	1	941	1209
#	1	1	0	0	941	1477
A	1	1	0	1	697	1633
B	1	1	1	0	770	1633
C	1	1	1	1	852	1633
D	0	0	0	0	941	1633

TONE CONTROL REGISTER (TONE) (continued)

BIT NO.	NAME	CONDITION		DESCRIPTION
D4	TX DTMF (Transmit DTMF)	0		Disable DTMF.
		1		Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.
D5	TX ANS (Transmit Answer Tone)	D5	D0	D5 interacts with bit D0 as shown.
		0	X	Disables answer tone generator.
		1	0	Enables answer tone generator. A 2225 Hz answer tone will be transmitted continuously when the transmit enable bit is set. The device must be in answer mode.
		1	1	Enables a 2100Hz answer tone generator, with operation same as above.
D6	TX Guard (Transmit Guard Tone)	0		Disables guard tone generator.
		1		Enables guard tone generator. (See D0 for selection of guard tones).
D7	RXD/TXD Control	STNDLN	D7	Function is dependant on status of STNDLN pin.
		0	0	RXD is output data received by modem, TXD is serial output of UART. For monitoring only.
		1	0	RXD is electrically an input, but the signal is ignored, TXD is forced to a mark.
		1	1	RXD is serial input to UART, TXD is serial output of UART.

CONTROL REGISTER (CR3)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 101 UA3 - UA0 = 1101

D0 - D4	Not Used			Not presently used.
D5	Off Hook	0		Relay driver open.
		1		Open drain driver pulling low.
D6, D7	Speaker Volume 0, 1	D7	D6	Speaker volume control status.
		0	0	Speaker off
		0	1	-24 dB
		1	0	-12 dB
		1	1	0 dB

SCRATCH REGISTER (SCR)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 110 UA3 - UA0 = 1110

The Scratch Register is a dual-port register, which can be accessed either through the UART bus or the modem bus. It can be used for a communication path outside the data stream.

UART CONTROL REGISTER (UCR)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 111 UA3 - UA0 = 1111

The UART Control Register contains the handshaking signals necessary for the microprocessor to communicate with the central CPU through the UART.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	CTS	1	In dual-port mode, CTS, DSR, DCD and RI are writeable locations, which can be read through the 16C450 port in the Modem Status Register.
D1	DSR	1	In the single-port mode, D0 - D3 are ignored and the information for the Modem Status Register comes directly from the external pins.
D2	DCD	1	
D3	RI	1	
D4	DTR	1	
D5	RTS	1	DTR and RTS are read only versions of the same register bits in the Modem Control Register.
D6	Not Used		
D7	TXCLK	Clock	TXCLK is the clock that the UART puts out with TXD. The falling edge of TXCLK is coincident with the transitions of data on TXD. TXCLK can also be used for the microprocessor to send synchronous data independent of the UART by forcing data patterns using CR1 bits 6 and 7 before the rising edge of TXCLK.
NOTE: Control Register 2 (CR2) is reserved for future products and is disabled.			

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

TA = -40°C to 85°C, VDD = 5V ± 10%, unless otherwise noted.

PARAMETER	RATING	UNIT
VDD Supply Voltage	7	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD +0.3	V
NOTE: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.		

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VDD, Supply Voltage		4.5	5	5.5	V
TA, Operating Free-Air Temperature		-40		85	°C
External Component (Refer to application drawing for placement.)					
VREF Bypass Capacitor [2]	(VREF to GND)	0.1			µF
Bias Setting Resistor [1]	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass Capacitor [2]	ISET pin to GND	0.1			µF
VDD Bypass Capacitor [2]	(VDD to GND)	0.1			µF
XTL1 Load Capacitor	From pin to GND			40	pF
XTL2 Load Capacitor	From pin to GND			20	pF
Input Clock Variation	(11.0592 MHz)	-0.01		+0.01	%
Hybrid Loading					
R1	See Figure 3		600		Ω
R2			600		Ω
C	TXA Hybrid Loading		0.033		µF

1. Optional for minimum worst-case current consumption.
2. Minimum for optimized system layout; may require higher values for noisy environments.

DC ELECTRICAL CHARACTERISTICS

TA = -40°C to +85 °C, VDD = 5V ± 10%, unless otherwise noted.

PARAMETER		CONDITION		MIN	NOM	MAX	UNIT
IDD, Supply Current							
IDDA, Active		ISET Resistor = 2 MΩ			8	12	mA
IDDA, Active		ISET = GND			8	15	mA
IDD1, Power-Down		CLK = 11.0592 MHz			3	4	mA
IDD2, Power-Down		CLK = 19.200 kHz			2	3	mA
Digital Inputs							
Input High Current	IIH	VI = VDD				100	µA
Input Low Current	IIL	VI = 0		-200			µA
Input Low Voltage	VIL					0.8	V
Input High Voltage	VIH	Except RESET & XTL1		2.0			V
Input High Voltage	VIH	RESET & XTL1		3.0			V
Pull Down Current	RESET PIN			5		30	µA
Input Capacitance						10	pF
Digital Outputs							
Output High Voltage	VOH	IOUT = - 1 mA		2.4		VDD	V
VOL UD0-UD7 and INTRPT		IOUT = 3.2 mA				0.4	V
VOL other outputs		IOUT = 1.6 mA				0.4	V
CLK Output	VOL	IOUT = 3.2 mA				0.6	V
OH Output	VOL	IOUT = 20 mA				1.0	V
OH Output	VOL	IOUT = 10 mA				0.5	V
Offstate Current INTRPT pin		VO = 0V		-20		20	µA
Capacitance							
Inputs		Input Capacitance				10	pF
CLK		Maximum capacitive load to pin				15	pF
Analog Pins							
RXA Input Resistance					200		kΩ
RXA Input Capacitance						25	pF

ELECTRICAL SPECIFICATIONS (continued)

DYNAMIC CHARACTERISTICS AND TIMING
TA = -40°C to +85°C, VDD = 5V ± 10%, unless otherwise noted.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
DPSK Modulator					
Carrier Suppression	Measured at TXA	55			dB
Output Amplitude	ANS TONE 2225 or 2100 Hz	-11	-10.0	-9	dBm0
	DPSK TX Scrambled Marks	-11	-10.0	-9	dBm0
	FSK Dotting Pattern	-11	-10.0	-9	dBm0
FSK Tone Error	Bell 103 or V.21			±5	Hz
DTMF Generator					
Freq. Accuracy		-.25		.25	%
Output Amplitude	Low Band, not in V.21 mode	-10	-9	-8	dBm0
Output Amplitude	High Band, not in V.21 mode	-8	-7	-6	dBm0
Long Loop Detect	DPSK or FSK	-40		-32	dBm0
Demodulator Dynamic Range	DPSK or FSK		45		dB
Call Progress Detector					
Detect Level	2-Tones in 350-600 Hz Band	-39		0	dBm0
Reject Level	2-Tones in 350-600 Hz Band			-46	dBm0
Delay Time	-70 dBm0 to -30 dBm0 Step	27		80	ms
Hold Time	-30 dBm0 to -70 dBm0 Step	27		80	ms
Hysteresis		2			dB
Carrier Detect					
Threshold	DPSK or FSK Receive Data	-49		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 Step	15		45	ms
Hysteresis		2	3.0		dB
Hold Time	-30 dBm0 to -70 dBm0 Step	10		24	ms
Answer Tone Detector					
Detect Level Threshold	In FSK mode	-49.5		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 Step	20		45	ms
Hold Time	-30 dBm0 to -70 dBm0 Step	10		30	ms
Detect Frequency Range		-2.5		+2.5	%

1. All units in dBm0 are measured at the line input to the transformer. The interface circuit inserts an 8 dB loss in the transmit path (TXA1 - TXA2 to line), and a 3 dB loss in the receive path (line to RXA).

DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Speaker Output					
Gain Error		-1		+1	dB
Output Swing SPKR	10K||50 pF LOAD 5% THD	2.75			VP
Carrier VCO					
Capture Range	Originate or Answer	-10		10	Hz
Capture Time	-10 Hz to +10 Hz Carrier Frequency change assumed		40	100	ms
Recovered Clock					
Capture Range	% of Center Frequency	-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin.		30	50	ms
Guard Tone Generator					
Tone Accuracy	550 or 1800 Hz	-20		+20	Hz
Tone Level	550 Hz	-4.0	-3.0	-2.0	dB
(Below DPSK Output)	1800 Hz	-7.0	-6.0	-5.0	dB
Harmonic Distortion	700 to 2900 Hz			-60	dB

SERIAL BUS INTERFACE (See Figure 4)
The following times are for CL = 100 pF.

PARAMETER	MIN	NOM	MAX	UNIT
Data out from Read			70	ns
Data out after Clock			110	ns
Data Float after Read			40	ns
Clock High after Read	0			ns
Write Width	65		10000	ns
Data Setup Before Clock	0			ns
Data Hold after Clock	55			ns
Write after Clock	60			ns
Address setup before Control [1]	0			ns
Address Hold after Control [1]	100			ns
Address setup before Write LOW	0			ns
Address Hold after Write HIGH	0			ns
1. Control is later of falling edge of RD or DCLK.				

ELECTRICAL SPECIFICATIONS (continued)

PARALLEL BUS INTERFACE (See Figure 5) The following times are for CI = 100 pF.

PARAMETER		MIN	MAX	MIN	MAX	UNIT
		Dual-Port Mode		Single-Port Mode		
RC	Read Cycle = TAD + TRC	240		340		ns
TDIW	DISTR Width	30		30		ns
TDDD	Delay DISTR to Data (read time)		45		45	ns
THZ**	DISTR to Floating Data Delay		50		40	ns
TRA	Address Hold after DISTR	20		5		ns
TRCS	Chip select hold after DISTR	20		20		ns
TAR*	DISTR Delay after Address	22		15		ns
TCSR	DISTR Delay after Chip Select	20		20		ns
WC	Write Cycle = TAW + TDOW + TWC	140		140		ns
TDOW	DOSTR Width	40		40		ns
TDS	Data Setup	15		25		ns
TDH**	Data Hold	5		5		ns
TWA	Address Hold after DOSTR	20		5		ns
TWCS	Chip select hold after DOSTR	20		20		ns
TAW*	DOSTR delay after Address	0		15		ns
DOSTR delay after Chip Select		20		20		ns
TADS	Address Strobe Width			15		ns
TAS	Address Setup Time			10		ns
TAH	Address Hold Time			0		ns
TCS	Chip Select Setup Time			10		ns
TCH	Chip Select Hold Time			0		ns
TRC	Read Cycle Delay	40		40		ns
TWC	Write Cycle Delay	40		40		ns
TAD	Address to Read Data	110		110		ns

* TAR and TAW are referenced from the falling edge of either $\overline{CS2}$ or $\overline{DISTR}$ or $\overline{DOSTR}$, whichever is later.

** THZ and TDH are referenced from the rising edge of $\overline{CS2}$ or $\overline{DISTR}$ or $\overline{DOSTR}$, whichever is earlier.

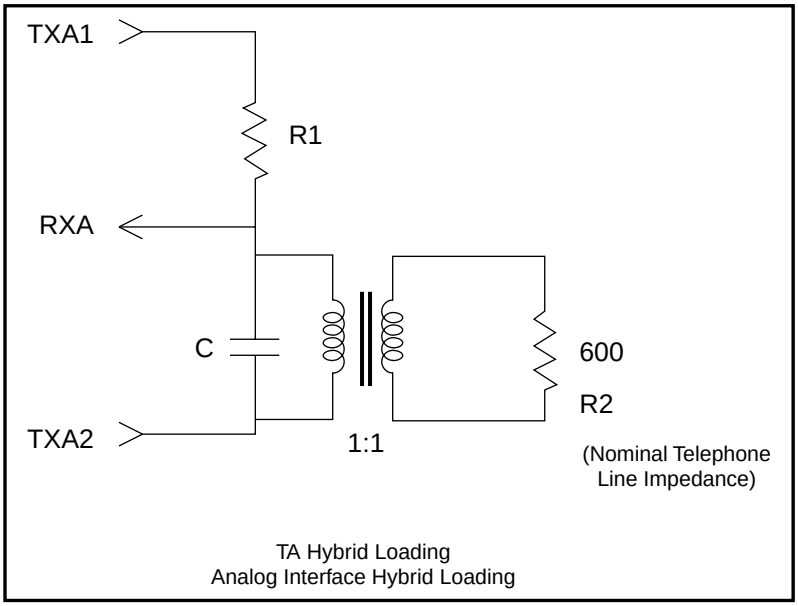


FIGURE 3: TXA Hybrid Loading Analog Interface Hybrid Loading

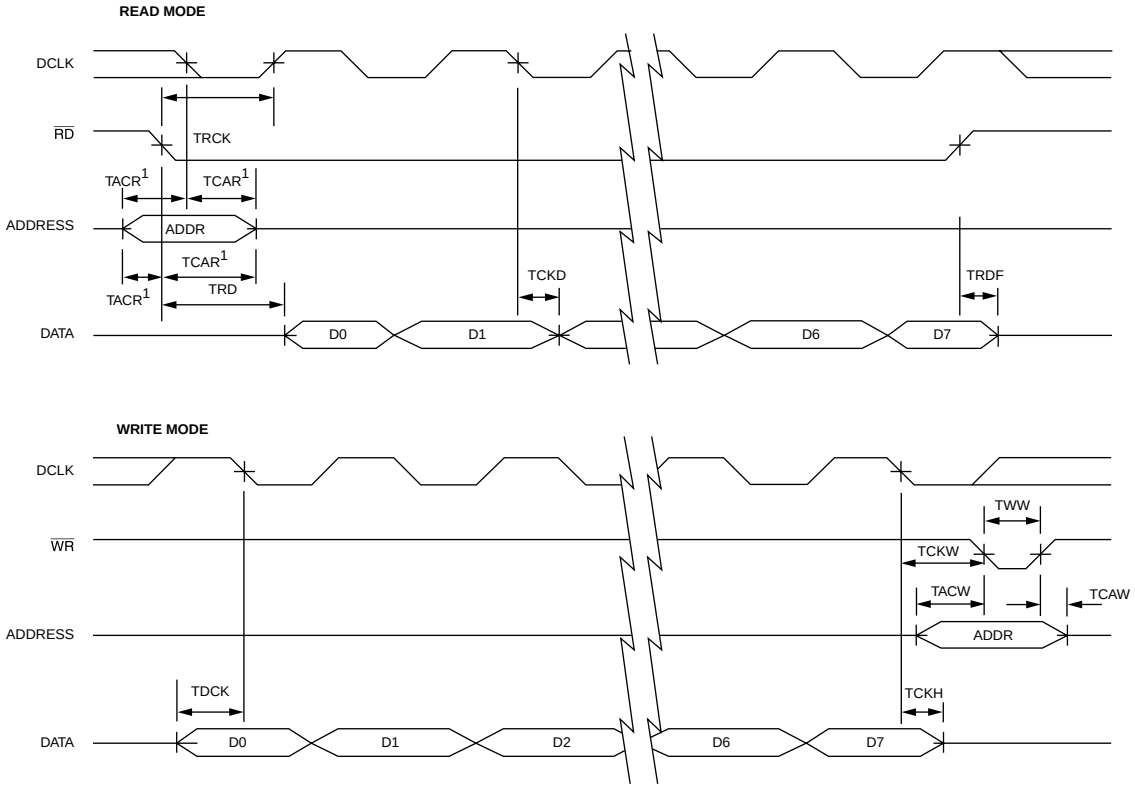


FIGURE 4: Modem Serial Bus Timing

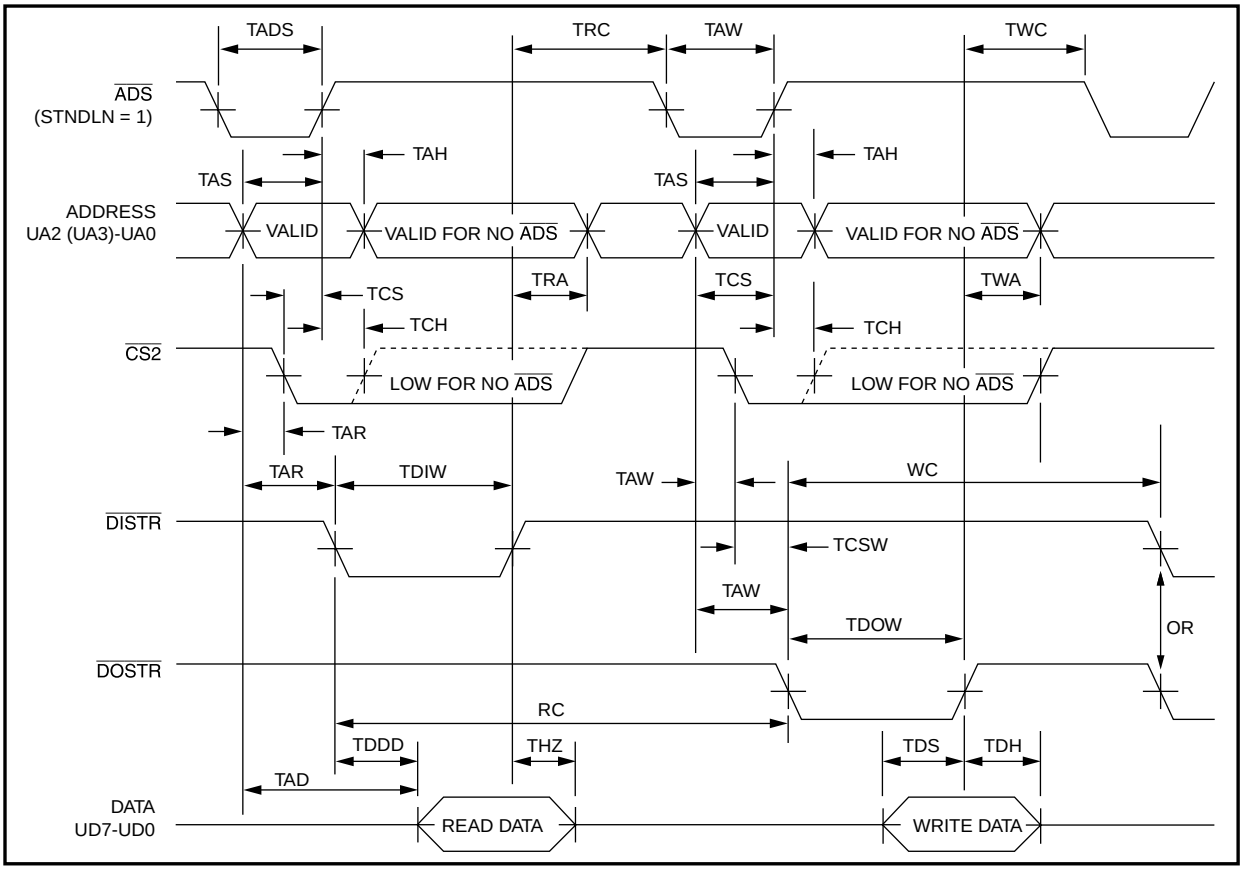


FIGURE 5: UART Bus Timing

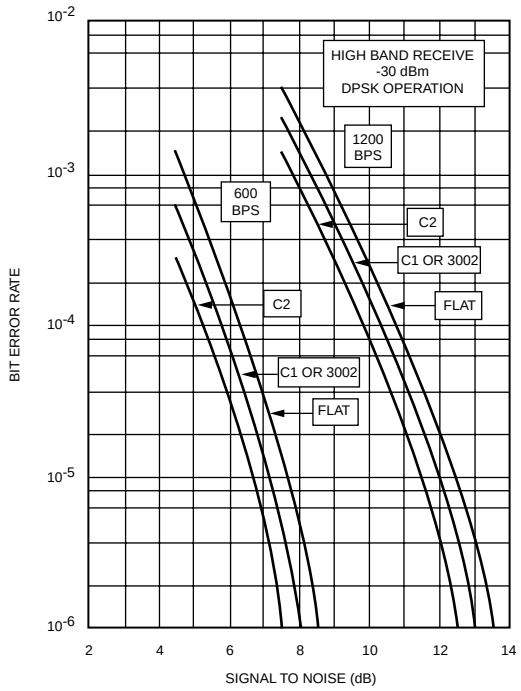
TYPICAL PERFORMANCE CHARACTERISTICS

The 73K222AU was designed using an integrated analog/digital architecture that offers optimum performance over a wide range of line conditions. The 73K222AU utilizes the circuit design proven in TERIDIAN Semiconductor's 73K222L one-chip modem, with added enhancements, which extend low signal level performance and increase immunity to spurious noise typically encountered in integral bus applications. The 73K222AU provides excellent immunity to the types of disturbances present with usage of the dial-up telephone network. The following curves show representative Bit Error Rate performance under various line conditions.

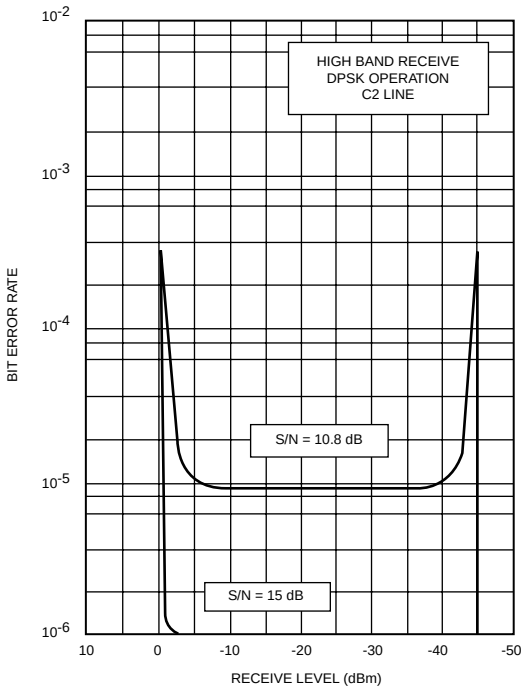
BER vs. S/N

This test measures the ability of the modem to function with minimum errors when operating over noisy lines. Since some noise is generated by even the best dial-up lines, the modem must operate with as low a S/N ratio as possible. Optimum performance is shown by curves that are closest to the zero axis. A narrow spread between curves for the four line conditions indicates minimal variation in performance when operating over a range of line qualities and is typical of high performance adaptive equalization receivers. High band receive data is typically better than low band due to the inherent design of PSK modems.

73K222AU
BER vs S/N



73K222AU
BER vs RECEIVE LEVEL

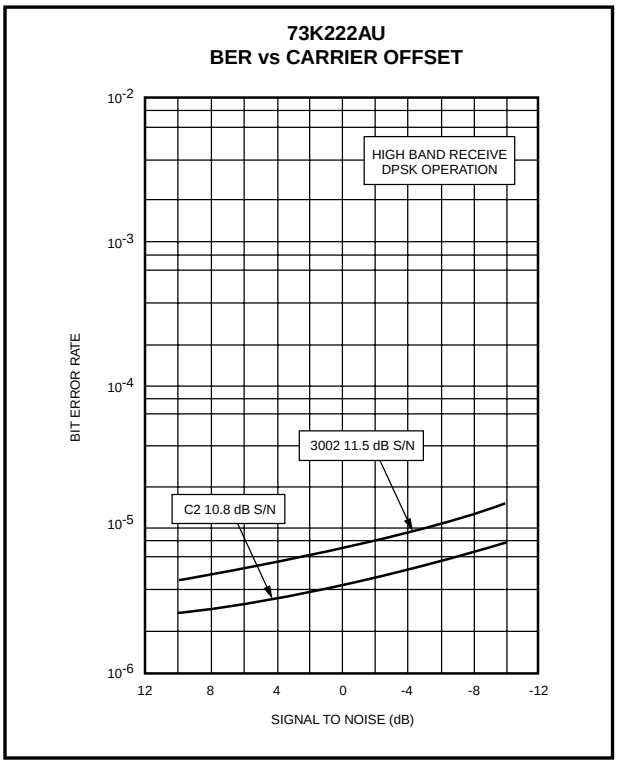


BER vs. Receive Level

This measures the dynamic range of the modem. As signal levels vary widely over dial-up lines, the widest dynamic range possible is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios were held constant at the indicated values while receive level was lowered from very high to very low signal levels. The "width of the bowl" of these curves taken at the 10^{-4} BER point is a measure of the dynamic range.

BER vs. Carrier Offset

This parameter indicates how the modem performance is impacted by frequency shifts encountered in normal PSTN operation. Flat curves show no performance degradation from frequency offsets. The K-Series devices use a 2nd order carrier tracking phase-locked-loop, which is insensitive to carrier offsets in excess of 10 Hz. The Bell network specifications allow as much as 7 Hz offset, and the CCITT specifications require modems to operate with 7 Hz of offset.



APPLICATION

The 73K222AU includes additional circuitry to greatly simplify integral modem designs in either of two different configurations. The single-port mode represents the most efficient implementation for an integral modem. Figure 9 shows a typical schematic using this mode. In this configuration, the 73K222AU transfers data and commands through the single parallel port. All modem control is provided by the main CPU, eliminating the need for an external microcontroller and supporting components. The 73K222AU is unique in that access to both the UART and modem sections is possible through the UART port. Also shown is a separate serial port, which can be used independent of the modem function when the modem section is inactive. Figure 10 shows a more conventional integral modem design, in which a local microprocessor handles modem supervision, allowing the modem function to be transparent to the main processor. Inclusion of the hybrid drivers, audio volume control, and off hook relay driver reduces component count for a highly efficient design. In either mode of operation, the 73K222AU's ability to operate from a single +5 volt power supply eliminates the need for additional supply voltages and keeps power usage to a minimum.

(See Figure 9 & 10: Typical Integral Applications Single and Dual-Port Modes.)

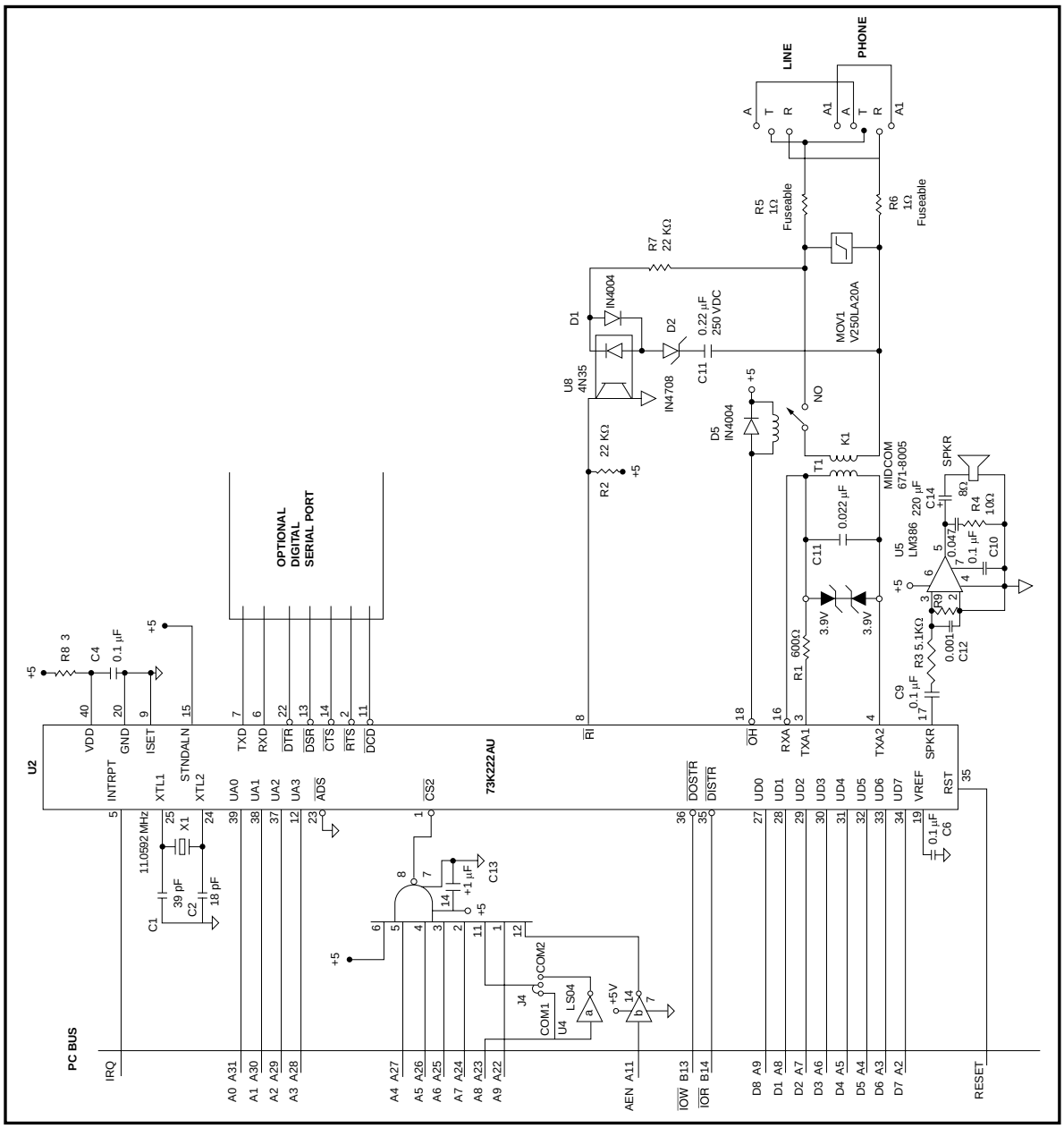


FIGURE 9: 73K222AU Typical Integral Application Single-Port Mode

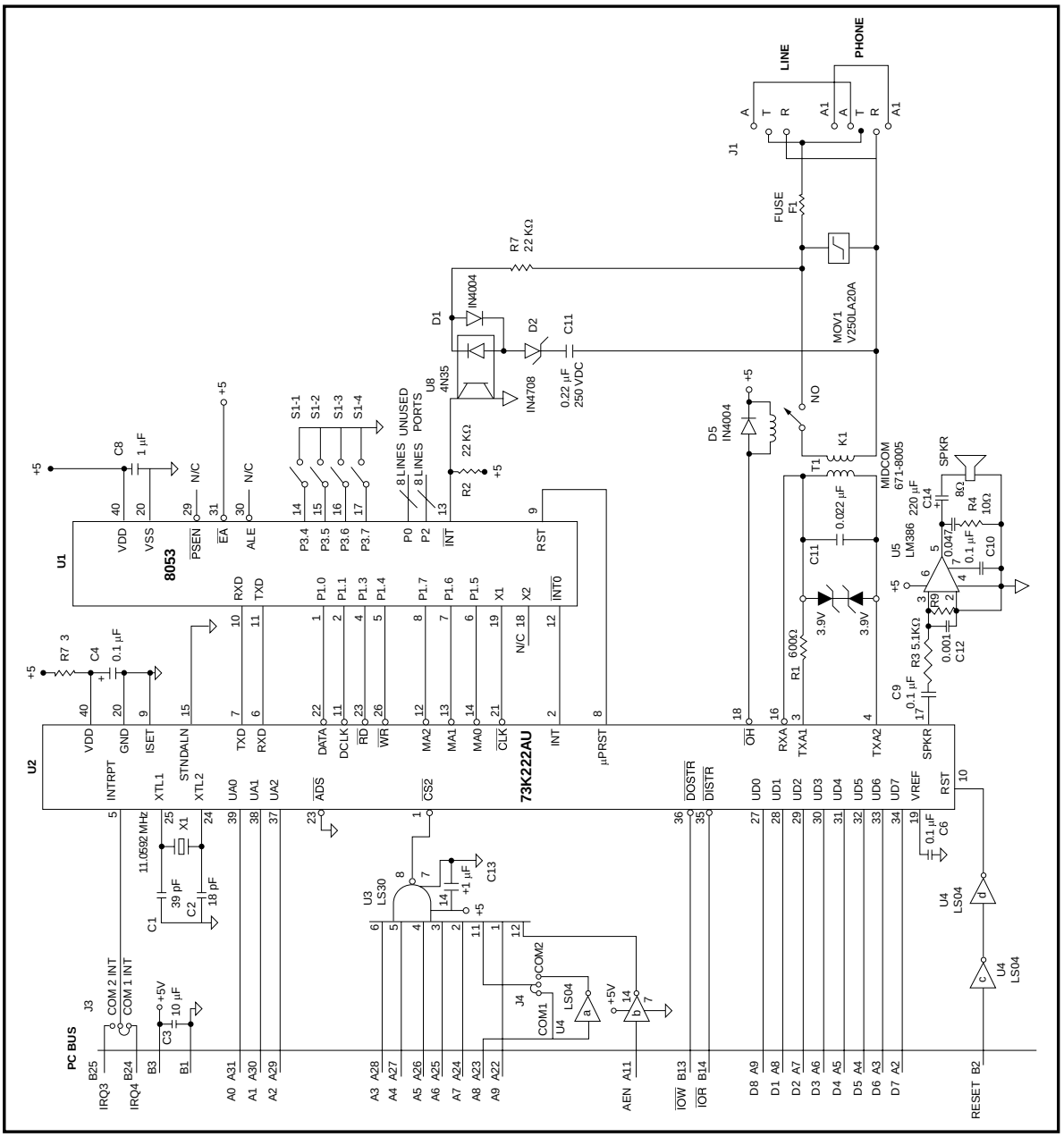
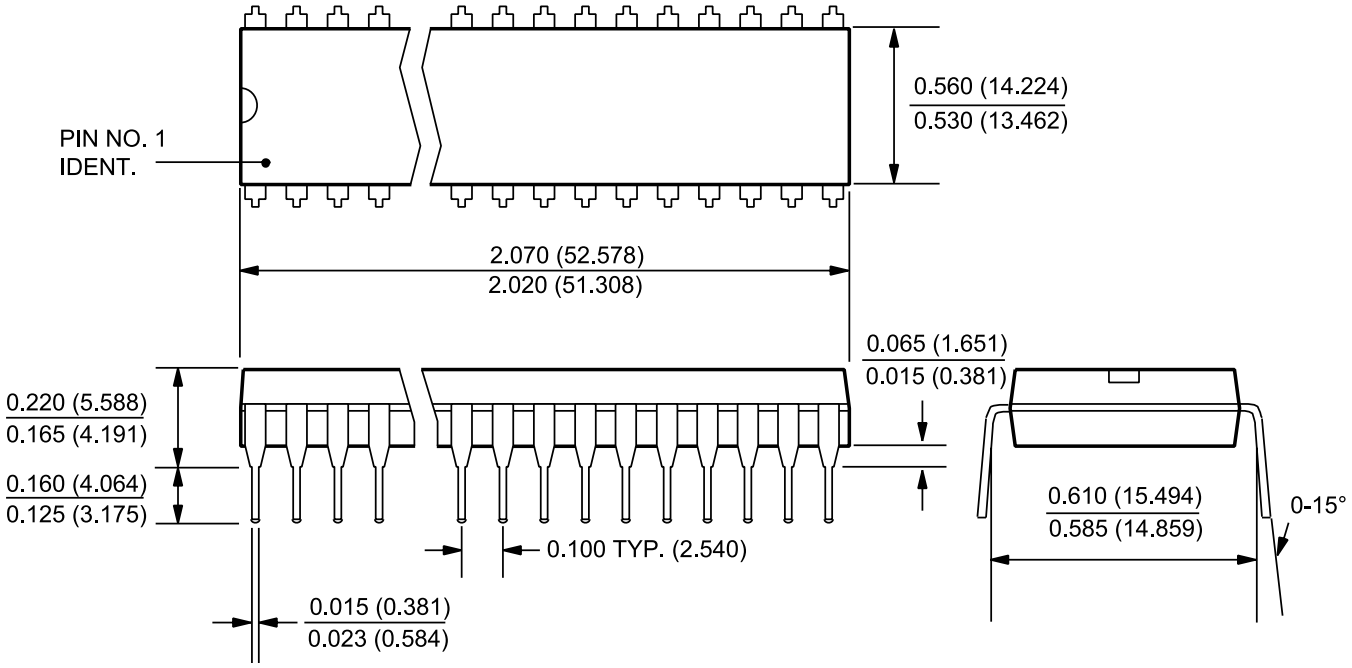


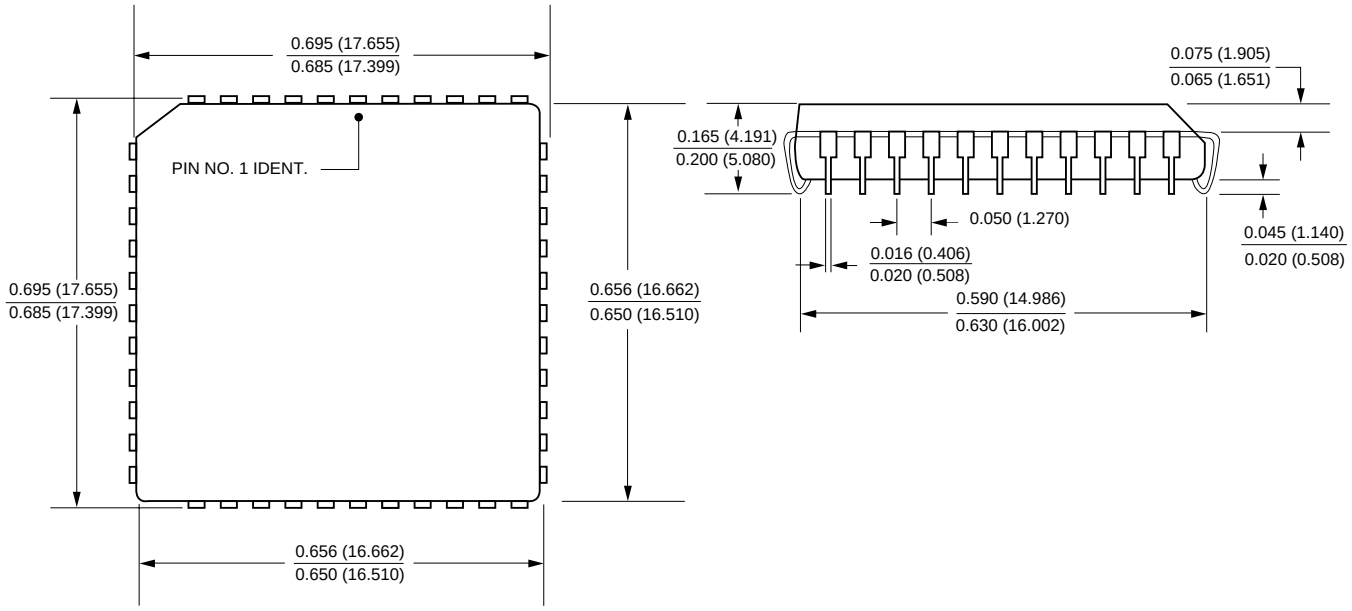
FIGURE 10: 73K222AU Typical Integral Application Dual-Port Mode

MECHANICAL SPECIFICATIONS

40-Pin DIP



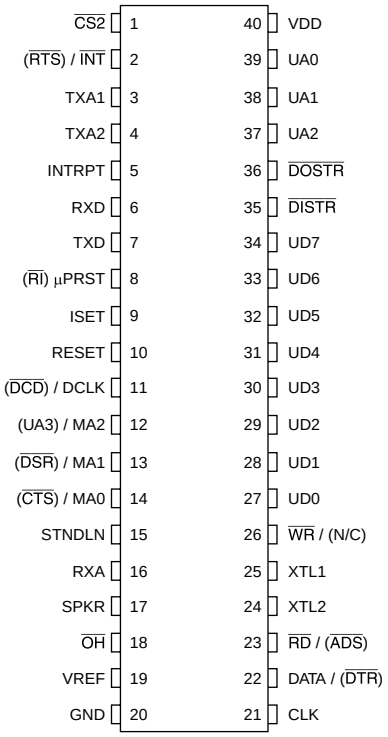
44-Pin PLCC



PACKAGE PIN DESIGNATIONS

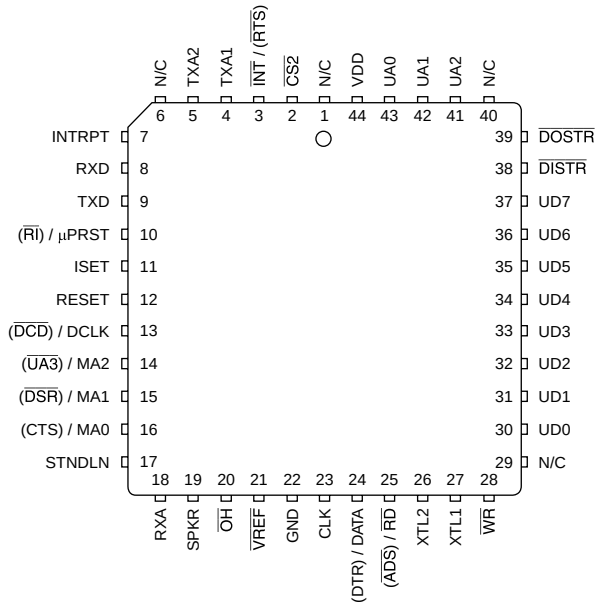
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



600-Mil
40-Pin DIP
73K222AU-IP

Parentheses indicate single-port mode.



44-Pin
PLCC
73K222AU-IH

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGING MARK
73K222AU		
40-Pin Plastic Dual In-Line	73K222AU-IP	73K222AU-IP
44-Pin Plastic Leaded Chip Carrier	73K222AU-IH	73K222AU-IH

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htt://www.teridiansemi.com

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