54/74125
54LS/74LS125A

QUAD BUS BUFFER GATE

(With 3-State Outputs)

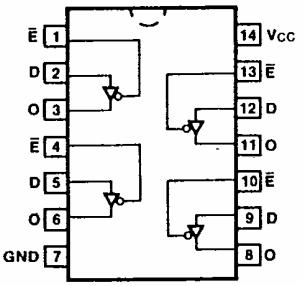
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74125PC, 74LS125APC		9A
Ceramic DIP (D)	A	74125DC, 74LS125ADC	54125DM, 54LS125ADM	6A
Flatpak (F)	A	74125FC, 74LS125AFC	54125FM, 54LS125AFM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	0.5/0.25
Outputs	130/10 (50)	65/15 (25)/(7.5)

CONNECTION DIAGRAM
PINOUT A



TRUTH TABLE

INPUTS		OUTPUT
Ē	D	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

DC AND AC CHARACTERISTICS: See Seciton 3*

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	XM	2.4				V	I_{OH} = -2.0 mA; V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}
		XC	2.4					I_{OH} = -5.2 mA
		XM			2.4			I_{OH} = -1.0 mA
		XC			2.4			I_{OH} = -2.6 mA
I_{OS}	Output Short Circuit Current	XM	-30	-70	-30	-130	mA	V_{CC} = Max
		XC	-28	-70	-30	-130		
I_{CC}	Power Supply Current			54		20	mA	Outputs OFF, V_{IN} = Gnd V_E = 4.5 V, V_{CC} = Max
t_{PLH} t_{PHL}	Propagation Delay Data to Output			13 18		15 18	ns	Figs. 3-3, 3-5
t_{PZH} t_{PZL}	Output Enable Time			17 25		16 25	ns	Figs. 3-3, 3-11, 3-12
t_{PLZ} t_{PHZ}	Output Disable Time			8.0 12		25 25	ns	Figs. 3-3, 3-11, 3-12

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.