

MM54HCT640/MM74HCT640 Inverting Octal TRI-STATE® Transceiver

MM54HCT643/MM74HCT643 True-Inverting Octal TRI-STATE Transceiver

General Description

These TRI-STATE bi-directional transceivers utilize advanced silicon-gate CMOS technology and are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power consumption of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits.

All devices are TTL input compatible and can drive up to 15 LS-TTL loads, and all inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Both the MM54HCT640/MM74HCT640 and the MM54HCT643/MM74HCT643 have one active low enable input (\bar{G}), and a direction control (DIR). When the DIR input is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from B to A. The MM54HCT640/

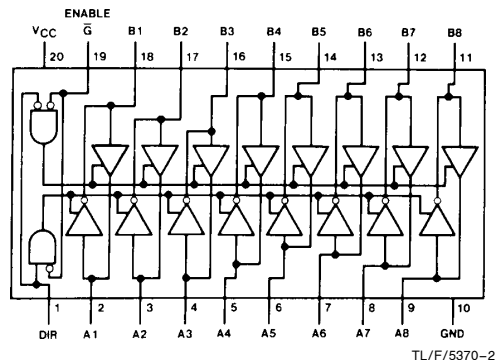
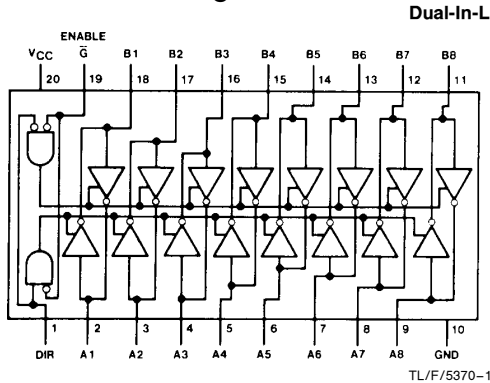
MM74HCT640 transfers inverted data from one bus to the other. The MM54HCT643/MM74HCT643 transfers inverted data from the A bus to the B bus and non-inverted data from the B bus to the A bus.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL input compatible
- Octal TRI-STATE outputs for μP bus applications: 6 mA, typical
- High speed: 16 ns typical propagation delay
- Low power: 80 μA maximum (74HCT)

Connection Diagram



Truth Table

Control Inputs	Operation	
	640	643
\bar{G} DIR	640	643
L L	\bar{B} data to A bus	B data to A bus
L H	\bar{A} data to B bus	\bar{A} data to B bus
H X	Isolation	Isolation

H = high level, L = low level, X = irrelevant

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input Voltage (V_{IN})	-1.5 to $V_{CC} + 1.5V$
DC Output Voltage (V_{OUT})	-0.5 to $V_{CC} + 0.5V$
Clamp Diode Current (I_{IK}, I_{OK})	± 20 mA
DC Output Current, per pin (I_{OUT})	± 35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	± 70 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	-40	+85	°C
MM54HCT	-55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics $V_{CC} = 5V \pm 10\%$ (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A = 25^\circ C$		74HCT	54HCT	Units
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_{OUT} = 20 \mu A$ $I_{OUT} = 6.0 mA, V_{CC} = 4.5V$ $I_{OUT} = 7.2 mA, V_{CC} = 5.5V$	V_{CC}	$V_{CC}-0.1$	$V_{CC}-0.1$	$V_{CC}-0.1$	V
			4.2	3.98	3.84	3.7	V
			5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_{OUT} = 20 \mu A$ $I_{OUT} = 6.0 mA, V_{CC} = 4.5V$ $I_{OUT} = 7.2 mA, V_{CC} = 5.5V$	0	0.1	0.1	0.1	V
			0.2	0.26	0.33	0.4	V
			0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND, V_{IH} or V_{IL}		± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND Enable $\bar{G} = V_{IH}$		± 0.5	± 5.0	± 10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$		8	80	160	μA
		$V_{IN} = 2.4V$ or $0.5V$ (Note 4)	0.6	1.0	1.3	1.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

Note 4: Measured per input. All other inputs held at V_{CC} or ground.

AC Electrical Characteristics MM54HCT640/MM74HCT640

$V_{CC} = 5.0V, t_r = t_f = 6$ ns, $T_A = 25^\circ C$ (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	$C_L = 45$ pF	16	20	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$C_L = 45$ pF $R_L = 1$ k Ω	29	40	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	$C_L = 5$ pF $R_L = 1$ k Ω	20	25	ns

AC Electrical Characteristics MM54HCT640/MM74HCT640

$V_{CC} = 5.0V \pm 10\%$, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A = 25^\circ\text{C}$		74HCT	54HCT	Units
			Typ	Guaranteed Limits		$T_A = -40$ to 85°C	
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	$C_L = 50$ pF	17	23	29	34	ns
		$C_L = 150$ pF	24	30	38	45	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1$ k Ω , $C_L = 50$ pF	23	30	38	45	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1$ k Ω , $C_L = 50$ pF	21	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L = 50$ pF	8	12	15	18	ns
C_{IN}	Maximum Input Capacitance		10	15	15	15	pF
C_{OUT}	Maximum Output/ Input Capacitance		20	25	25	25	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per output) $\bar{G} = V_{CC}$	7				pF
		$\bar{G} = \text{GND}$	100				pF

AC Electrical Characteristics MM54HCT643/MM74HCT643

$V_{CC} = 5.0V$, $t_r = t_f = 6$ ns, $T_A = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	$C_L = 45$ pF	16	20	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$C_L = 45$ pF, $R_L = 1$ k Ω	29	40	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	$C_L = 5$ pF, $R_L = 1$ k Ω	20	25	ns

AC Electrical Characteristics MM54HCT643/MM74HCT643

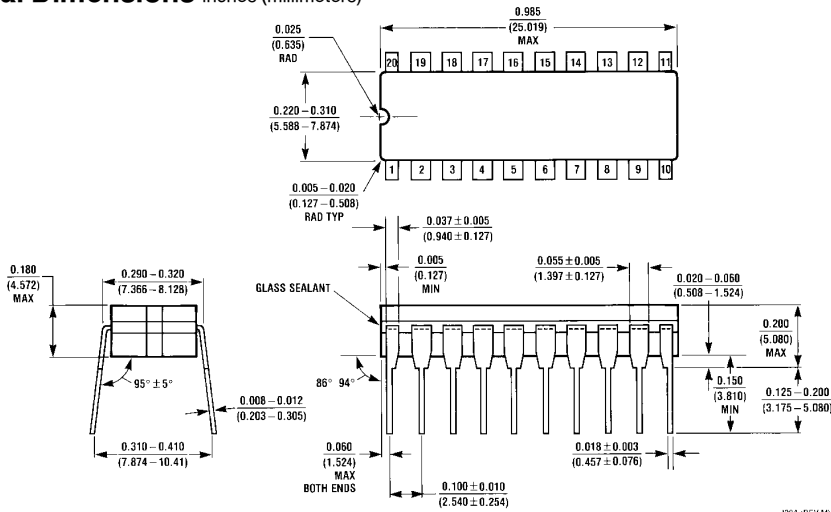
$V_{CC} = 5.0V \pm 10\%$, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A = 25^\circ\text{C}$		74HCT	54HCT	Units
			Typ	Guaranteed Limits		$T_A = -40$ to 85°C	
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	$C_L = 50$ pF	17	23	29	34	ns
		$C_L = 150$ pF	24	30	38	45	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1$ k Ω , $C_L = 50$ pF	23	30	38	45	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1$ k Ω , $C_L = 50$ pF	21	30	38	45	ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L = 50$ pF	8	12	15	18	ns
C_{IN}	Maximum Input Capacitance		10	15	15	15	pF
C_{OUT}	Maximum Output/ Input Capacitance		20	25	25	25	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per output) $\bar{G} = V_{CC}$	7				pF
		$\bar{G} = \text{GND}$	100				pF

Note 5: C_{PD} determines the no load power consumption. $P_D = C_{PD}V_{CC}^2f + I_{CC}V_{CC}$. The no load dynamic current consumption, $I_S = C_{PD}V_{CC} + I_{CC}$.

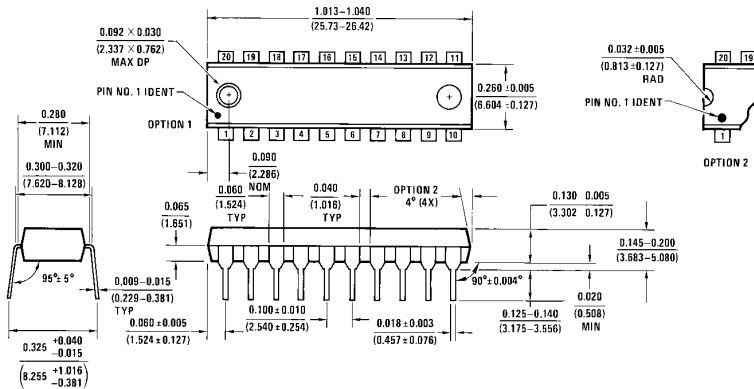
MM54HCT640/MM74HCT640 Inverting Octal TRI-STATE Transceiver
MM54HCT643/MM74HCT643 True-Inverting Octal TRI-STATE Transceiver

Physical Dimensions inches (millimeters)



J20A (REV M)

Cavity Dual-In line Package (J)
Order Number MM54HCT640J, MM54HCT643J, MM74HCT640J, or MM74HCT643J
See NS Package J20A



N20A (REV G)

Moulded Dual-In line Package (N)
Order Number MM74HCT640N or MM74HCT643N
See NS Package N20A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Corporation
 1111 West Bardin Road
 Arlington, TX 76017
 Tel: 1(800) 272-9959
 Fax: 1(800) 737-7018

National Semiconductor Europe
 Fax: (+49) 0-180-530 85 86
 Email: cnjwge@tevm2.nsc.com
 Deutsch Tel: (+49) 0-180-530 85 85
 English Tel: (+49) 0-180-532 78 32
 Français Tel: (+49) 0-180-532 93 58
 Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
 19th Floor, Straight Block,
 Ocean Centre, 5 Canton Rd.
 Tsimshatsui, Kowloon
 Hong Kong
 Tel: (852) 2737-1600
 Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
 Tel: 81-043-299-2309
 Fax: 81-043-299-2408

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.