54/7480
GATED FULL ADDER

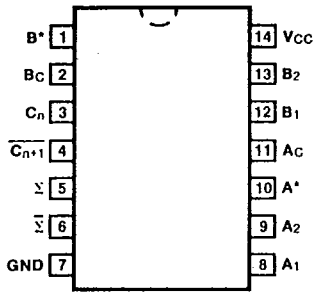
DESCRIPTION — The '80 is a single-bit, high speed, binary full adder with gated complementary inputs, complementary sum (Σ and $\overline{\Sigma}$) outputs and inverted carry output. It is designed for medium and high speed, multiple-bit, parallel-add/serial carry applications. The circuit utilizes DTL for the gated inputs and high speed, high fan-out TTL for the sum and carry outputs. The circuit is entirely compatible with both DTL and TTL logic families. The implementation of a single-inversion, high speed, Darlington-connected serial-carry circuit minimizes the necessity for extensive "lookahead" and carry-cascading circuits.

ORDERING CODE: See Section 9

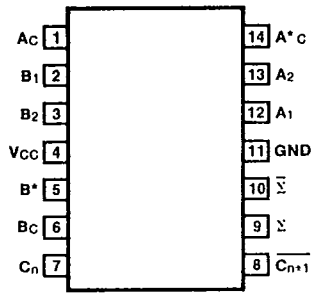
PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7480PC		9A
Ceramic DIP (D)	A	7480DC	5480DM	6A
Flatpak (F)	B	7480FC	5480FM	3I

CONNECTION DIAGRAMS

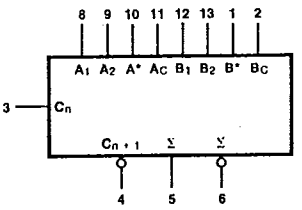
PINOUT A



PINOUT B



LOGIC SYMBOL



Vcc = Pin 14
GND = Pin 7

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
A_1, A_2, B_1, B_2	Operand Inputs	0.4/1.0
A*, B*	Inverted Operand Inputs	-/1.63
Ac, Bc	Control Inputs	0.4/1.0
C_n	Carry Input	5.0/5.0
$\overline{C_{n+1}}$	Inverted Carry Output	5.0/5.0
Σ, $\overline{\Sigma}$	Sum Outputs	10/10
A*, B*	When Used As Outputs	3.0/3.0

TRUTH TABLE

INPUTS			OUTPUTS		
C_n	B	A	$\overline{C_{n+1}}$	$\overline{\Sigma}$	Σ
L	L	L	H	H	L
L	L	H	H	L	H
L	H	L	H	L	H
L	H	H	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	H	L	L	H	L
H	H	H	L	L	H

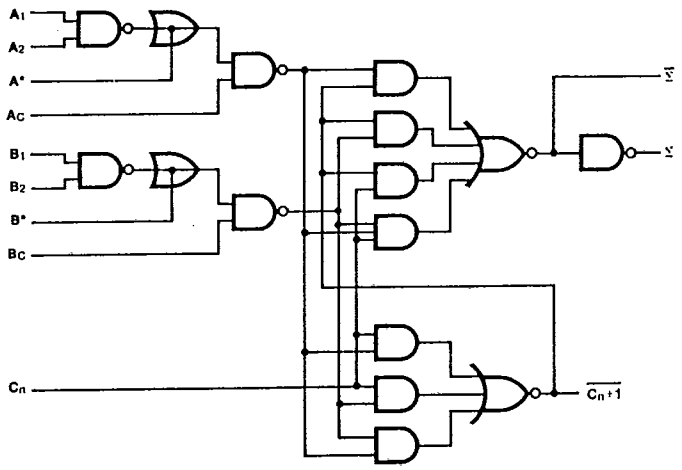
NOTES:

(1) $A = \overline{A^* \bullet A_C}$, $B = \overline{B^* \bullet B_C}$ where $\overline{A_1 \bullet A_2}$. $B^* = \overline{B_1 \bullet B_2}$

(2) When A^* or B^* are used as inputs, A_1 and A_2 or B_1 and B_2 respectively must be connected to Gnd.

(3) When A_1 and A_2 or B_1 and B_2 are used as inputs, A^* or B^* respectively must be open or used to perform Dot-OR logic.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unlsess otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current at $\overline{C_{n+1}}$	XM	-20	-70	mA	V_{CC} = Max
		XC	-18	-70		
I_{OS}	Output Short Circuit Current at A^*, B^*	XM	-0.9	-2.9	mA	V_{CC} = Max
		XC	-0.9	-2.9		
I_{CC}	Power Supply Current	XM		31	mA	V_{CC} = Max
		XC		35		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF Min	54/74 C_L = 15 pF Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay C_n to $\overline{C_{n+1}}$		17 12	ns	Figs. 3-1, 3-4 R_L = 780 Ω
t_{PLH} t_{PHL}	Propagation Delay B_C to $\overline{C_{n+1}}$		25 55	ns	Figs. 3-1, 3-5 R_L = 780 Ω
t_{PLH} t_{PHL}	Propagation Delay A_C to Σ		70 80	ns	Figs. 3-1, 3-4 R_L = 400 Ω
t_{PLH} t_{PHL}	Propagation Delay B_C to $\overline{\Sigma}$		55 75	ns	Figs. 3-1, 3-5 R_L = 400 Ω
t_{PLH} t_{PHL}	Propagation Delay A_1 to A^* or B_1 to B^*		65 25	ns	Figs. 3-1, 3-4 R_L not used