FAIRCHILD
SEMICONDUCTOR™

April 1992
Revised November 1999

74ABT162244
16-Bit Buffer/Line Driver with 25Ω Series Resistors in the Outputs

General Description

The ABT162244 contains sixteen non-inverting buffers with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Individual 3-STATE control inputs can be shorted together for 8-bit or 16-bit operation.

The 25Ω series resistors in the outputs reduce ringing and eliminate the need for external resistors.

Features

■ Separate control logic for each nibble
■ 16-bit version of the ABT2244
■ Guaranteed latchup protection
■ High impedance glitch free bus loading during entire power up and power down cycle
■ Non-destructive hot insertion capability

Ordering Code:

Order Number	Package Number	Package Description
74ABT162244CSSC	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ABT162244CMTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol
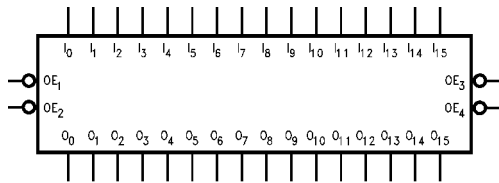
Connection Diagram
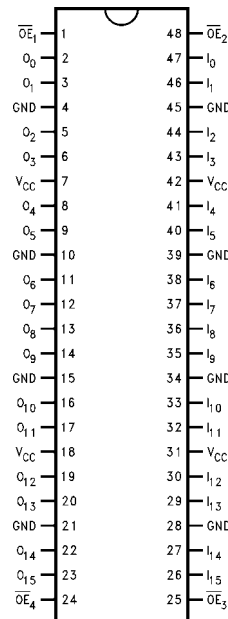
Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
I_0–I_{15}	Inputs
O_0–O_{15}	Outputs

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$I_0 - I_3$	$O_0 - O_3$
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	$I_8 - I_{11}$	$O_8 - O_{11}$
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	$I_4 - I_7$	$O_4 - O_7$
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	$I_{12} - I_{15}$	$O_{12} - O_{15}$
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
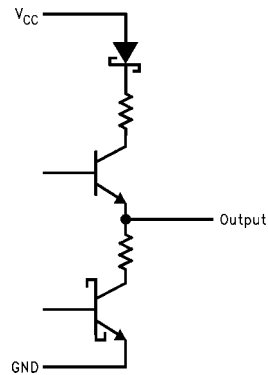X = Immaterial
Z = High Impedance

Functional Description

The ABT162244 contains sixteen non-inverting buffers with 3-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

Logic Diagram
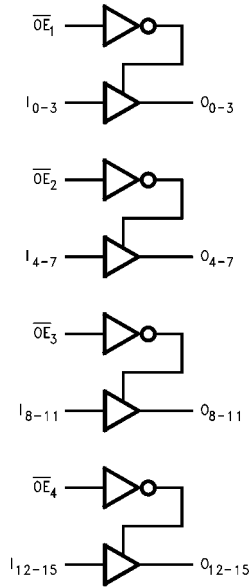
Schematic of each Output

Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or	
Power-Off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	−40°C to +85°C
Supply Voltage	+4.5V to +5.5V
Minimum Input Edge Rate (ΔV/Δt)	
Data Input	50 mV/ns
Enable Input	20 mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage		2.5			V	Min	I_{OH} = −3 mA
			2.0			V	Min	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage				0.8	V	Min	I_{OL} = 12 mA
I_{IH}	Input HIGH Current				1	μA	Max	V_{IN} = 2.7V (Note 3)
					1			V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−1	μA	Max	V_{IN} = 0.5V (Note 3)
					−1			V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA
								All Other Pins Grounded
I_{OZH}	Output Leakage Current				10	μA	0 – 5.5V	V_{OUT} = 2.7V; $\overline{OE}_n$ = 2.0V
I_{OZL}	Output Leakage Current				−10	μA	0 – 5.5V	V_{OUT} = 0.5V; $\overline{OE}_n$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.5V; All Others GND
I_{CCH}	Power Supply Current				2.0	mA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				60	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				2.0	mA	Max	$\overline{OE}_n$ = V_{CC}
								All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled			3.0	mA		V_I = V_{CC} − 2.1V
		Outputs 3-STATE			3.0	mA	Max	Enable Input V_I = V_{CC} − 2.1V
		Outputs 3-STATE			50	μA		Data Input V_I = V_{CC} − 2.1V
								All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC}	No Load				mA/	Max	Outputs OPEN
	(Note 3)				0.1	MHz		$\overline{OE}_n$ = GND
								One Bit Toggling, 50% Duty Cycle

Note 3: Guaranteed, but not tested.

AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$ $V_{CC} = +5V$ $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
t_{PLH}	Propagation	1.0	2.4	3.9	1.0	3.9	ns
t_{PHL}	Delay Data to Outputs	1.0	3.2	4.7	1.0	4.7	
t_{PZH}	Output	1.5	3.5	6.3	1.5	6.3	ns
t_{PZL}	Enable Time	1.5	4.2	6.9	1.5	6.9	
t_{PHZ}	Output	1.0	4.2	6.7	1.0	6.7	ns
t_{PLZ}	Disable Time	1.0	3.8	6.7	1.0	6.7	

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25°C$
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0.0V$
C_{OUT} (Note 4)	Output Capacitance	9.0	pF	$V_{CC} = 5.0V$

Note 4: C_{OUT} is measured at frequency f = 1 MHz per MIL-STD-883, Method 3012.

AC Loading
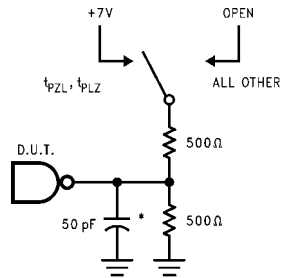
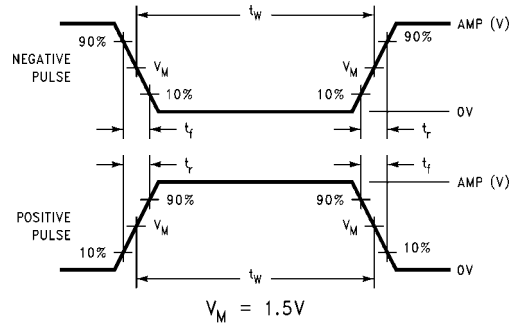*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

$V_M = 1.5V$

FIGURE 2. Input Pulse Requirements

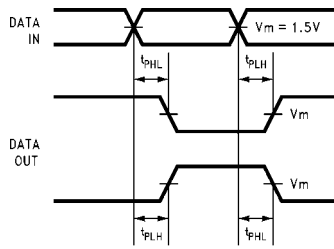| Amplitude	Rep. Rate	t_W	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

AC Waveforms

**FIGURE 4. Propagation Delay Waveforms for Inverting
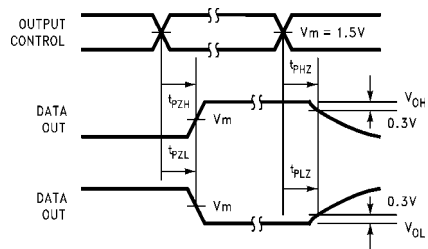and Non-Inverting Functions**

**FIGURE 6. 3-STATE Output HIGH
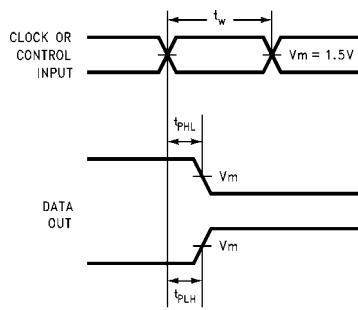and LOW Enable and Disable Times**
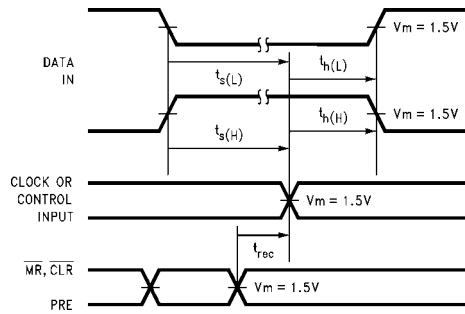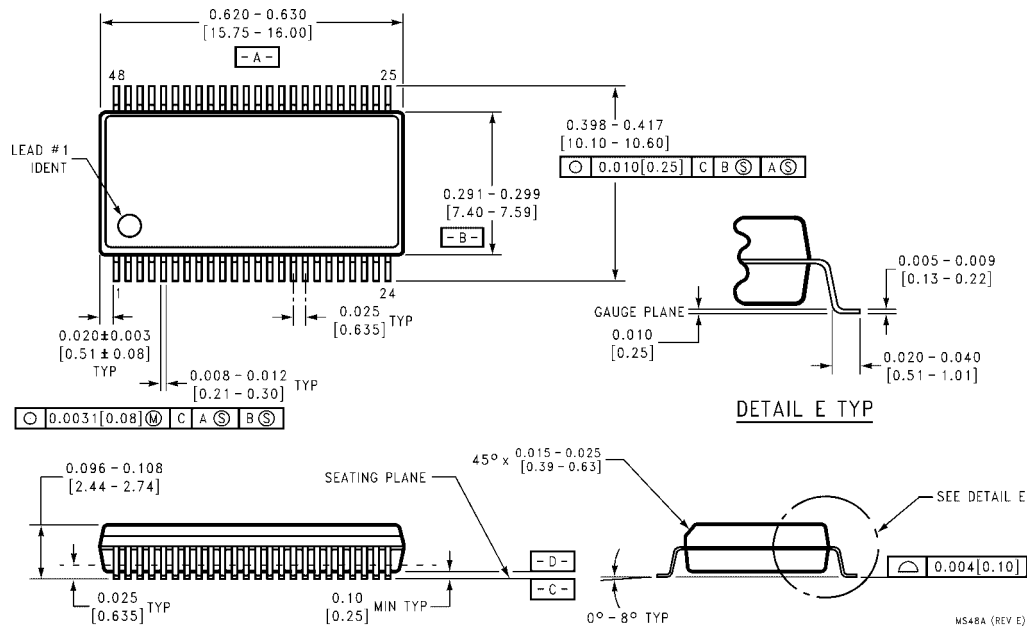

**FIGURE 5. Propagation Delay,
Pulse Width Waveforms**

**FIGURE 7. Setup Time, Hold Time
and Recovery Time Waveforms**

Physical Dimensions inches (millimeters) unless otherwise noted

0.620 – 0.630
[15.75 – 16.00]
– A –

48   25

LEAD #1
IDENT

0.398 – 0.417
[10.10 – 10.60]
⌀ | 0.010[0.25] | C | B Ⓢ | A Ⓢ

0.291 – 0.299
[7.40 – 7.59]
– B –

1   24

0.025
[0.635] TYP

0.020±0.003
[0.51±0.08]
TYP

0.008 – 0.012
[0.21 – 0.30] TYP

⌀ | 0.0031[0.08]Ⓜ | C | A Ⓢ | B Ⓢ

GAUGE PLANE

0.010
[0.25]

0.005 – 0.009
[0.13 – 0.22]

0.020 – 0.040
[0.51 – 1.01]

DETAIL E TYP

0.096 – 0.108
[2.44 – 2.74]

SEATING PLANE

45° x 0.015 – 0.025
[0.39 – 0.63]

SEE DETAIL E

– D –
– C –

0.025
[0.635] TYP

0.10
[0.25] MIN TYP

0° – 8° TYP

⌂ | 0.004[0.10]

MS48A (REV E)

48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

DIMENSIONS ARE IN MILLIMETERS

NOTES:
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48RevB1

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

www.fairchildsemi.com