# DATA SHEET



## 74ABT16841A
## 74ABTH16841A
20-bit bus interface latch (3-State)

Product specification
Supersedes data of 1995 Sep 28
IC23 Data Handbook

1998 Feb 27

Philips
Semiconductors

PHILIPS

# 20-bit bus interface latch (3-State)

# 74ABT16841A
# 74ABTH16841A

## FEATURES

- High speed parallel latches
- Live insertion/extraction permitted
- Extra data width for wide address/data paths or buses carrying parity
- Power-up 3-State
- 74ABTH16841A incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Power-up reset
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

## DESCRIPTION

The 74ABT16841A Bus interface latch is designed to provide extra data width for wider data/address paths of buses carrying parity.

The 74ABT16841A consists of two sets of ten D-type latches with 3-State outputs. The flip-flops appear transparent to the data when Latch Enable (nLE) is High. This allows asynchronous operation, as the output transition follows the data in transition. On the nLE High-to-Low transition, the data that meets the setup and hold time is latched.

Data appears on the bus when the Output Enable ($n\overline{OE}$) is Low. When $n\overline{OE}$ is High the output is in the High-impedance state.

Two options are available, 74ABT16841A which does not have the bus-hold feature and 74ABTH16841A which incorporates the bus-hold feature.

## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS $T_{amb}$ = 25°C; GND = 0V | TYPICAL | UNIT |
|---|---|---|---|---|
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>nDx to nQx | $C_L$ = 50pF; $V_{CC}$ = 5V | 3.1<br>2.2 | ns |
| $C_{IN}$ | Input capacitance | $V_I$ = 0V or $V_{CC}$ | 4 | pF |
| $C_{OUT}$ | Output capacitance | $V_O$ = 0V or $V_{CC}$; 3-State | 7 | pF |
| $I_{CCZ}$ | Quiescent supply current | Outputs disabled; $V_{CC}$ = 5.5V | 500 | µA |
| $I_{CCL}$ | | Outputs LOW; $V_{CC}$ = 5.5V | 10 | mA |

## ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | DWG NUMBER |
|---|---|---|---|---|
| 56-Pin Plastic SSOP Type III | –40°C to +85°C | 74ABT16841A DL | BT16841A DL | SOT371-1 |
| 56-Pin Plastic TSSOP Type II | –40°C to +85°C | 74ABT16841A DGG | BT16841A DGG | SOT364-1 |
| 56-Pin Plastic SSOP Type III | –40°C to +85°C | 74ABTH16841A DL | BH16841A DL | SOT371-1 |
| 56-Pin Plastic TSSOP Type II | –40°C to +85°C | 74ABTH16841A DGG | BH16841A DGG | SOT364-1 |

## PIN DESCRIPTION

| PIN NUMBER | SYMBOL | FUNCTION |
|---|---|---|
| 55, 54, 52, 51, 49, 48, 47, 45, 44, 43<br>42, 41, 40, 38, 37, 36, 34, 33, 31, 30 | 1D0 – 1D9<br>2D0 – 2D9 | Data inputs |
| 2, 3, 5, 6, 8, 9, 10, 12, 13, 14<br>15, 16, 17, 19, 20, 21, 23, 24, 26, 27 | 1Q0 – 1Q9<br>2Q0 – 2Q9 | Data outputs |
| 1, 28 | $1\overline{OE}$, $2\overline{OE}$ | Output enable inputs (active-Low) |
| 56, 29 | 1LE, 2LE | Latch enable inputs (active rising edge) |
| 4, 11, 18, 25, 32, 39, 46, 53 | GND | Ground (0V) |
| 7, 22, 35, 50 | $V_{CC}$ | Positive supply voltage |

# 20-bit bus interface latch (3-State)

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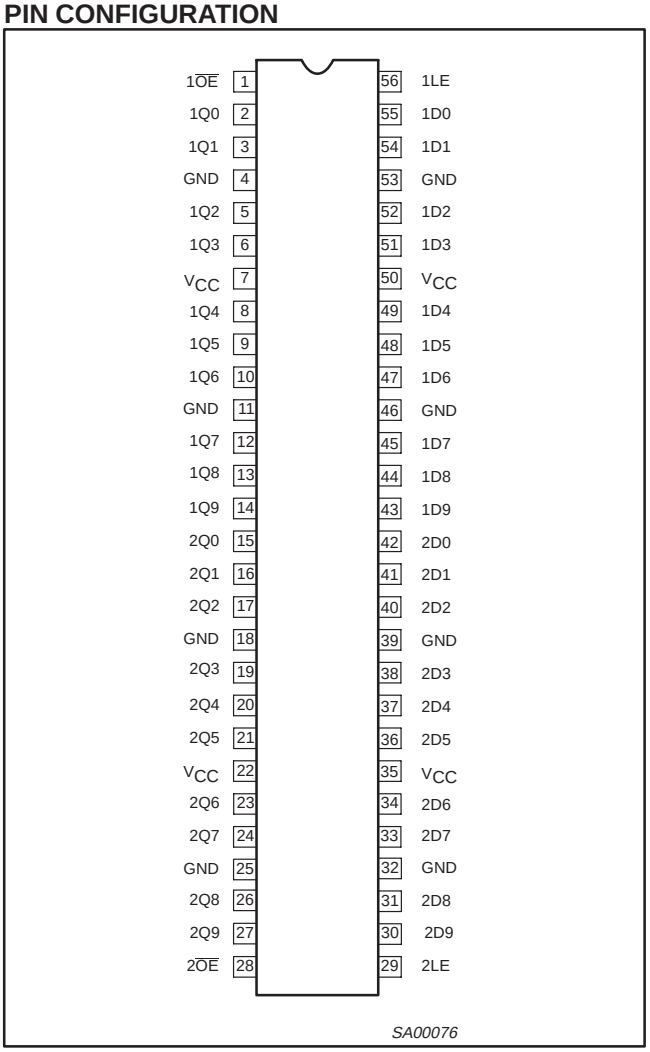
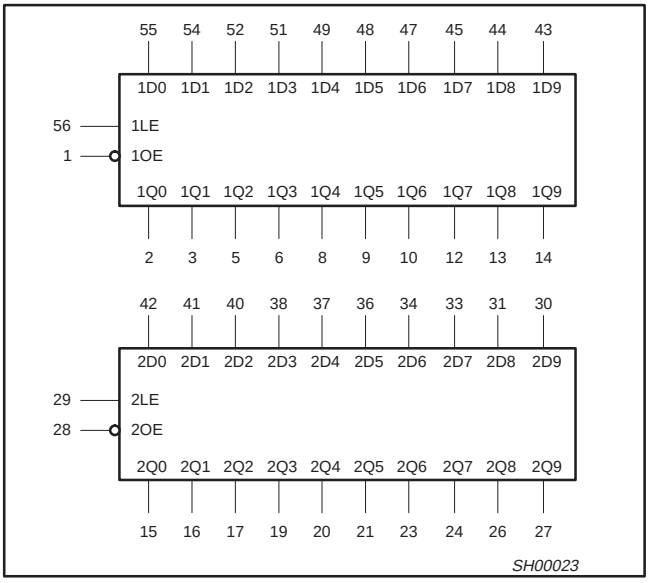
# 74ABTH16841A

## PIN CONFIGURATION



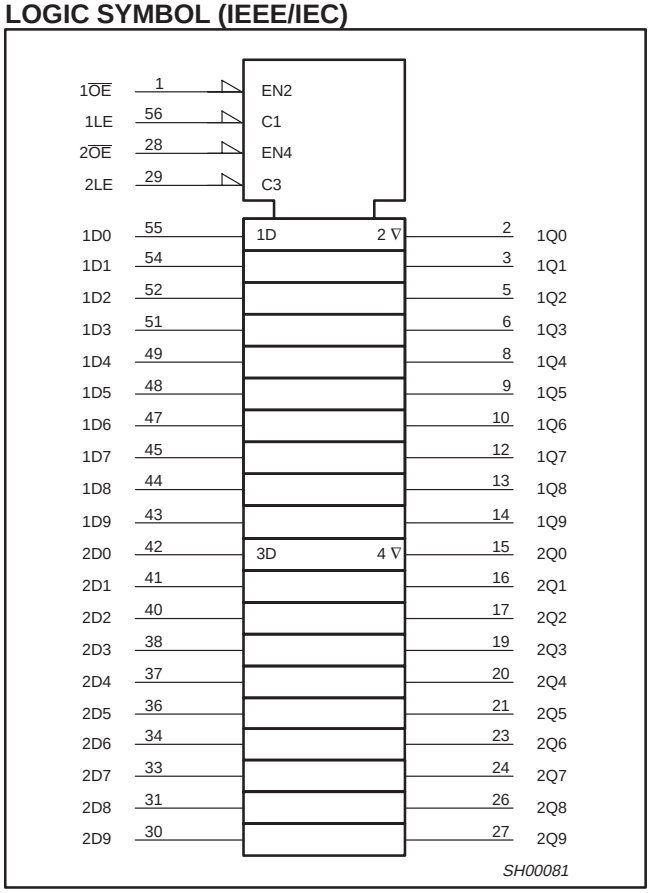

SA00076

## LOGIC SYMBOL




SH00023

## LOGIC SYMBOL (IEEE/IEC)



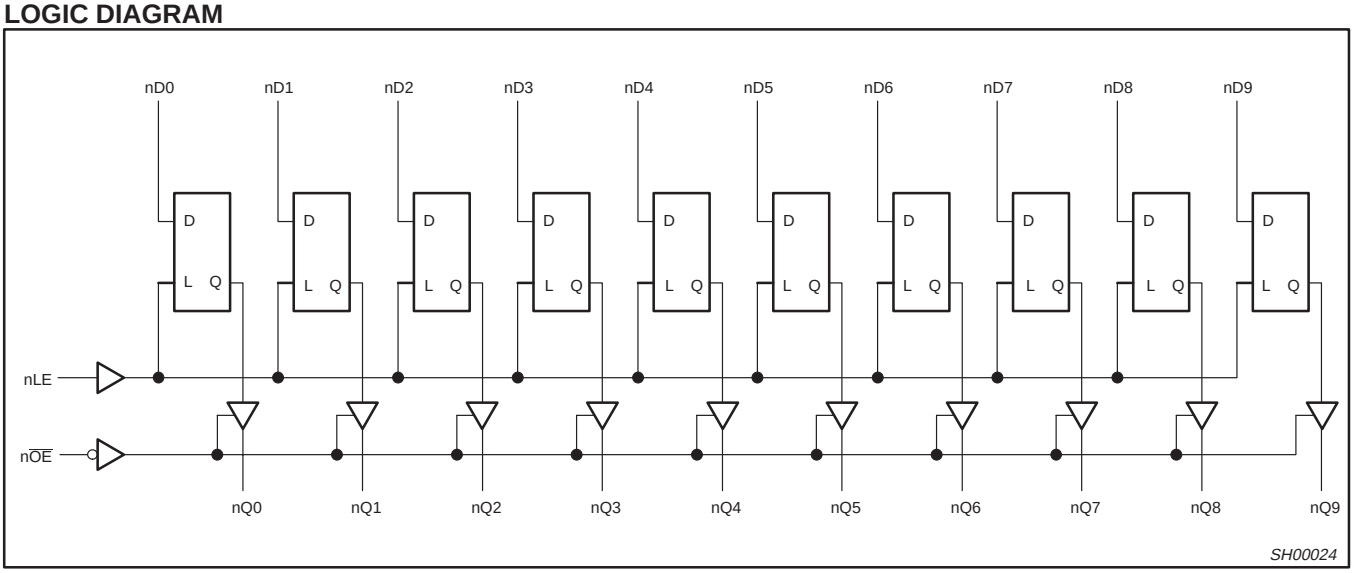

SH00081

## FUNCTION TABLE

| INPUTS | | | OUTPUTS | OPERATING MODE |
|---|---|---|---|---|
| n$\overline{OE}$ | nLE | nDx | nQ0 – nQ9 | |
| L<br>L | H<br>H | L<br>H | L<br>H | Transparent |
| L<br>L | ↓<br>↓ | l<br>h | L<br>H | Latched |
| H | X | X | Z | High impedance |
| L | L | X | NC | Hold |

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low LE transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low LE transition
↓ = High-to-Low LE transition
NC = No change
X = Don't care
Z = High impedance "off" state

## LOGIC DIAGRAM




## ABSOLUTE MAXIMUM RATINGS[1, 2]

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | DC supply voltage | | –0.5 to +7.0 | V |
| $I_{IK}$ | DC input diode current | $V_I < 0$ | –18 | mA |
| $V_I$ | DC input voltage[3] | | –1.2 to +7.0 | V |
| $I_{OK}$ | DC output diode current | $V_O < 0$ | –50 | mA |
| $V_{OUT}$ | DC output voltage[3] | Output in Off or High state | –0.5 to +5.5 | V |
| $I_{OUT}$ | DC output current | Output in Low state | 128 | mA |
| | | Output in High state | –64 | |
| $T_{stg}$ | Storage temperature range | | –65 to 150 | °C |

**NOTES:**
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | UNIT |
|---|---|---|---|---|
| | | Min | Max | |
| $V_{CC}$ | DC supply voltage | 4.5 | 5.5 | V |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | V |
| $V_{IH}$ | High-level input voltage | 2.0 | | V |
| $V_{IL}$ | Low-level Input voltage | | 0.8 | V |
| $I_{OH}$ | High-level output current | | –32 | mA |
| $I_{OL}$ | Low-level output current | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | 0 | 5 | ns/V |
| $T_{amb}$ | Operating free-air temperature range | –40 | +85 | °C |

## DC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITIONS | | LIMITS | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_{amb}$ = +25°C | | | $T_{amb}$ = -40°C to +85°C | | |
| | | | | Min | Typ | Max | Min | Max | |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = 4.5V; $I_{IK}$ = -18mA | | | –0.9 | –1.2 | | –1.2 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = 4.5V; $I_{OH}$ = -3mA; $V_I$ = $V_{IL}$ or $V_{IH}$ | | 2.5 | 2.9 | | 2.5 | | V |
| | | $V_{CC}$ = 5.0V; $I_{OH}$ = -3mA; $V_I$ = $V_{IL}$ or $V_{IH}$ | | 3.0 | 3.4 | | 3.0 | | V |
| | | $V_{CC}$ = 4.5V; $I_{OH}$ = -32mA; $V_I$ = $V_{IL}$ or $V_{IH}$ | | 2.0 | 2.4 | | 2.0 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = 4.5V; $I_{OL}$ = 64mA; $V_I$ = $V_{IL}$ or $V_{IH}$ | | | 0.42 | 0.55 | | 0.55 | V |
| $V_{RST}$ | Power-up output voltage[3] | $V_{CC}$ = 5.5V; $I_O$ = 1mA; $V_I$ = GND or $V_{CC}$ | | | 0.13 | 0.55 | | 0.55 | V |
| $I_I$ | Input leakage current 74ABT16841A | $V_{CC}$ = 5.5V; $V_I$ = $V_{CC}$ or GND | | | ±0.01 | ±1 | | ±1.0 | µA |
| $I_I$ | Input leakage current 74ABTH16841A | $V_{CC}$ = 5.5V; $V_I$ = $V_{CC}$ or GND | Control pins | | ±0.01 | ±1 | | ±1 | µA |
| | | $V_{CC}$ = 5.5V; $V_I$ = $V_{CC}$ | Data pins[5] | | 0.01 | 1 | | 1 | µA |
| | | $V_{CC}$ = 5.5V; $V_I$ = 0 | | | –2 | –3 | | –5 | µA |
| $I_{HOLD}$ | Bus Hold current inputs[6] 74ABTH16841A | $V_{CC}$ = 4.5V; $V_I$ = 0.8V | | 35 | | | 35 | | µA |
| | | $V_{CC}$ = 4.5V; $V_I$ = 2.0V | | –75 | | | –75 | | |
| | | $V_{CC}$ = 5.5V; $V_I$ = 0 to 5.5V | | ±800 | | | | | |
| $I_{OFF}$ | Power-off leakage current | $V_{CC}$ = 0.0V; $V_O$ or $V_I \leq$ 4.5V | | | ±5.0 | ±100 | | ±100 | µA |
| $I_{PU/PD}$ | Power-up/down 3-State output current[4] | $V_{CC}$ = 2.1V; $V_O$ = 0.5V; $V_I$ = GND or $V_{CC}$; $\overline{V_{OE}}$ = Don't care | | | ±5.0 | ±50 | | ±50 | µA |
| $I_{OZH}$ | 3-State output High current | $V_{CC}$ = 5.5V; $V_O$ = 2.7V; $V_I$ = $V_{IL}$ or $V_{IH}$ | | | 5.0 | 10 | | 10 | µA |
| $I_{OZL}$ | 3-State output Low current | $V_{CC}$ = 5.5V; $V_O$ = 0.5V; $V_I$ = $V_{IL}$ or $V_{IH}$ | | | –5.0 | –10 | | –10 | µA |
| $I_{CEX}$ | Output High leakage current | $V_{CC}$ = 5.5V; $V_O$ = 5.5V; $V_I$ = GND or $V_{CC}$ | | | 5.0 | 50 | | 50 | µA |
| $I_O$ | Output current[1] | $V_{CC}$ = 5.5V; $V_O$ = 2.5V | | –50 | –70 | –180 | –50 | –180 | mA |
| $I_{CCH}$ | Quiescent supply current | $V_{CC}$ = 5.5V; Outputs High, $V_I$ = GND or $V_{CC}$ | | | 0.5 | 1 | | 1 | mA |
| $I_{CCL}$ | | $V_{CC}$ = 5.5V; Outputs Low, $V_I$ = GND or $V_{CC}$ | | | 10 | 19 | | 19 | mA |
| $I_{CCZ}$ | | $V_{CC}$ = 5.5V; Outputs 3-State; $V_I$ = GND or $V_{CC}$ | | | 0.5 | 1 | | 1 | mA |
| $\Delta I_{CC}$ | Additional supply current per input pin[2] | $V_{CC}$ = 5.5V; one input at 3.4V, other inputs at $V_{CC}$ or GND | | | 0.2 | 1 | | 1 | mA |

**NOTES:**
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any $V_{CC}$ between 0V and 2.1V with a transition time of up to 10msec. From $V_{CC}$ = 2.1V to $V_{CC}$ = 5V ± 10% a transition time of up to 100µsec is permitted.
5. Unused pins at $V_{CC}$ or GND.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

## AC CHARACTERISTICS

GND = 0V, $t_R$ = $t_F$ = 2.5ns, $C_L$ = 50pF, $R_L$ = 500Ω

| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $T_{amb}$ = +25°C $V_{CC}$ = +5.0V | | | $T_{amb}$ = -40 to +85°C $V_{CC}$ = +5.0V ±0.5V | | |
| | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{PLH}$ $t_{PHL}$ | Propagation delay nDx to nQx | 2 | 1.1 1.5 | 3.1 2.2 | 4.1 3.1 | 1.1 1.5 | 4.9 3.6 | ns |
| $t_{PLH}$ $t_{PHL}$ | Propagation delay nLE to nQx | 1 | 1.5 1.0 | 2.5 2.1 | 3.3 2.8 | 1.5 1.0 | 3.7 3.1 | ns |
| $t_{PZH}$ $t_{PZL}$ | Output enable time to High and Low level | 4 5 | 1.2 1.2 | 2.4 2.2 | 3.2 2.9 | 1.2 1.2 | 4.0 3.6 | ns |
| $t_{PHZ}$ $t_{PLZ}$ | Output disable time from High and Low level | 4 5 | 1.8 1.5 | 3.0 2.5 | 4.0 3.2 | 1.8 1.5 | 4.9 3.7 | ns |

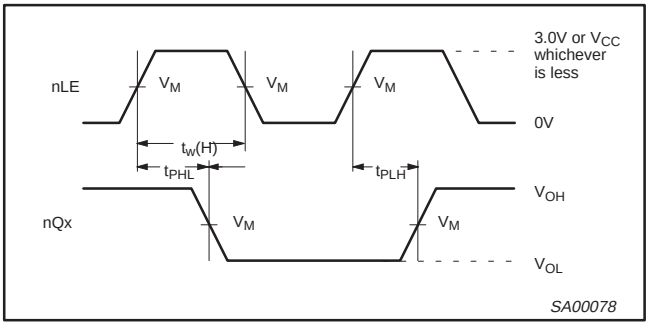
## AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, $C_L$ = 50pF, $R_L$ = 500Ω

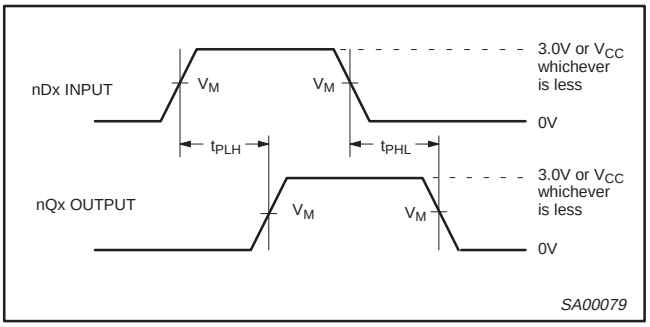
| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | $T_{amb}$ = +25°C, $V_{CC}$ = +5.0V | | $T_{amb}$ = -40 to +85°C, $V_{CC}$ = +5.0V ±0.5V | | |
| | | | Min | Typ | Min | Max | |
| $t_s(H)$<br>$t_s(L)$ | Setup time, High or Low<br>nDx to nLE | 3 | 2.0<br>1.0 | 1.0<br>0.4 | 2.0<br>1.0 | | ns |
| $t_h(H)$<br>$t_h(L)$ | Hold time, High or Low<br>nDx to nLE | 3 | 2.0<br>2.0 | –0.3<br>–0.7 | 2.0<br>2.0 | | ns |
| $t_w(H)$ | nLE pulse width High | 1 | 2.9 | 1.9 | 2.9 | | ns |

## AC WAVEFORMS

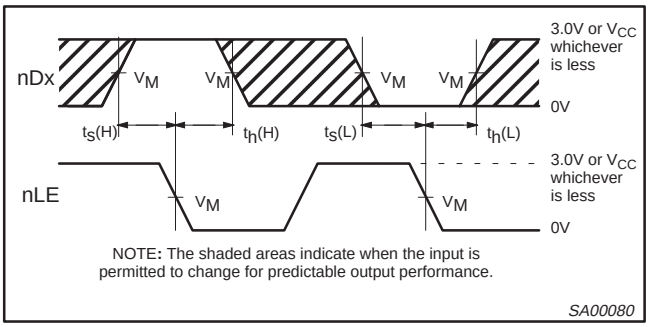
$V_M$ = 1.5V, $V_{IN}$ = GND to 3.0V



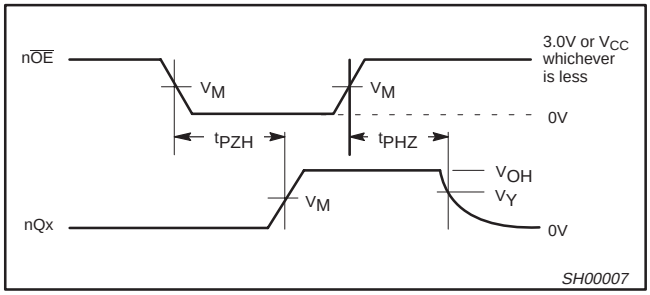

**Waveform 1. Propagation Delay, Latch Enable Input to Output, and Enable Pulse Width**



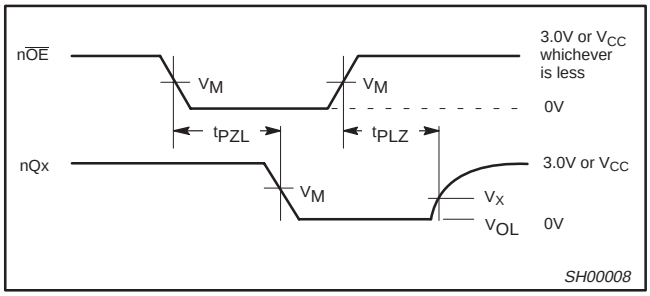

**Waveform 2. Propagation Delay for Data to Outputs**




**Waveform 3. Data Setup and Hold Times**

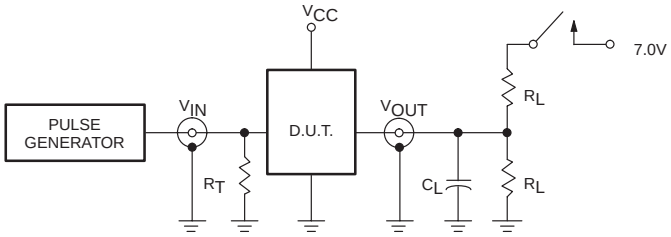



**Waveform 4. 3–State Output Enable Time to High Level and Output Disable Time from High Level**

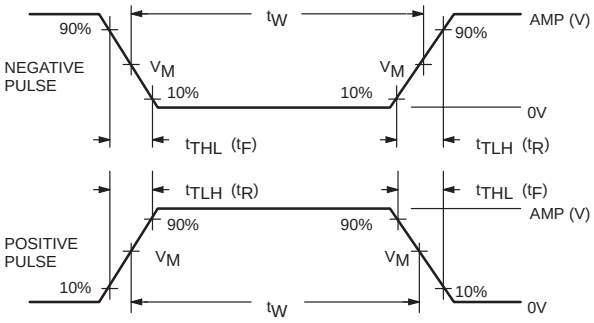



**Waveform 5. 3–State Output Enable Time to Low Level and Output Disable Time from Low Level**

## TEST CIRCUIT AND WAVEFORM




**Test Circuit for 3-State Outputs**




**$V_M$ = 1.5V**
**Input Pulse Definition**

### SWITCH POSITION

| TEST | SWITCH |
|---|---|
| $t_{PLZ}$ | closed |
| $t_{PZL}$ | closed |
| All other | open |

### DEFINITIONS

$R_L$ = Load resistor; see AC CHARACTERISTICS for value.

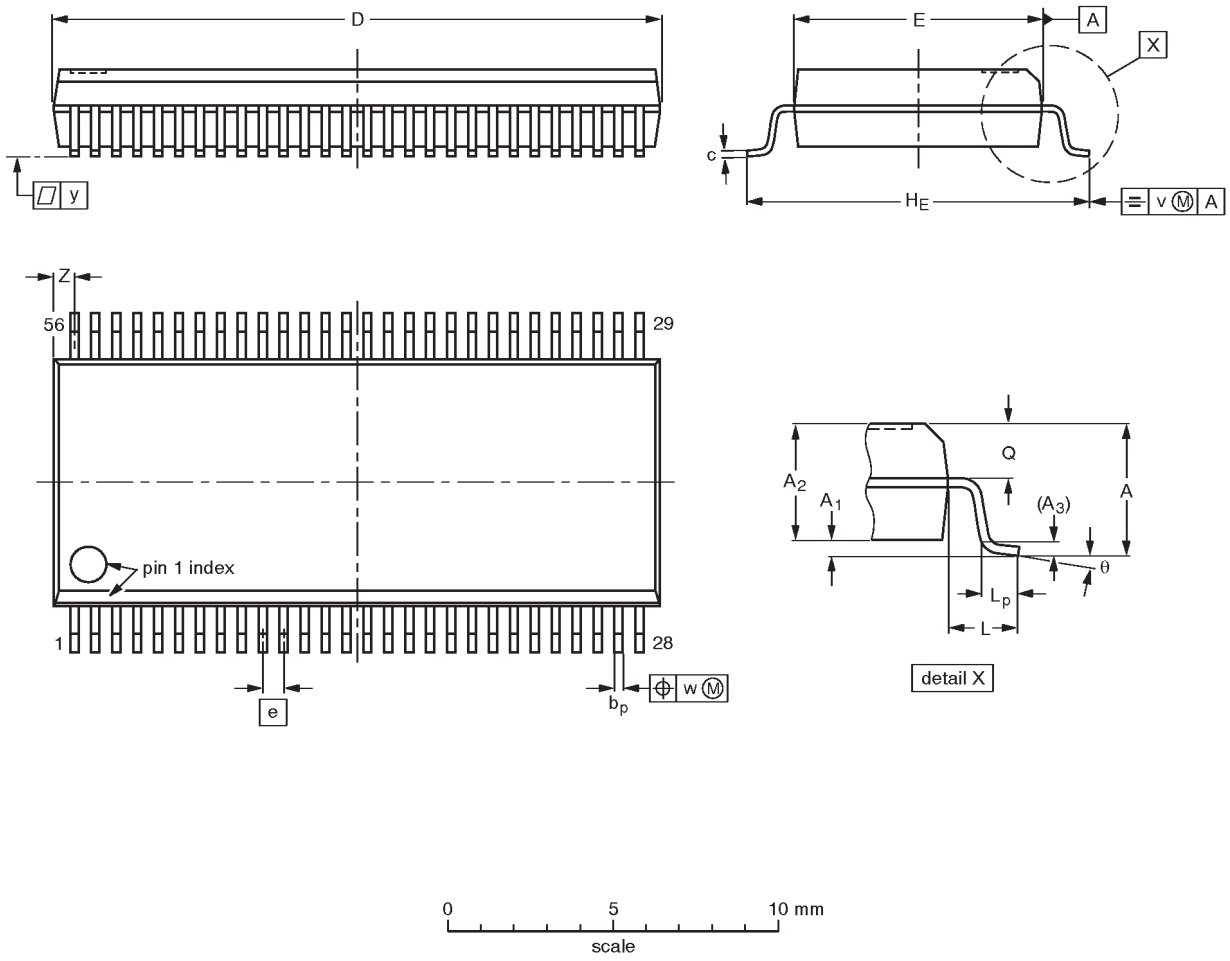
$C_L$ = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

$R_T$ = Termination resistance should be equal to $Z_{OUT}$ of pulse generators.

| FAMILY | INPUT PULSE REQUIREMENTS | | | | |
|---|---|---|---|---|---|
| | Amplitude | Rep. Rate | $t_W$ | $t_R$ | $t_F$ |
| 74ABT/H16 | 3.0V | 1MHz | 500ns | 2.5ns | 2.5ns |

*SA00018*

**SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm** **SOT371-1**




**DIMENSIONS (mm are the original dimensions)**

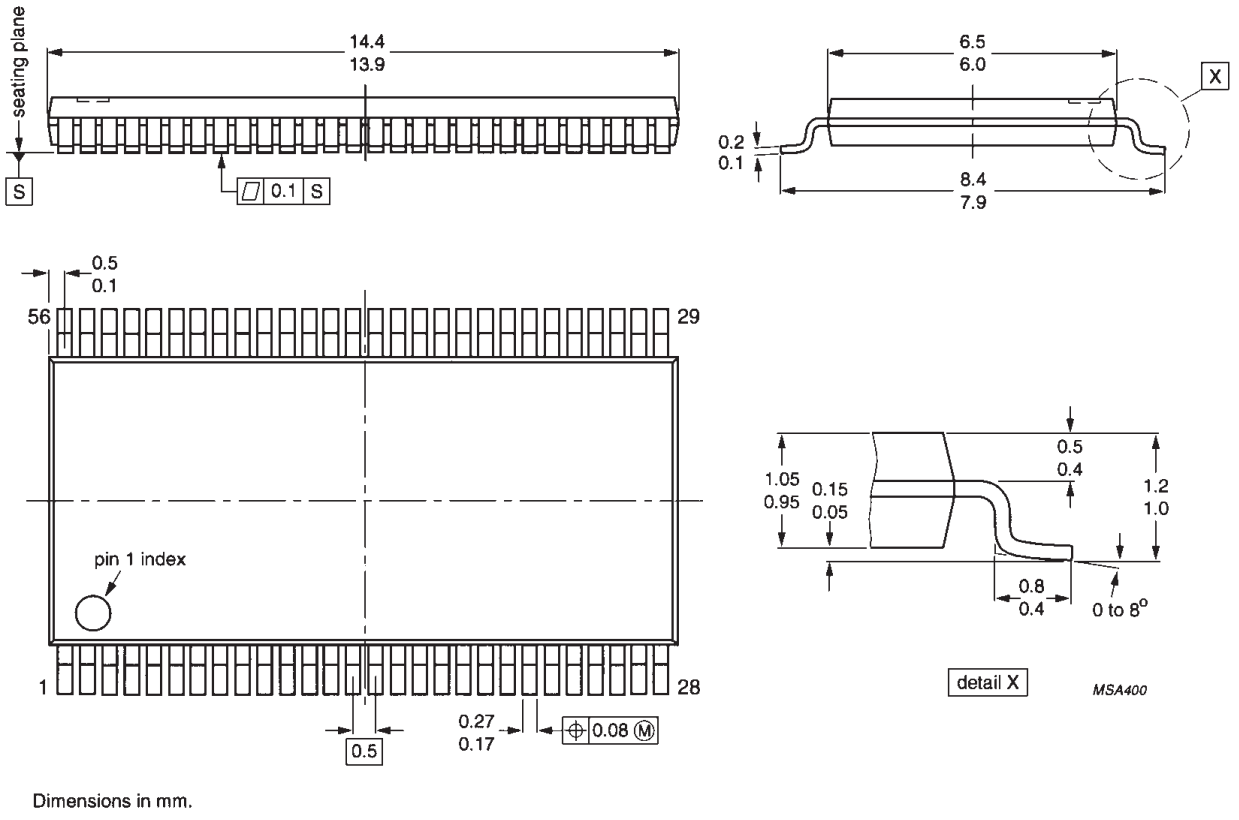
| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.8 | 0.4<br>0.2 | 2.35<br>2.20 | 0.25 | 0.3<br>0.2 | 0.22<br>0.13 | 18.55<br>18.30 | 7.6<br>7.4 | 0.635 | 10.4<br>10.1 | 1.4 | 1.0<br>0.6 | 1.2<br>1.0 | 0.25 | 0.18 | 0.1 | 0.85<br>0.40 | 8°<br>0° |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT371-1 | | MO-118AB | | | | ~~93-11-02~~<br>95-02-04 |

**TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm** **SOT364-1**




Dimensions in mm.

## Data sheet status

| Data sheet status | Product status | Definition [1] |
|---|---|---|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

## Definitions

**Short-form specification —** The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition —** Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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