

DATA SHEET

74ABT162244

74ABTH162244

16-bit buffer/line driver with 30Ω series
termination resistors (3-State)

Product specification
Supersedes data of 1996 Oct 23
IC23 Data Handbook

1998 Feb 25

16-bit buffer/line driver with 30Ω series termination resistors (3-State)

74ABT162244
74ABTH162244

FEATURES

- 16-bit bus interface
- Multiple V_{CC} and GND pins minimize switching noise
- Power-up 3-State
- 3-State buffers
- Output capability: +12 mA/−32mA
- Live insertion/extraction permitted
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Same part as 74ABT16244-1
- 74ABTH162244 incorporates bus hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

DESCRIPTION

The 74ABT162244 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed.

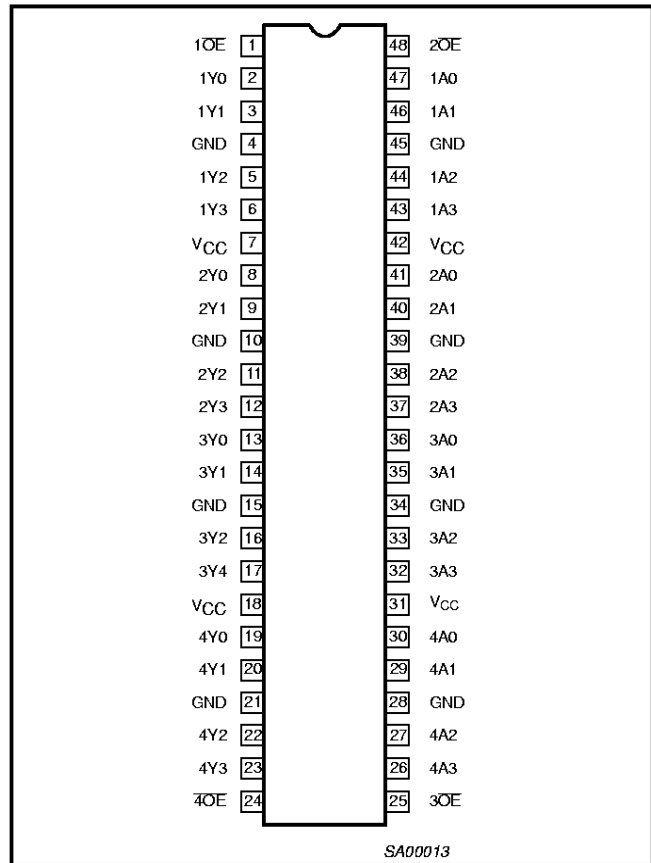
The 74ABT162244 device is a 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables (1OE, 2OE, 3OE, 4OE), each controlling four of the 3-State outputs.

The 74ABT162244 is designed with 30Ω series resistance in both the upper and lower output structures. This design reduces line noise in applications such as memory address drivers, clock drivers and bus receivers/transmitters.

The 74ABT162244 is the same as the 74ABT16244-1. The part number has been changed to reflect industry standards.

Two options are available, 74ABT162244 which does not have the bus hold feature and the 74ABTH162244 which incorporates the bus hold feature.

PIN CONFIGURATION



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T _{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t _{PLH} t _{PHL}	Propagation delay nAx to nYx	C _L = 50pF; V _{CC} = 5V	1.8 3.2	ns
C _{IN}	Input capacitance	V _I = 0V or V _{CC}	3	pF
C _{OUT}	Output capacitance	V _O = 0V or V _{CC} ; 3-State	7	pF
I _{CCZ}	Quiescent supply current	Outputs disabled; V _{CC} = 5.5V	500	μA
I _{CCL}		Outputs Low; V _{CC} = 5.5V	10	mA

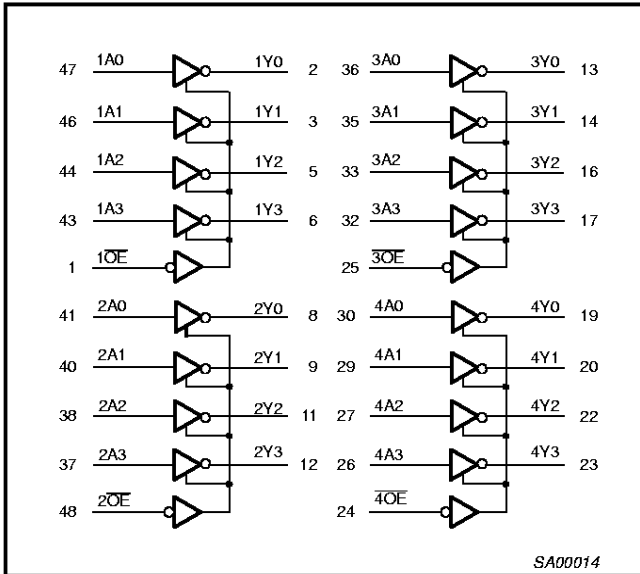
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	−40°C to +85°C	74ABT162244 DL	BT162244 DL	SOT370-1
48-Pin Plastic TSSOP Type II	−40°C to +85°C	74ABT162244 DGG	BT162244 DGG	SOT362-1
48-Pin Plastic SSOP Type III	−40°C to +85°C	74ABTH162244 DL	BH162244 DL	SOT370-1
48-Pin Plastic TSSOP Type II	−40°C to +85°C	74ABTH162244 DGG	BH162244 DGG	SOT362-1

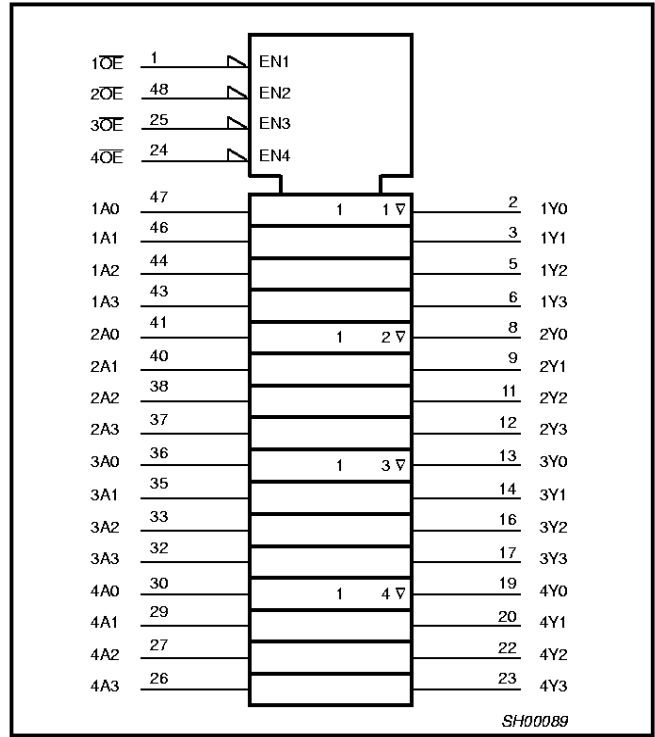
16-bit buffer/line driver with 30Ω series termination resistors (3-State)

74ABT162244
74ABTH162244

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

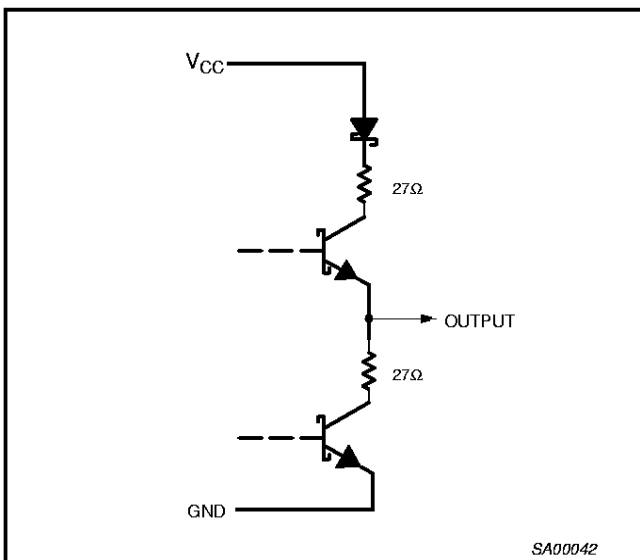


FUNCTION TABLE

INPUTS		OUTPUTS
nOE	nAx	nYx
L	L	L
L	H	H
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

SCHEMATIC OF Y OUTPUTS



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43 41, 40, 38, 37 36, 35, 33, 32 30, 29, 27, 26	1A0 – 1A3, 2A0 – 2A3, 3A0 – 3A3, 4A0 – 4A3	Data inputs
2, 3, 5, 6 8, 9, 11, 12 13, 14, 16, 17 19, 20, 22, 23	1Y0 – 1Y3, 2Y0 – 2Y3, 3Y0 – 3Y3, 4Y0 – 4Y3	Data outputs
1, 48 25, 24	1OE, 2OE, 3OE, 4OE	Output enables
4, 10, 15, 21 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	VCC	Positive supply voltage

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ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0	-18	mA
V _I	DC input voltage ³		-1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	-50	mA
V _{OUT}	DC output voltage ³	output in Off or High state	-0.5 to +5.5	V
I _{OUT}	DC output current	output in Low state	128	mA
		output in High state	-64	
T _{stg}	Storage temperature range		-65 to 150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V _{CC}	DC supply voltage	4.5	5.5	V
V _I	Input voltage	0	V _{CC}	V
V _{IH}	High-level input voltage	2.0		V
V _{IL}	Low-level input voltage		0.8	V
I _{OH}	High-level output current		-32	mA
I _{OL}	Low-level output current		12	mA
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _{amb}	Operating free-air temperature range	-40	+85	°C

16-bit buffer/line driver with 30Ω series termination resistors (3-State)

74ABT162244 74ABTH162244

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT	
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C			
			Min	Typ	Max	Min	Max		
V _{IK}	Input clamp voltage	V _{CC} = 4.5V; I _{IK} = -18mA		-0.9	-1.2		-1.2	V	
V _{OH}	High-level output voltage ³	V _{CC} = 4.5V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}	2.5	2.9		2.5		V	
		V _{CC} = 5V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}	3.0	3.4		3.0		V	
		V _{CC} = 4.5V; I _{OH} = -32mA; V _I = V _{IL} or V _{IH}	2.0	2.4		2.0		V	
V _{OL}	Low-level output voltage	V _{CC} = 4.5V; I _{OL} = 8mA; V _I = V _{IL} or V _{IH}			0.65		0.65	V	
		V _{CC} = 4.5V; I _{OL} = 12mA; V _I = V _{IL} or V _{IH}			0.80		0.80	V	
I _I	Input leakage current	V _{CC} = 5.5V; V _I = GND or 5.5V		±0.01	±1.0		±1.0	μA	
I _I	Input leakage current 74ABTH162244	V _{CC} = 5.5V; V _I = V _{CC} or GND	Control pins		±0.01	±1.0		±1.0	μA
		V _{CC} = 5.5V; V _I = V _{CC}			0.01	1.0		1.0	μA
		V _{CC} = 5.5V; V _I = 0	Data pins		-2.0	-3.0		-5.0	μA
I _{HOLD}	Bus Hold Current A Inputs ⁴ 74ABTH162244	V _{CC} = 4.5V; V _I = 0.8V		50			50	μA	
		V _{CC} = 5.5V; V _I = 2.0V		-75			-75		
		V _{CC} = 5.5V; V _I = 0 to 5.5V		±500					
I _{OFF}	Power-off leakage current	V _{CC} = 0.0V; V _O or V _I ≤ 4.5V		±5.0	±100		±100	μA	
I _{PU/PD}	Power-up/down 3-State output current	V _{CC} = 2.0V; V _O = 0.5V; V _I = GND or V _{CC} ; V _{OE} = Don't care		±5.0	±50		±50	μA	
I _{OZH}	3-State output High current	V _{CC} = 5.5V; V _O = 5.5V; V _I = V _{IL} or V _{IH}		0.1	10		10	μA	
I _{OZL}	3-State output Low current	V _{CC} = 5.5V; V _O = 0.0V; V _I = V _{IL} or V _{IH}		-0.1	-10		-10	μA	
I _{CEX}	Output High leakage current	V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC}		5.0	50		50	μA	
I _O	Output current ¹	V _{CC} = 5.5V; V _O = 2.5V	-50	-100	-180	-50	-180	mA	
I _{CCH}	Quiescent supply current ³	V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC}		0.50	1.0		1.0	mA	
I _{CCL}		V _{CC} = 5.5V; Outputs Low, V _I = GND or V _{CC}		10	19		19	mA	
I _{CCZ}		V _{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC}		0.50	1.0		1.0	mA	
ΔI _{CC}	Additional supply current per input pin ^{2,3}	Outputs enabled, one data input at 3.4V, other inputs at V _{CC} or GND; V _{CC} = 5.5V		100	250		250	μA	
		Outputs disabled, one data input at 3.4V, other inputs at V _{CC} or GND; V _{CC} = 5.5V		100	250		250	μA	
		Control pins, outputs disabled, one enable input at 3.4V, other inputs at V _{CC} or GND; V _{CC} = 5.5V		100	250		250	μA	

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- This data sheet limit may vary among suppliers.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

16-bit buffer/line driver with 30Ω series termination resistors (3-State)

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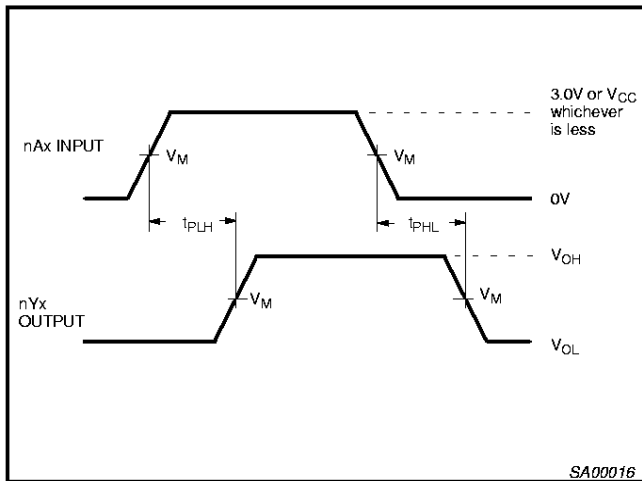
AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$, $R_L = 500\Omega$

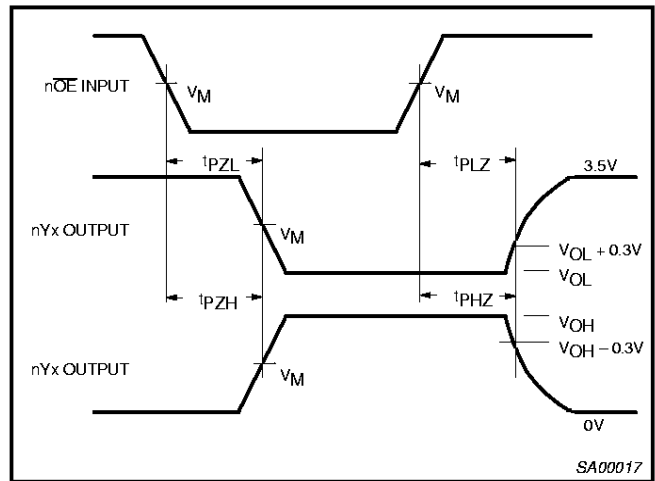
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$			$T_{\text{amb}} = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	1.0 1.6	1.8 3.2	2.4 4.0	1.0 1.6	2.7 4.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.2 2.6	2.7 5.0	3.5 6.2	1.2 2.6	4.3 7.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.3	3.0 2.6	3.8 3.3	1.5 1.3	4.5 4.6	ns

AC WAVEFORMS

$V_M = 1.5\text{V}$, $V_{\text{IN}} = \text{GND to } 3.0\text{V}$



Waveform 1. Input (An) to Output (Yn) Propagation Delays

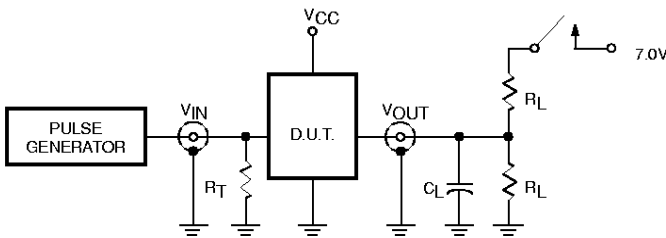


Waveform 2. 3-State Output Enable and Disable Times

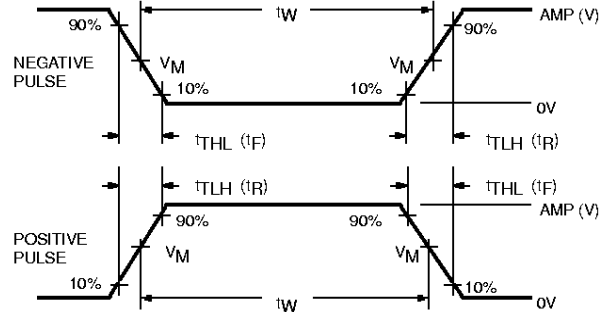
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TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



$V_M = 1.5V$
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{pZL}	closed
All other	open

DEFINITIONS

- R_L = Load resistor; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

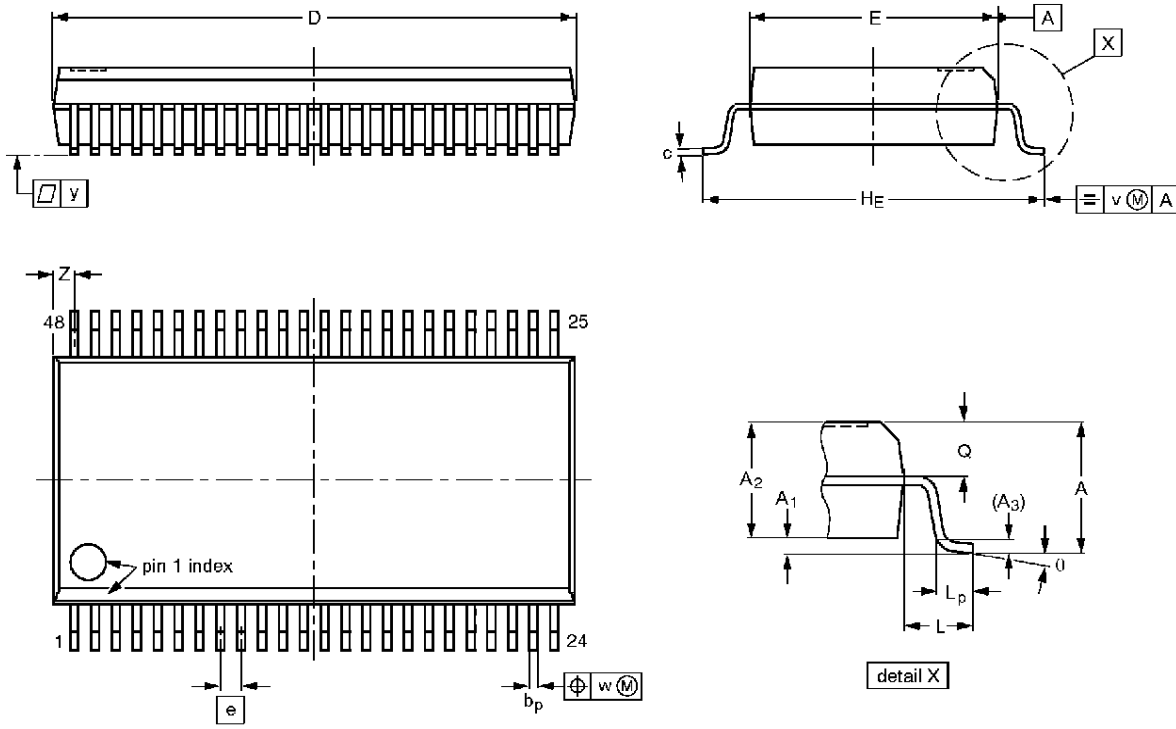
SA00018

16-bit buffer/line driver with 30Ω series termination resistors (3-State)

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SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

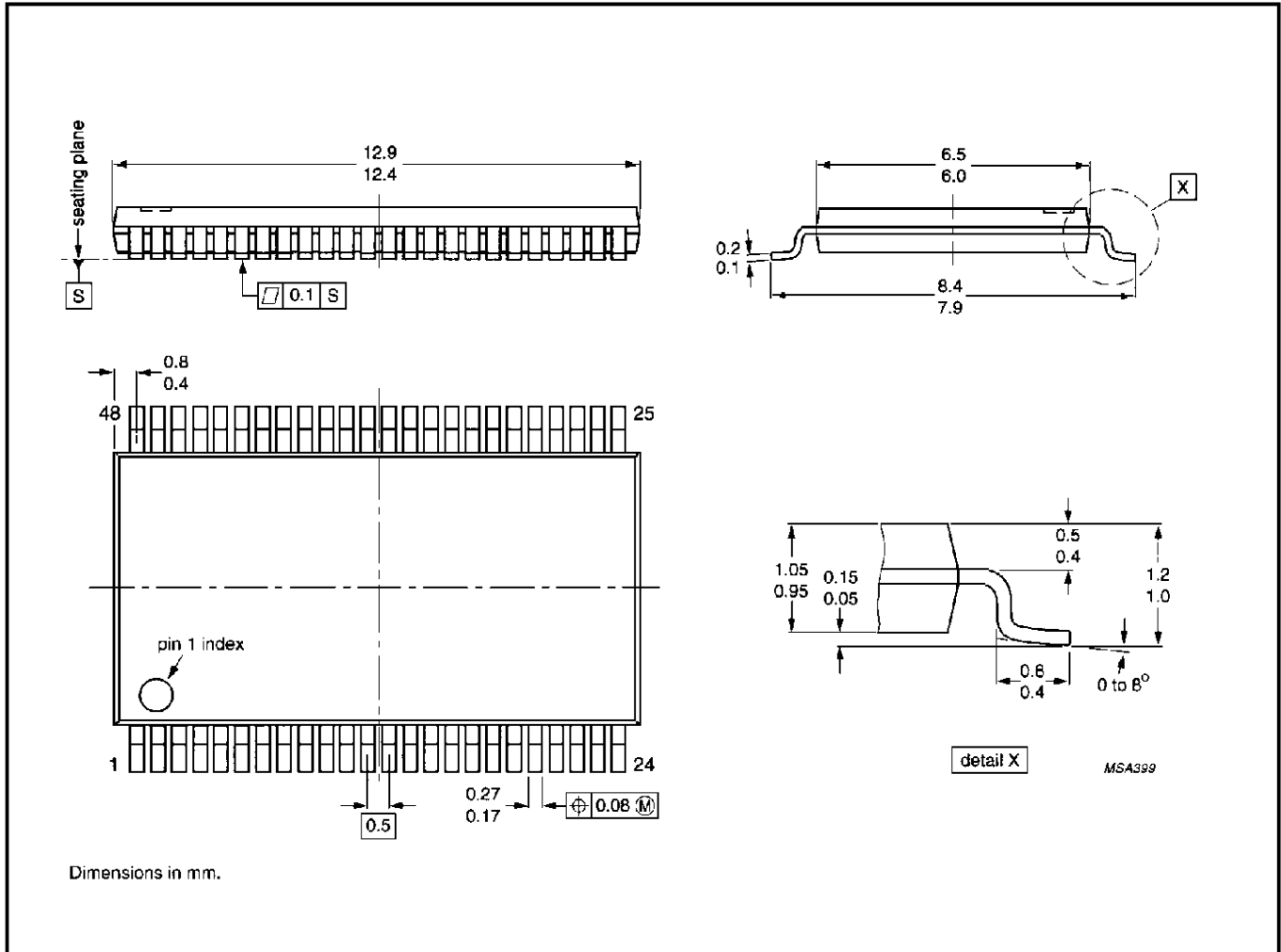
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118AA				93-11-02 95-02-04

16-bit buffer/line driver with 30Ω series termination resistors (3-State)

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TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm

SOT362-1



16-bit buffer/line driver with 30Ω series
termination resistors (3-State)

74ABT162244
74ABTH162244

NOTES