DATA SHEET

74ABT16241A
74ABTH16241A
16-bit buffer/driver (3-State)

Product specification
Supersedes data of 1997 Jun 12
IC23 Data Handbook

1998 Feb 25

Philips
Semiconductors

PHILIPS

FEATURES

- 16-bit bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- 74ABTH16241A incorporates bus hold data inputs which eliminate the need for external pull up resistors to hold unused inputs
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT16241A is a high-performance BiCMOS device which combines low static and dynamic power dissipation with high speed and high output drive.

This device is a 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables (1$\overline{OE}$, 2OE, 3OE, 4$\overline{OE}$), each controlling four of the 3-State outputs.

Two options are available, 74ABT16241A which does not have the bus hold feature and 74ABTH16241A which incorporates the bus hold feature.

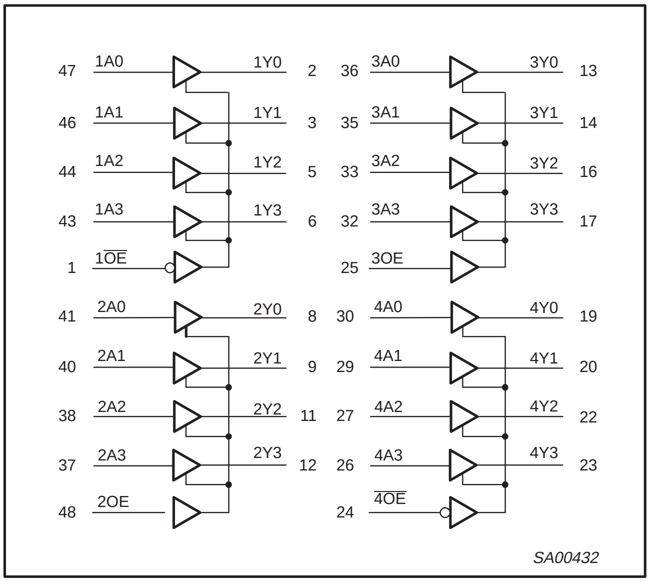
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	C_L = 50pF; V_{CC} =	1.8 1.6	ns
C_{IN}	Input capacitance n$\overline{OE}$	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or	6	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} =	500	µA
I_{CCL}		Outputs low; V_{CC} = 5.5V	8	mA

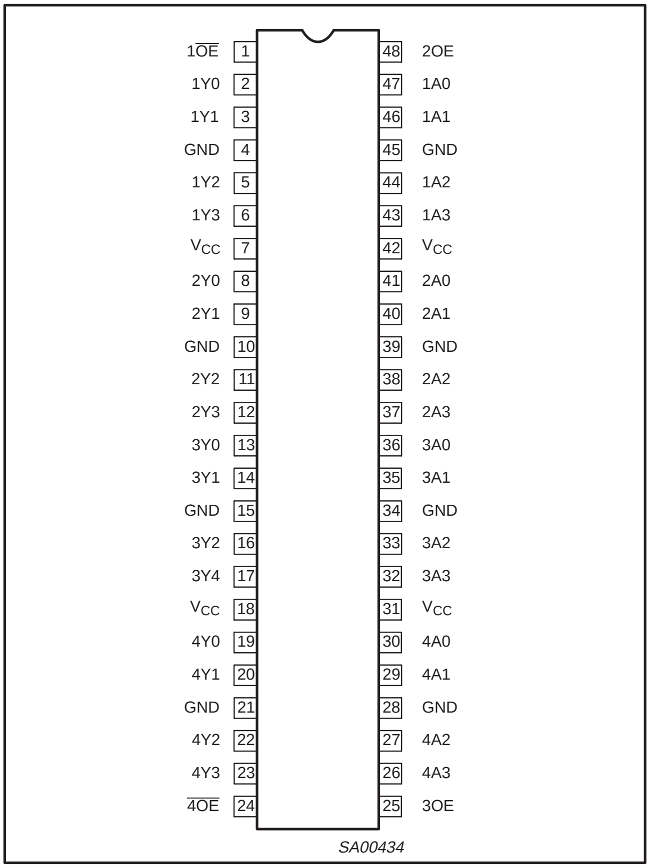
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT16241A DL	BT16241A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT16241A DGG	BT16241A DGG	SOT362-1
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH16241A DL	BH16241A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH16241A DGG	BH16241A DGG	SOT362-1

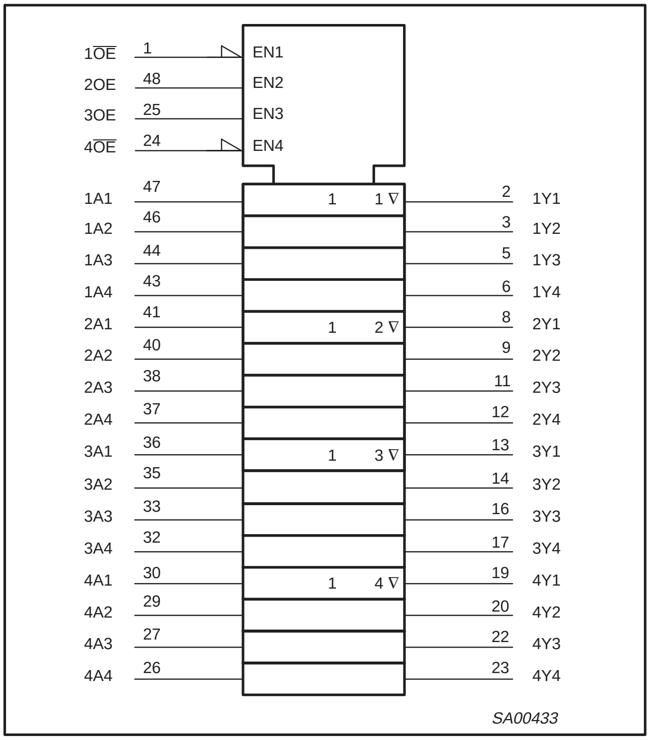
LOGIC SYMBOL



PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

Inputs		Outputs
1$\overline{OE}$, 4$\overline{OE}$	1An, 4An	1Yn, 4Yn
L	L	L
L	H	H
H	X	Z
2OE, 3OE	2An, 3An	2Yn, 3Yn
H	L	L
H	H	H
L	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A0-1A3 2A0-2A3 3A0-3A3 4A0-4A3	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1Y0-1Y3 2Y0-2Y3 3Y0-3Y3 4Y0-4Y3	Data outputs
1, 48, 25, 24	1$\overline{OE}$, 2$\overline{OE}$, 3OE, 4$\overline{OE}$	Output enables
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA			–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}		2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}		3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}		2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}			0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V			±0.01	±1.0		±1.0	μA
I_I	Input leakage current 74ABTH16241A	V_{CC} = 5.5V; V_I = V_{CC} or GND	Control pins		±0.01	±1		±1	μA
		V_{CC} = 5.5V; V_I = V_{CC}	Data pins		0.01	1		1	μA
		V_{CC} = 5.5V; V_I = 0			–2	–3		–5	μA
I_{HOLD}	Bus Hold current A inputs[3] 74ABTH16241A	V_{CC} = 4.5V; V_I = 0.8V		75			75		μA
		V_{CC} = 4.5V; V_I = 2.0V		–75			–75		
		V_{CC} = 5.5V; V_I = 0 to 5.5V		±500					
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or V_I ≤ 4.5V			±5.0	±100		±100	μA
I_{PU}/I_{PD}	Power-up/down 3-State output current	V_{CC} = 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; $V_{\overline{OE}}$ = V_{CC}			±5.0	±50		±50	μA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}			1.0	10		10	μA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			–1.0	–10		–10	μA
I_{CEX}	Output high leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}			1.0	50		50	μA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V		–50	–70	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}			0.5	1.0		1.0	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}			8	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}			0.5	1.0		1.0	mA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V			10	200		200	μA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This is the bus hold overdrive current required to force the input to the opposite logic state.

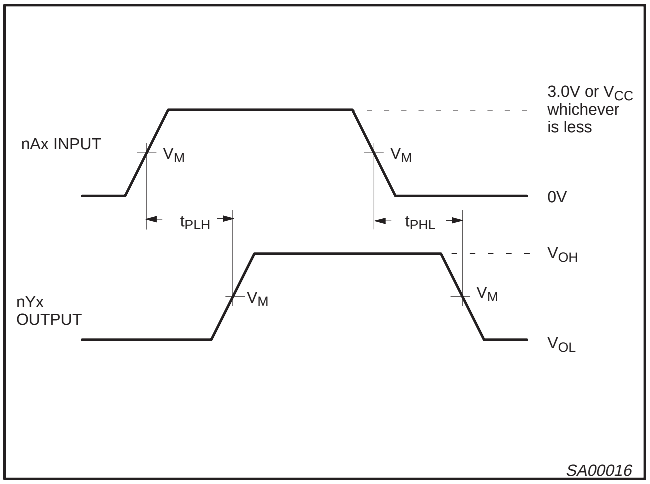
AC CHARACTERISTICS

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = -40°C to +85°C.

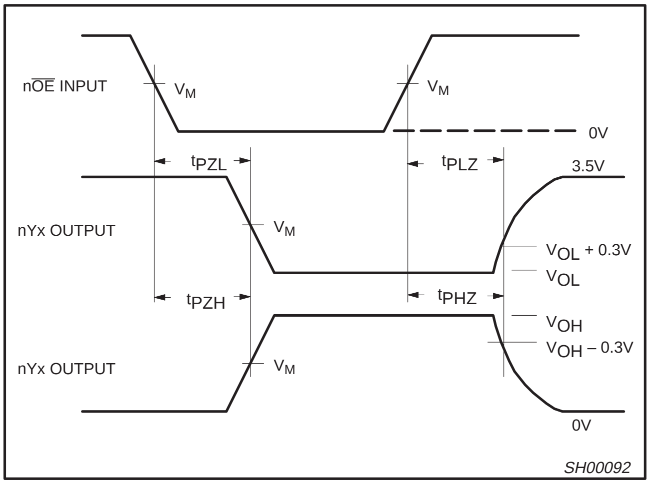
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = –40°C to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	1	1.0 1.0	1.8 1.6	2.6 2.4	1.0 1.0	3.1 2.9	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.0 1.0	2.4 2.6	3.4 4.6	1.0 1.0	3.9 5.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.3 1.3	3.0 2.4	4.3 3.6	1.0 1.0	5.3 4.2	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

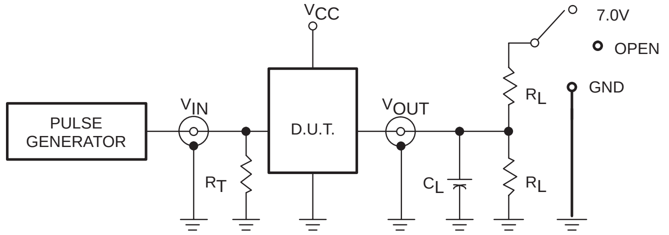


Waveform 1. Input (nAx) to Output (nYx) Propagation Delays

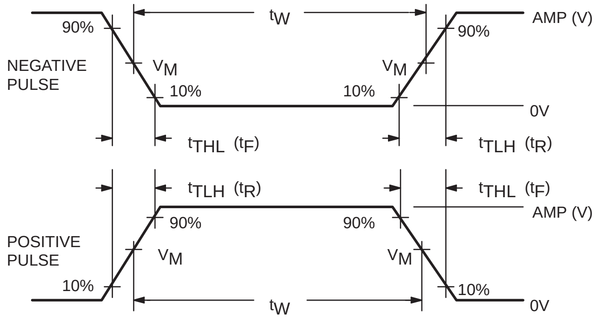


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	7V
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

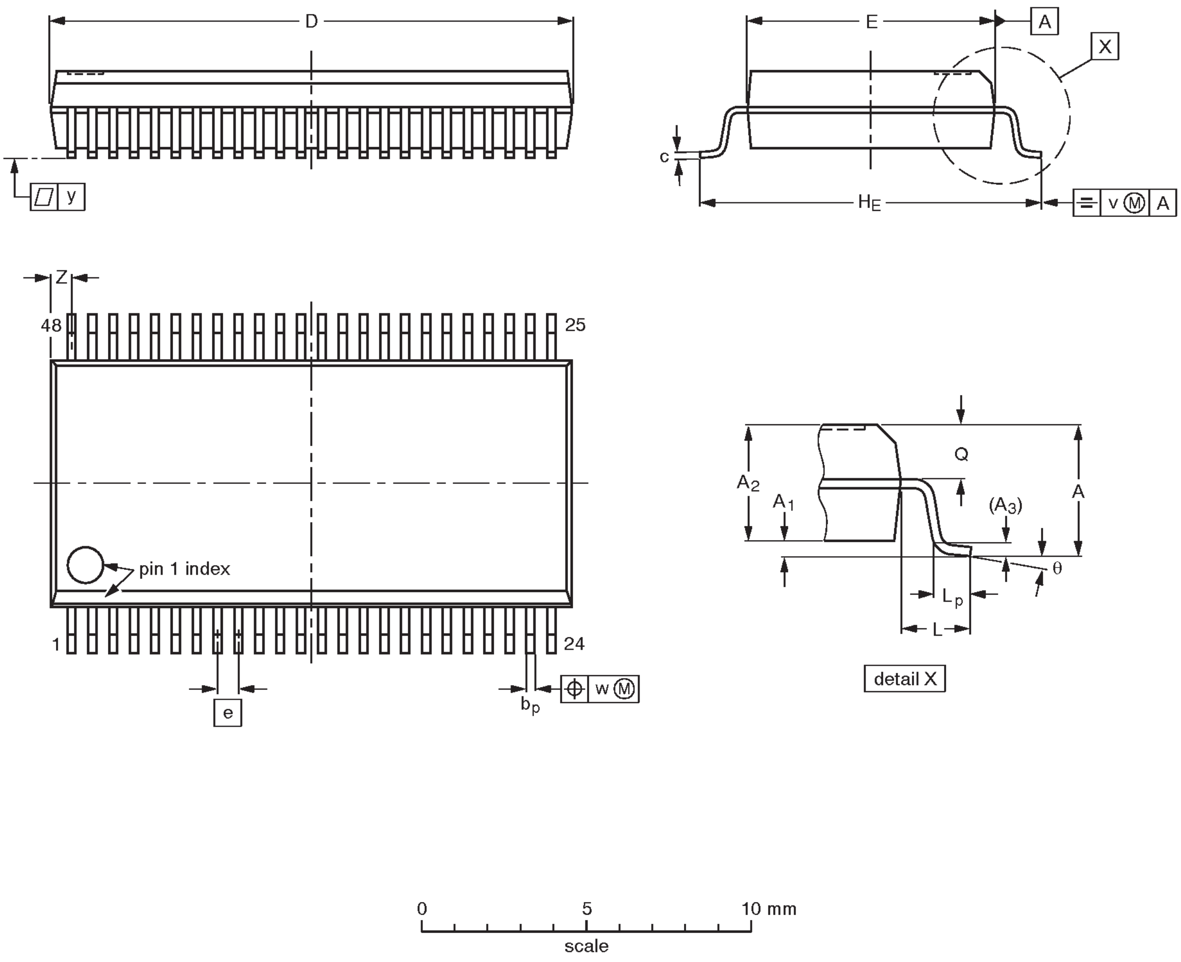
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT16	3.0V	1MHz	500ns	2.5ns	2.5ns

SH00093

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm SOT370-1



DIMENSIONS (mm are the original dimensions)

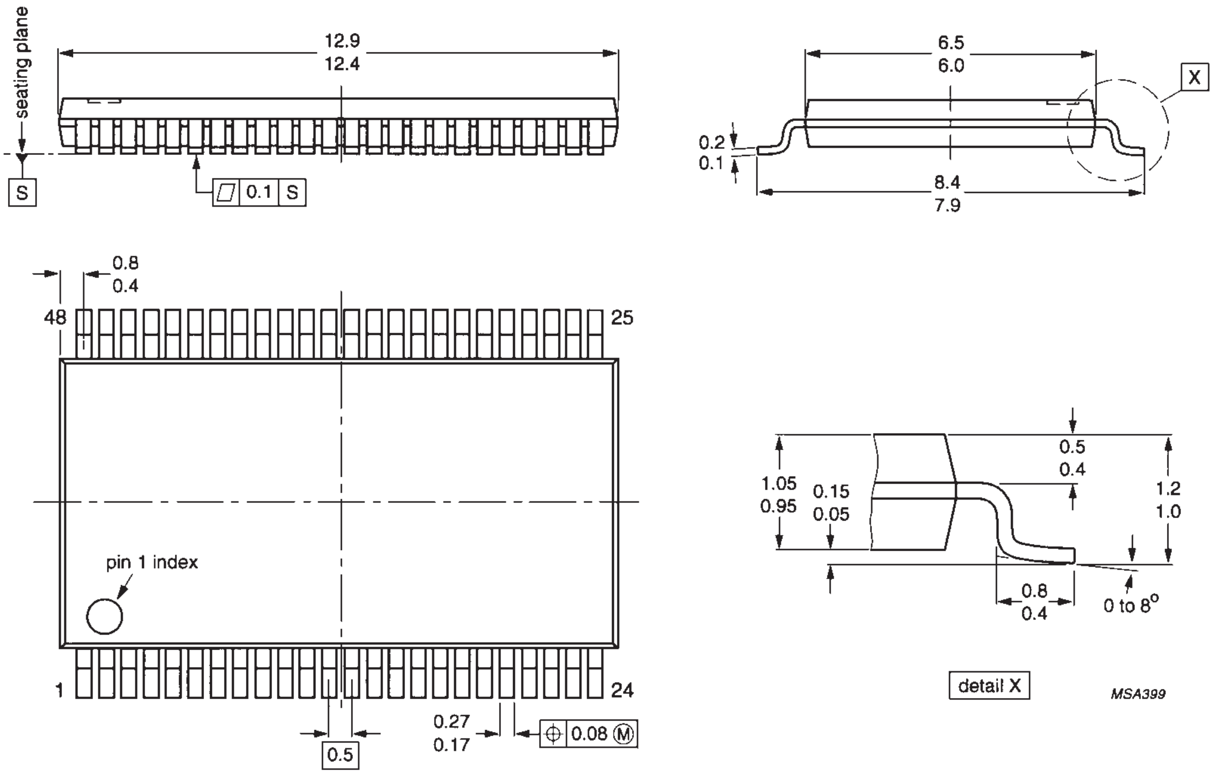
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118AA				~~93-11-02~~ 95-02-04

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm SOT362-1



Dimensions in mm.

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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