

# 74AC04, 74ACT04 Hex Inverter

## Features

- I<sub>CC</sub> reduced by 50% on 74AC only
- Outputs source/sink 24mA
- ACT04 has TTL-compatible inputs

## General Description

The AC/ACT04 contains six inverters.

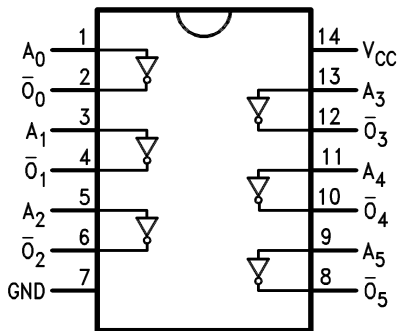
## Ordering Information

Order Number	Package Number	Package Description
74AC04SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74AC04SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC04MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC04PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT04SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74ACT04MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT04PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

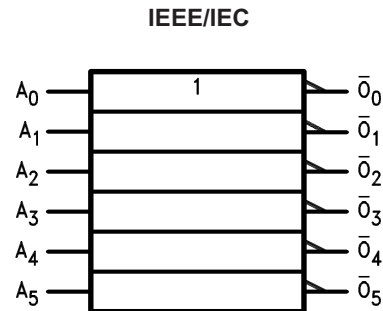
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code. (PC not available in Tape and Reel.)

All packages are lead free per JEDEC: J-STD-020B standard.

## Connection Diagram



## Logic Symbol



## Pin Description

Pin Names	Description
A <sub>n</sub>	Inputs
$\bar{O}_n$	Outputs

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## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	-0.5V to +7.0V
$I_{IK}$	DC Input Diode Current $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$	-20mA +20mA
$V_I$	DC Input Voltage	-0.5V to $V_{CC} + 0.5V$
$I_{OK}$	DC Output Diode Current $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$	-20mA +20mA
$V_O$	DC Output Voltage	-0.5V to $V_{CC} + 0.5V$
$I_O$	DC Output Source or Sink Current	$\pm 50mA$
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current per Output Pin	$\pm 50mA$
$T_{STG}$	Storage Temperature	-65°C to +150°C
$T_J$	Junction Temperature PDIP	140°C

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage AC ACT	2.0V to 6.0V 4.5V to 5.5V
$V_I$	Input Voltage	0V to $V_{CC}$
$V_O$	Output Voltage	0V to $V_{CC}$
$T_A$	Operating Temperature	-40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate, AC Devices: $V_{IN}$ from 30% to 70% of $V_{CC}$ , $V_{CC}$ @ 3.3V, 4.5V, 5.5V	125mV/ns
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACT Devices: $V_{IN}$ from 0.8V to 2.0V, $V_{CC}$ @ 4.5V, 5.5V	125mV/ns

## DC Electrical Characteristics for AC

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C		Units
				Typ.	Guaranteed Limits			
V <sub>IH</sub>	Minimum HIGH Level Input Voltage	3.0	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	2.1	2.1	V	
		4.5		2.25	3.15	3.15		
		5.5		2.75	3.85	3.85		
V <sub>IL</sub>	Maximum LOW Level Input Voltage	3.0	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	0.9	0.9	V	
		4.5		2.25	1.35	1.35		
		5.5		2.75	1.65	1.65		
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	3.0	I <sub>OUT</sub> = -50μA	2.99	2.9	2.9	V	
		4.5		4.49	4.4	4.4		
		5.5		5.49	5.4	5.4		
		3.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> ; I <sub>OH</sub> = -12mA		2.56	2.46		
		4.5	I <sub>OH</sub> = -24mA		3.86	3.76		
		5.5	I <sub>OH</sub> = -24mA <sup>(1)</sup>		4.86	4.76		
V <sub>OL</sub>	Maximum LOW Level Output Voltage	3.0	I <sub>OUT</sub> = 50μA	0.002	0.1	0.1	V	
		4.5		0.001	0.1	0.1		
		5.5		0.001	0.1	0.1		
		3.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> ; I <sub>OL</sub> = 12mA		0.36	0.44		
		4.5	I <sub>OL</sub> = 24mA		0.36	0.44		
		5.5	I <sub>OL</sub> = 24mA <sup>(1)</sup>		0.36	0.44		
I <sub>IN</sub> <sup>(3)</sup>	Maximum Input Leakage Current	5.5	V <sub>I</sub> = V <sub>CC</sub> , GND		±0.1	±1.0	μA	
I <sub>OLD</sub>	Minimum Dynamic Output Current <sup>(2)</sup>	5.5	V <sub>OLD</sub> = 1.65V Max.			75	mA	
I <sub>OHD</sub>		5.5	V <sub>OHD</sub> = 3.85V Min.			-75	mA	
I <sub>CC</sub> <sup>(3)</sup>	Maximum Quiescent Supply Current	5.5	V <sub>IN</sub> = V <sub>CC</sub> or GND		2.0	20.0	μA	

**Notes:**

1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0ms, one output loaded at a time.
3. I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

## DC Electrical Characteristics for ACT

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C		Units
				Typ.	Guaranteed Limits			
V <sub>IH</sub>	Minimum HIGH Level Input Voltage	4.5	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	2.0	2.0		V
		5.5		1.5	2.0	2.0		
V <sub>IL</sub>	Maximum LOW Level Input Voltage	4.5	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	0.8	0.8		V
		5.5		1.5	0.8	0.8		
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	4.5	I <sub>OUT</sub> = -50μA	4.49	4.4	4.4		V
		5.5		5.49	5.4	5.4		
		4.5	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> : I <sub>OH</sub> = -24mA		3.86	3.76		
		5.5		I <sub>OH</sub> = -24mA <sup>(4)</sup>		4.86	4.76	
V <sub>OL</sub>	Maximum LOW Level Output Voltage	4.5	I <sub>OUT</sub> = 50μA	0.001	0.1	0.1		V
		5.5		0.001	0.1	0.1		
		4.5	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> : I <sub>OL</sub> = 24mA		0.36	0.44		
		5.5		I <sub>OL</sub> = 24mA <sup>(4)</sup>		0.36	0.44	
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	V <sub>I</sub> = V <sub>CC</sub> , GND		±0.1	±1.0		μA
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	V <sub>I</sub> = V <sub>CC</sub> - 2.1V	0.6		1.5		mA
I <sub>OLD</sub>	Minimum Dynamic Output Current <sup>(5)</sup>	5.5	V <sub>OLD</sub> = 1.65V Max.			75		mA
I <sub>OHD</sub>		5.5	V <sub>OHD</sub> = 3.85V Min.			-75		mA
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	V <sub>IN</sub> = V <sub>CC</sub> or GND		4.0	40.0		μA

**Notes:**

4. All outputs loaded; thresholds on input associated with output under test.
5. Maximum test duration 2.0ms, one output loaded at a time.

**AC Electrical Characteristics for AC**

Symbol	Parameter	V <sub>CC</sub> (V) <sup>(6)</sup>	T <sub>A</sub> = +25°C, C <sub>L</sub> = 50pF			T <sub>A</sub> = -40°C to +85°C, C <sub>L</sub> = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
t <sub>PLH</sub>	Propagation Delay	3.3	1.5	4.5	9.0	1.0	10.0	ns
		5.0	1.5	4.0	7.0	1.0	7.5	
t <sub>PHL</sub>	Propagation Delay	3.3	1.5	4.5	8.5	1.0	9.5	ns
		5.0	1.5	3.5	6.5	1.0	7.0	

**Note:**

6. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V.

**AC Electrical Characteristics for ACT**

Symbol	Parameter	V <sub>CC</sub> (V) <sup>(7)</sup>	T <sub>A</sub> = +25°C, C <sub>L</sub> = 50pF			T <sub>A</sub> = -40°C to +85°C, C <sub>L</sub> = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
t <sub>PLH</sub>	Propagation Delay	5.0	1.0	6.0	8.5	1.0	9.0	ns
t <sub>PHL</sub>	Propagation Delay	5.0	1.0	5.5	8.0	1.0	8.5	ns

**Note:**

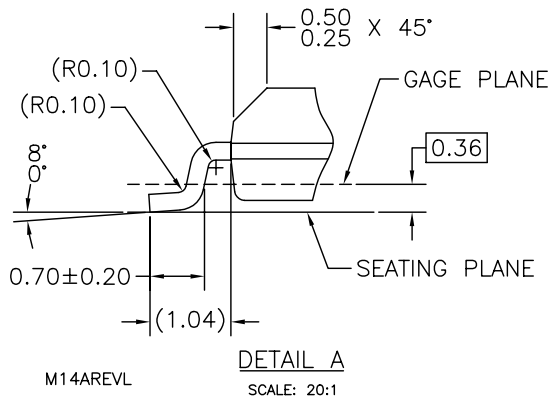
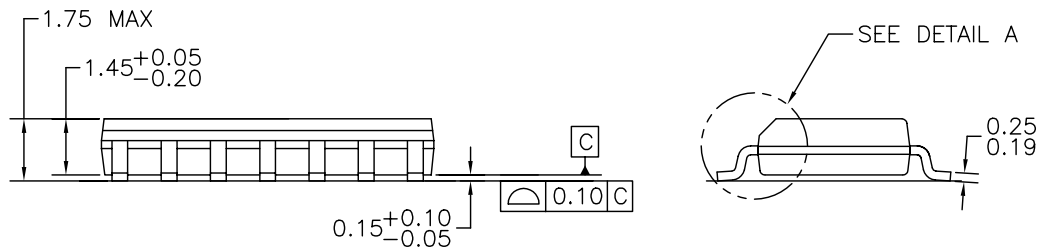
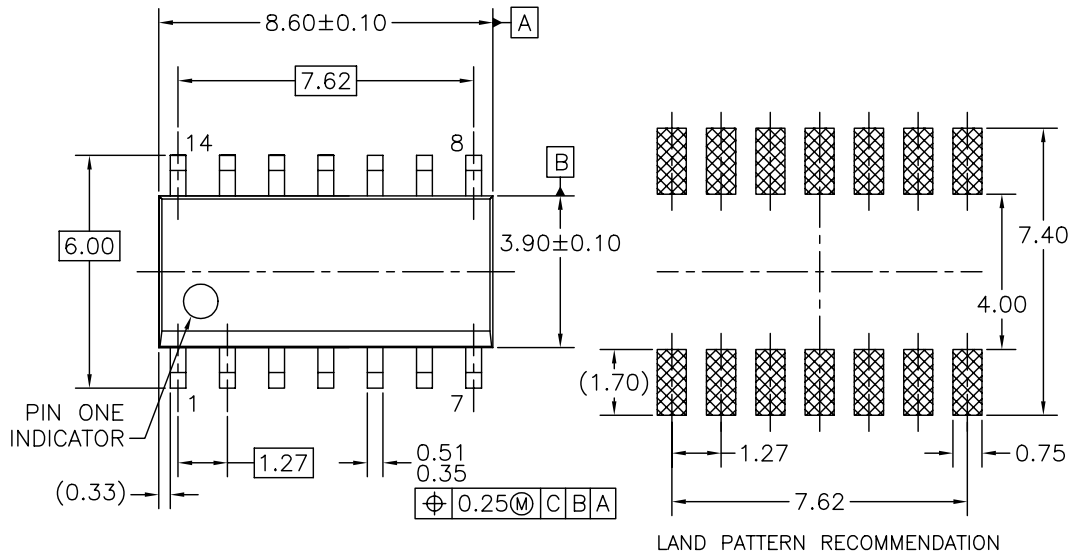
7. Voltage range 5.0 is 5.0V ± 0.5V.

**Capacitance**

Symbol	Parameter	Conditions	Typ.	Units
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = OPEN	4.5	pF
V <sub>CC</sub>	Power Dissipation Capacitance	V <sub>CC</sub> = 5.0V	30.0	pF

### Physical Dimensions

Dimensions are in millimeters unless otherwise noted.



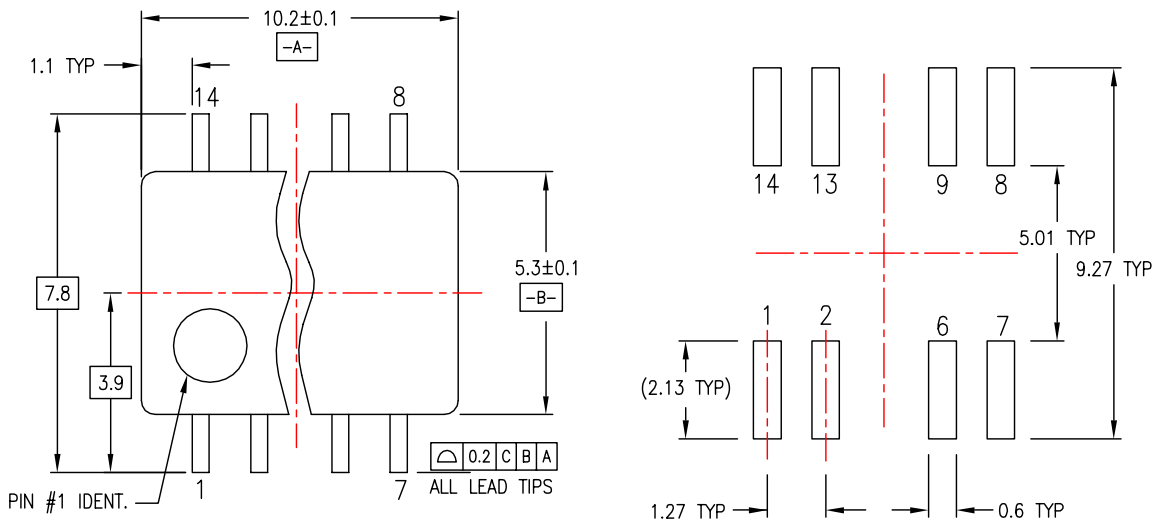
NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C, DATED MAY 1990.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.

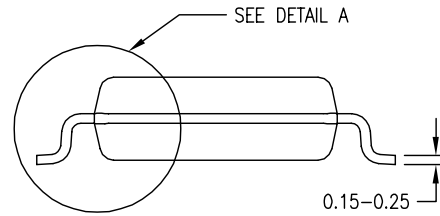
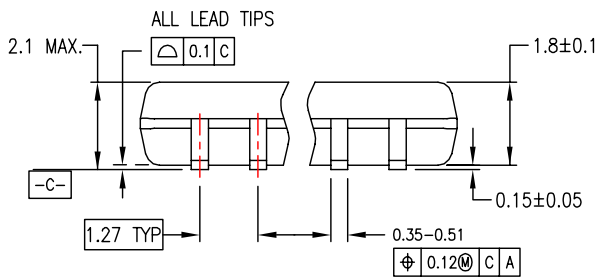
Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M14A

**Physical Dimensions** (Continued)

Dimensions are in millimeters unless otherwise noted.



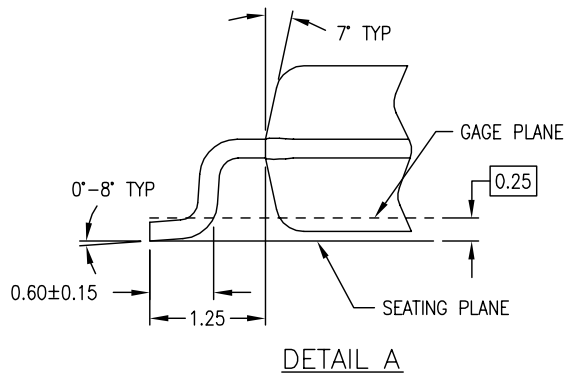
LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.



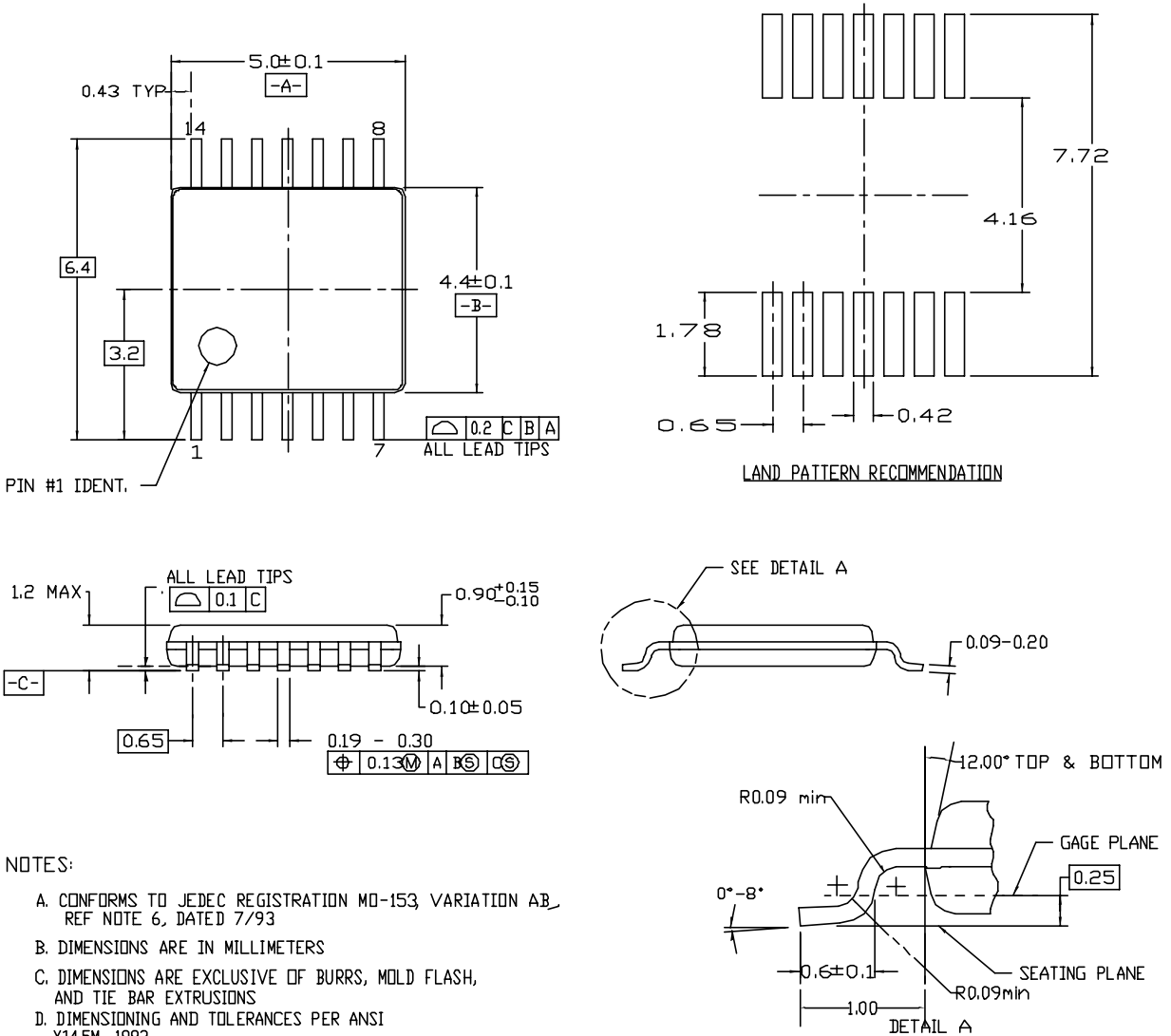
DETAIL A

M14DREVC

**Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M14D**

**Physical Dimensions** (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

MTC14revD

**Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14**



**Physical Dimensions** (Continued)

Dimensions are in inches (millimeters) unless otherwise noted.

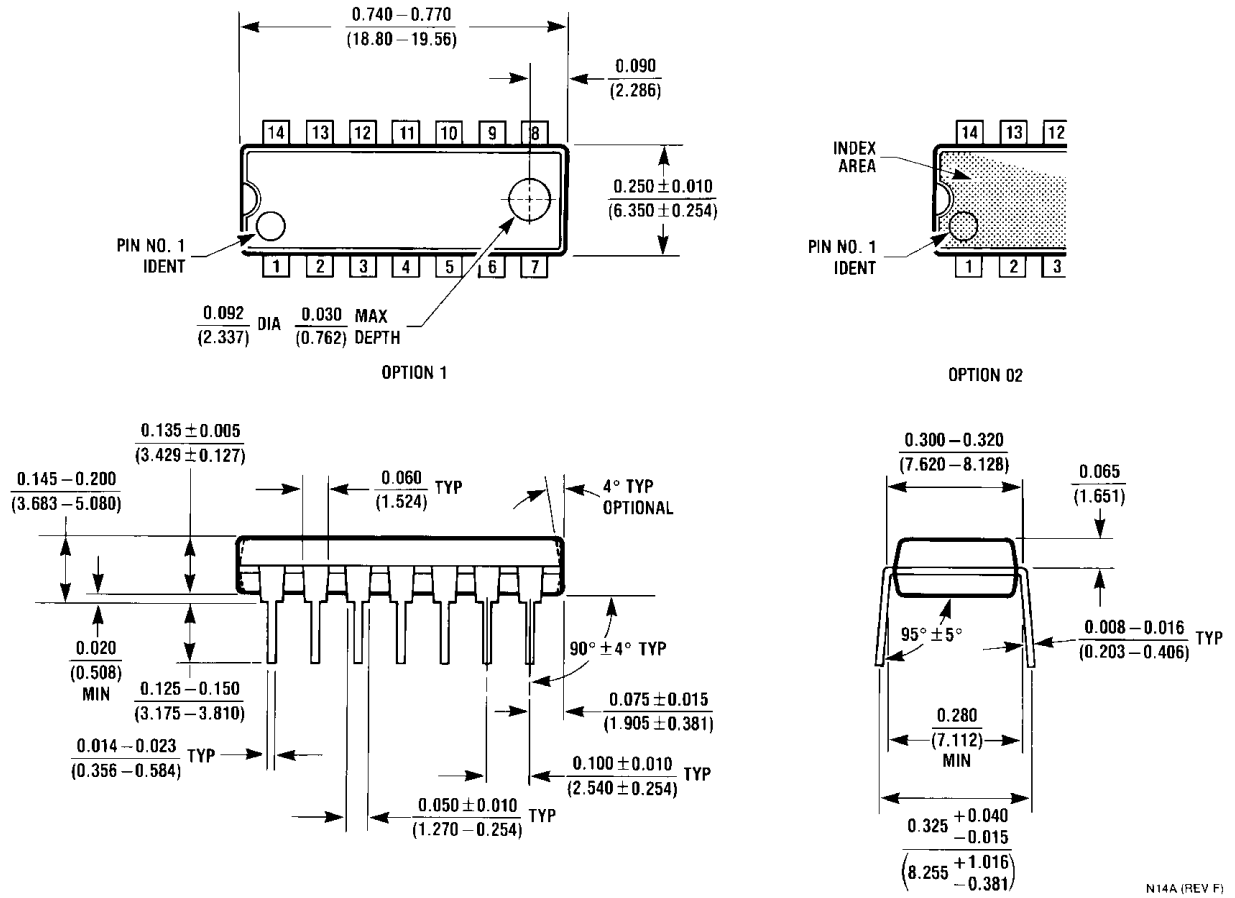



Figure 4. 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

N14A (REV F)



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## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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