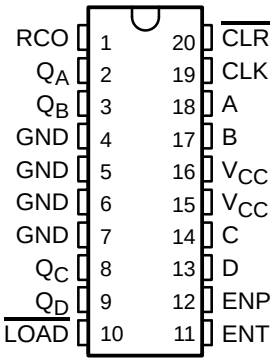
SCAS381 – D3199, AUGUST 1988 – REVISED APRIL 1993

- **Internal Look-Ahead Circuitry for Fast Counting**
- **Carry Output for N-Bit Cascading**
- **Fully Synchronous Operation for Counting**
- **Synchronously Programmable**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

This synchronous, presettable 4-bit decade counter features an internal carry look-ahead circuitry for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple-clock) counters; however, counting spikes may occur on the ripple-carry (RCO) output. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock-input waveform.

These counters are fully programmable in that they may be preset to any number between 0 and 9. As presetting is synchronous, setting up a low level at the load ($\overline{LOAD}$) input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

If one of these decade counters is preset to a number between 10 and 15 or assumes such an invalid state when power is applied, it progresses to the normal sequence within two counts as shown in the state diagram.

The clear function for the 74AC11162 is synchronous, and a low level at the clear ($\overline{CLR}$) input drives all four of the flip-flop outputs low after the next low-to-high transition of the clock regardless of the levels on the count-enable (ENP and ENT) inputs. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to the clear input to synchronously clear the counter to 0000 (LLLL on the Q outputs).

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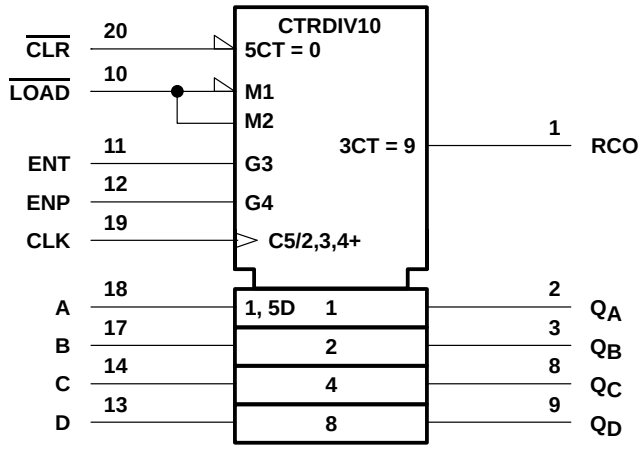
description (continued)

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable (ENP and ENT) inputs and a ripple-carry (RCO) output. Both ENP and ENT must be high to count, and ENT is fed foward to enable RCO. RCO thus enabled produces a high-level pulse while the count is 9 (HLLH). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT inputs are allowed regardless of the level of the clock input.

These counters feature fully independent clock circuits. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the setup and hold times.

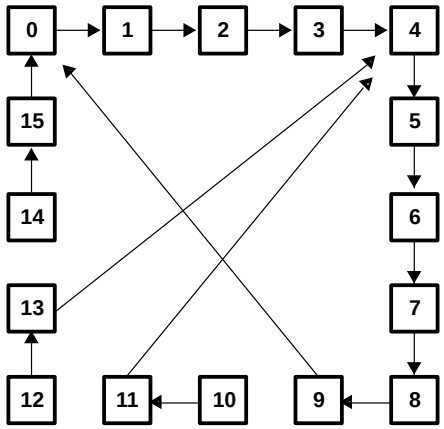
The 74AC11162 is characterized for operation from –40°C to 85°C.

logic symbol†

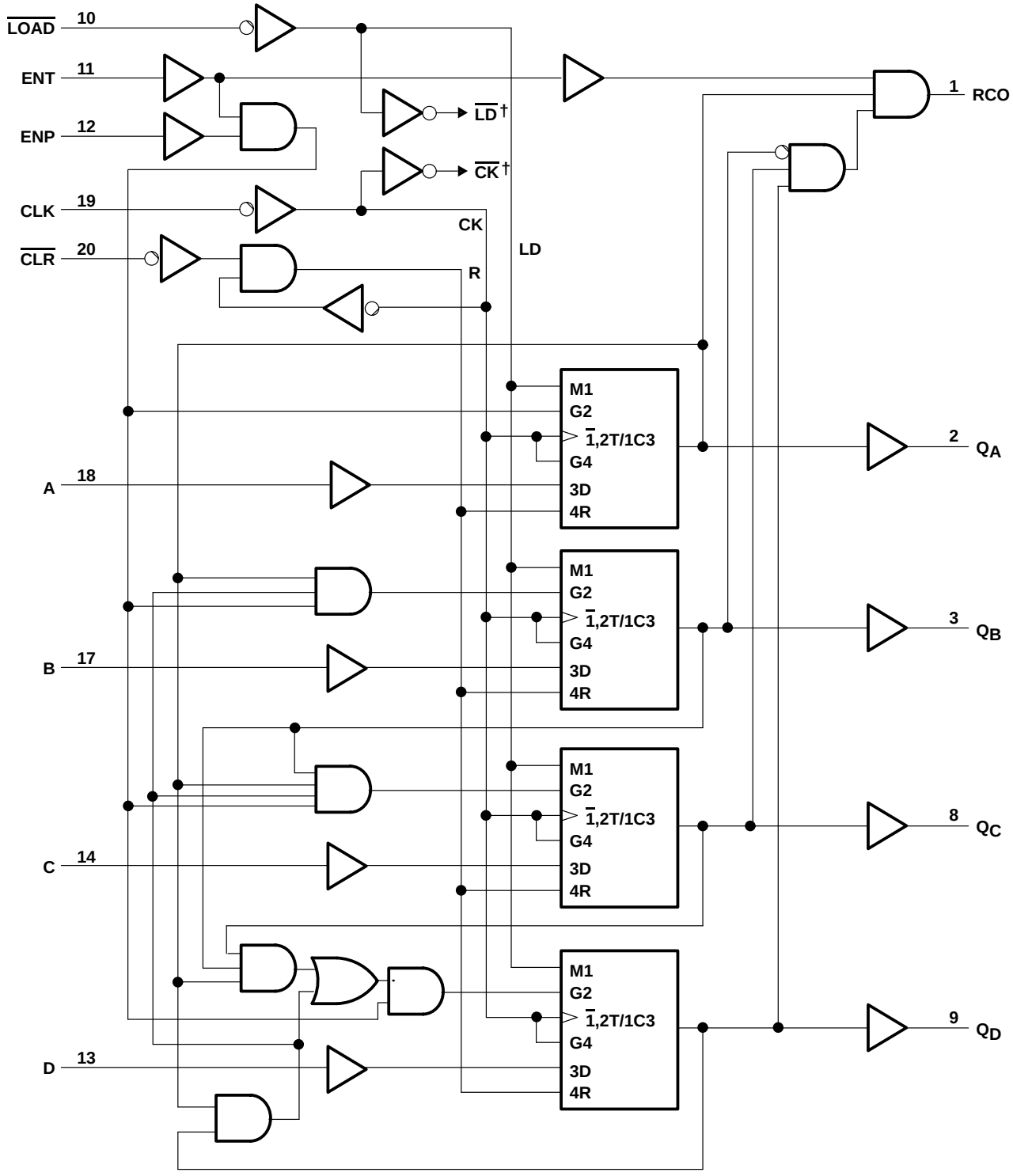


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

state diagram

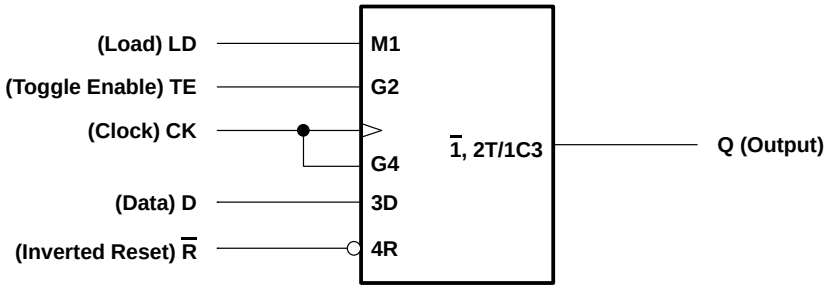


logic diagram (positive logic)

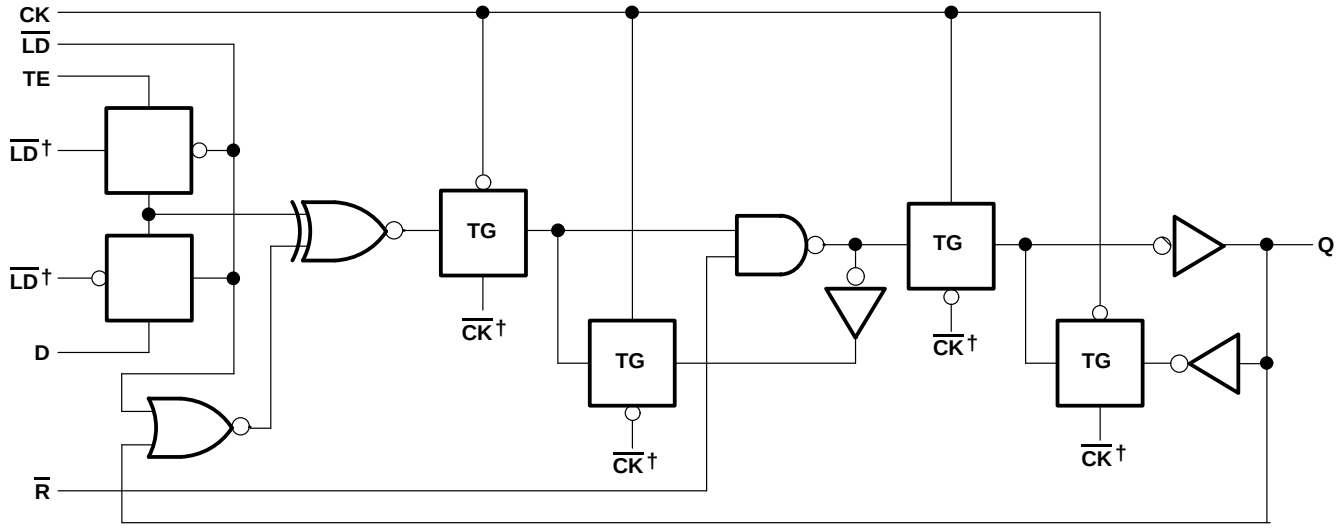


† For the sake of simplicity, the routing of the complementary signals $\overline{LD}$ and $\overline{CK}$ is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

logic symbol



logic diagram, each D/T flip-flop (positive logic)

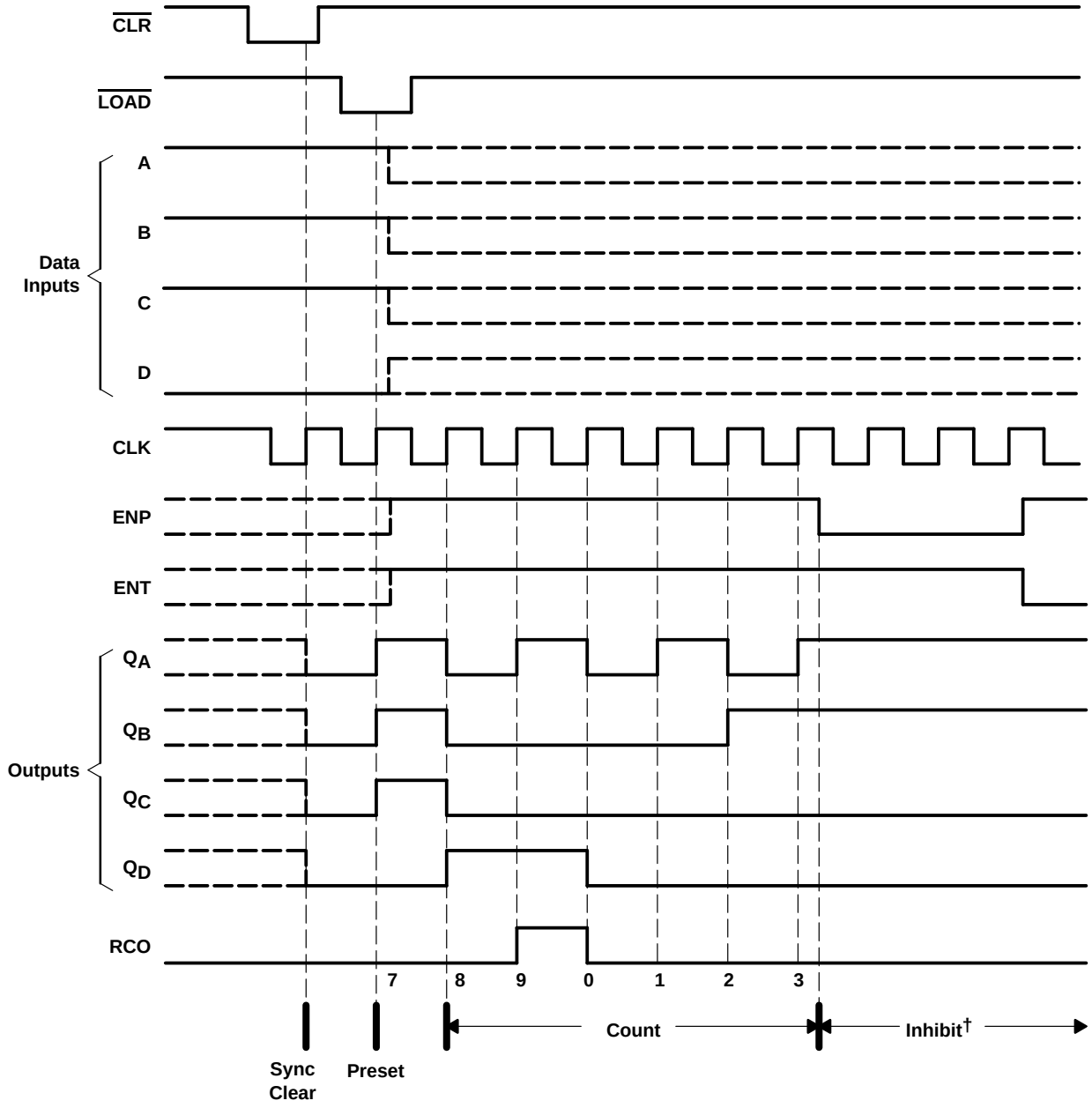


† The origins of the signals $\overline{LD}$ and $\overline{CK}$ are shown in the logic diagram of the overall device.

output sequence

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to BCD seven
3. Count to eight, nine (RCO high), zero, one, two, and three
4. Inhibit



† Counting is inhibited if either or both of ENT and ENP are low.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±125 mA
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}			3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 4.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 4.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			– 4	V
		V_{CC} = 4.5 V			– 24	
		V_{CC} = 4.5 V			– 24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	V
		V_{CC} = 4.5 V			24	
		V_{CC} = 4.5 V			24	
dt/dv	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		– 40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = – 50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = – 4 mA	3 V	2.58			2.48		
	I_{OL} = – 24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = – 75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	V_I = V_{CC} or GND	5 V		3.5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements, V_{CC} = 3.3 V ± 0.3 V (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	66	0	66	MHz
t_w	Pulse duration	CLK low or high	7.5		7.5		ns
t_{su}	Setup time before CLK↑	A, B, C, D	6		6		ns
		$\overline{LOAD}$	6		6		
		ENT, ENP	7.5		7.5		
		$\overline{CLR}$ low or high	7.5		7.5		
t_h	Hold time, all synchronous inputs after CLK↑		1		1		ns

timing requirements, V_{CC} = 5 V ± 0.5 V (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	110	0	110	MHz
t_w	Pulse duration	CLK low or high	4.5		4.5		ns
t_{su}	Setup time before CLK↑	A, B, C, D	4		4		ns
		$\overline{LOAD}$	5		5		
		ENT, ENP	6		6		
		$\overline{CLR}$ low or high	4.5		4.5		
t_h	Hold time, all synchronous inputs after CLK↑		1		1		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			66			66		MHz
t_{PLH}	CLK	RCO	1.5	10.5	14.1	1.5	15.9	ns
t_{PHL}			1.5	12.1	15.8	1.5	18	
t_{PLH}	CLK ($\overline{LOAD}$ high)	Any Q	1.5	8.7	11.7	1.5	13.2	ns
t_{PHL}			1.5	10.2	14.4	1.5	16	
t_{PLH}	CLK ($\overline{LOAD}$ low)	Any Q	1.5	8.7	11.2	1.5	12.6	ns
t_{PHL}			1.5	10.4	14.1	1.5	16	
t_{PLH}	ENT	RCO	1.5	5.8	7.6	1.5	8.5	ns
t_{PHL}			1.5	6.9	9.9	1.5	11	

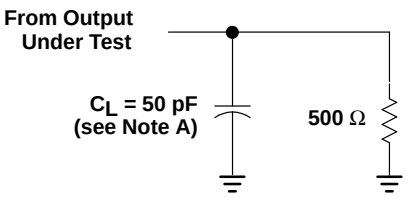
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			110			110		MHz
t_{PLH}	CLK	RCO	1.5	7.7	9.9	1.5	11.2	ns
t_{PHL}			1.5	8.3	11.9	1.5	12.6	
t_{PLH}	CLK ($\overline{LOAD}$ high)	Any Q	1.5	6.4	8.4	1.5	9.5	ns
t_{PHL}			1.5	7.4	10.5	1.5	11.9	
t_{PLH}	CLK ($\overline{LOAD}$ low)	Any Q	1.5	6	7.9	1.5	9	ns
t_{PHL}			1.5	7.2	10.1	1.5	11.5	
t_{PLH}	ENT	RCO	1.5	4	5.5	1.5	6	ns
t_{PHL}			1.5	5	7.4	1.5	8.8	

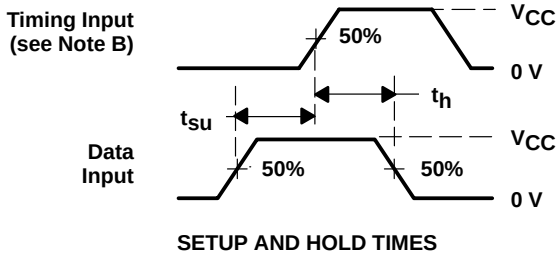
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	54	pF

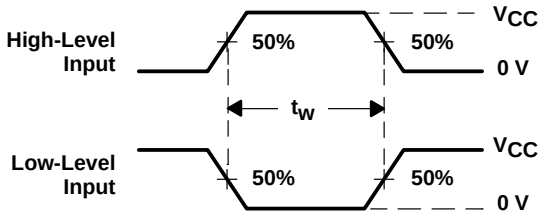
PARAMETER MEASUREMENT INFORMATION



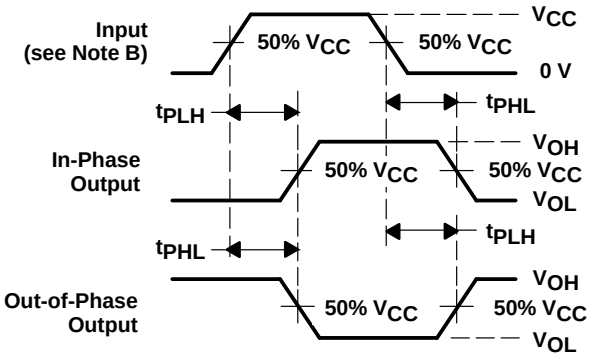
LOAD CIRCUIT



SETUP AND HOLD TIMES



PULSE DURATION



PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns. For testing f_{max} and pulse duration: t_r = 1 to 3 ns, t_f = 1 to 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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