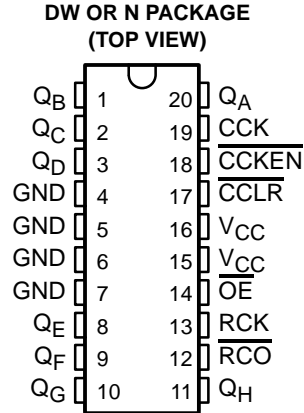


74AC11590
8-BIT BINARY COUNTER
WITH REGISTERED 3-STATE OUTPUTS

SCAS194 – D3988, MARCH 1992 – REVISED APRIL 1993

- Parallel Registered Outputs
- Internal Counters Have Direct Clear
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs



description

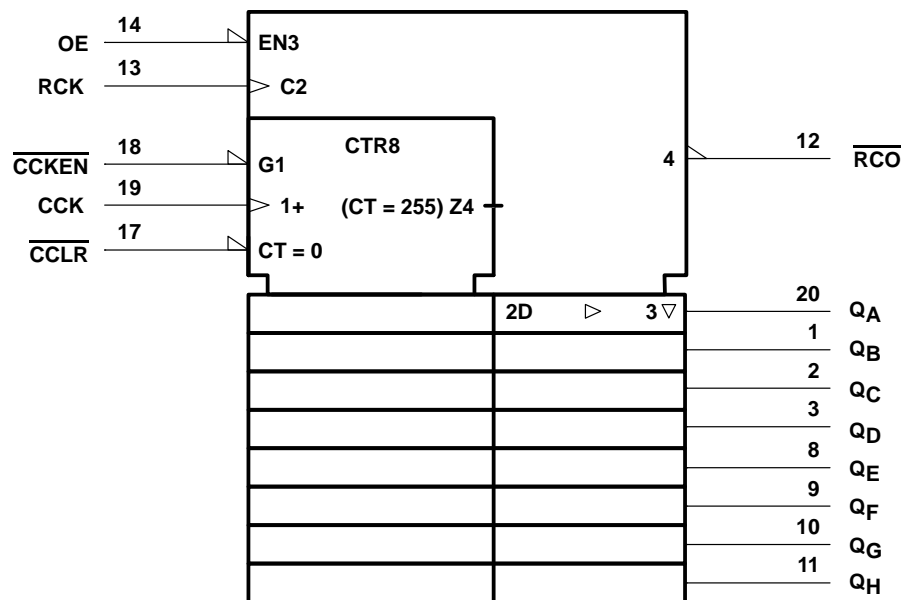
The 74AC11590 contains an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register.

The binary counter features a direct clear (\overline{CCLR}) input and a count-enable (\overline{CCKEN}) input. For cascading, a ripple-carry (\overline{RCO}) output is provided. Expansion is easily accomplished for two stages by connecting \overline{RCO} of the first stage to \overline{CCKEN} of the second stage. Cascading for larger count chains can be accomplished by connecting \overline{RCO} of each stage to CCK of the following stage.

Both the register and the counter have individual positive-edge-triggered clocks. If both clocks are connected together, the counter state is always one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

The 74AC11590 is characterized for operation from -40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

EPIC is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

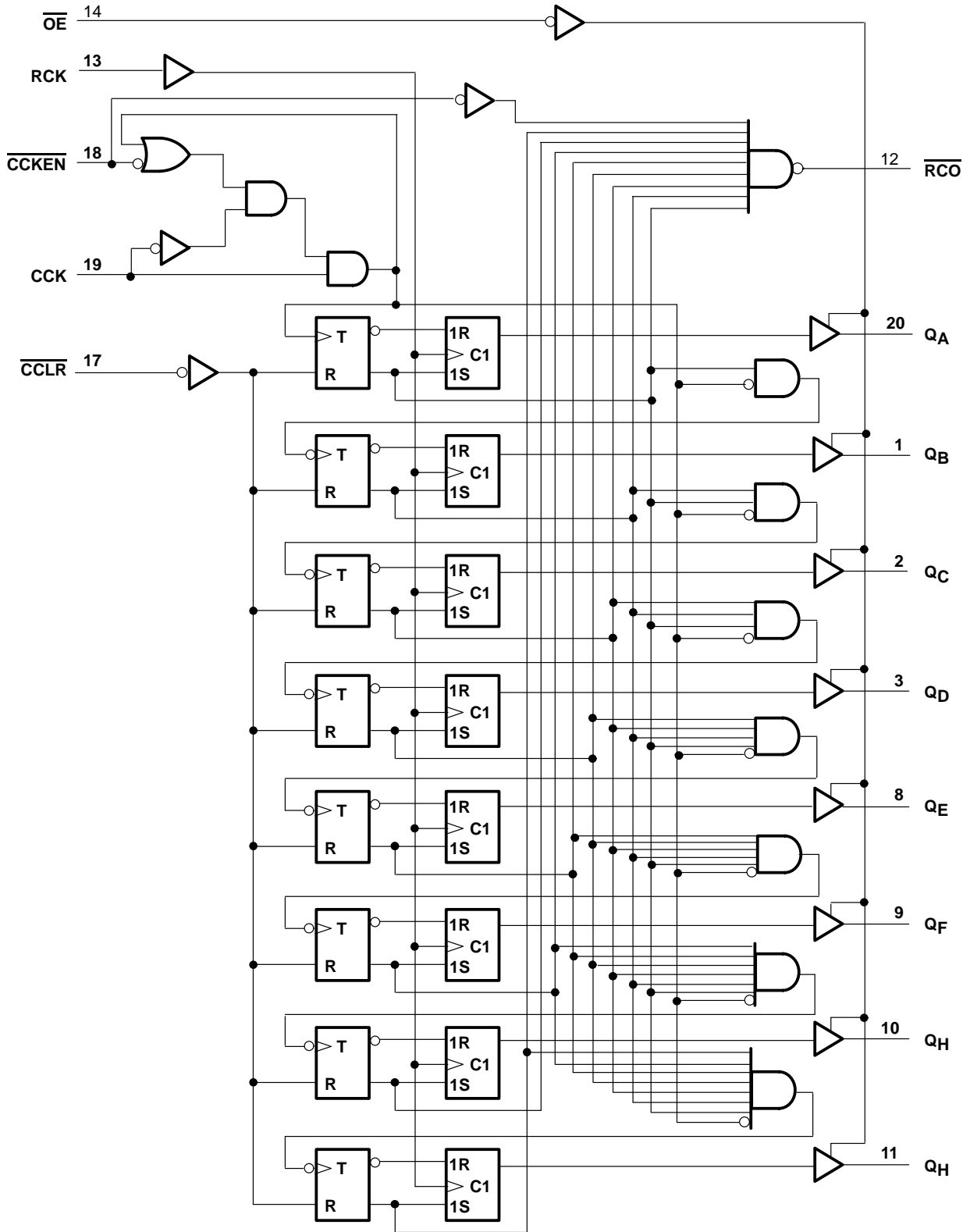
Copyright © 1993, Texas Instruments Incorporated



74AC11590
8-BIT BINARY COUNTER
WITH REGISTERED 3-STATE OUTPUTS

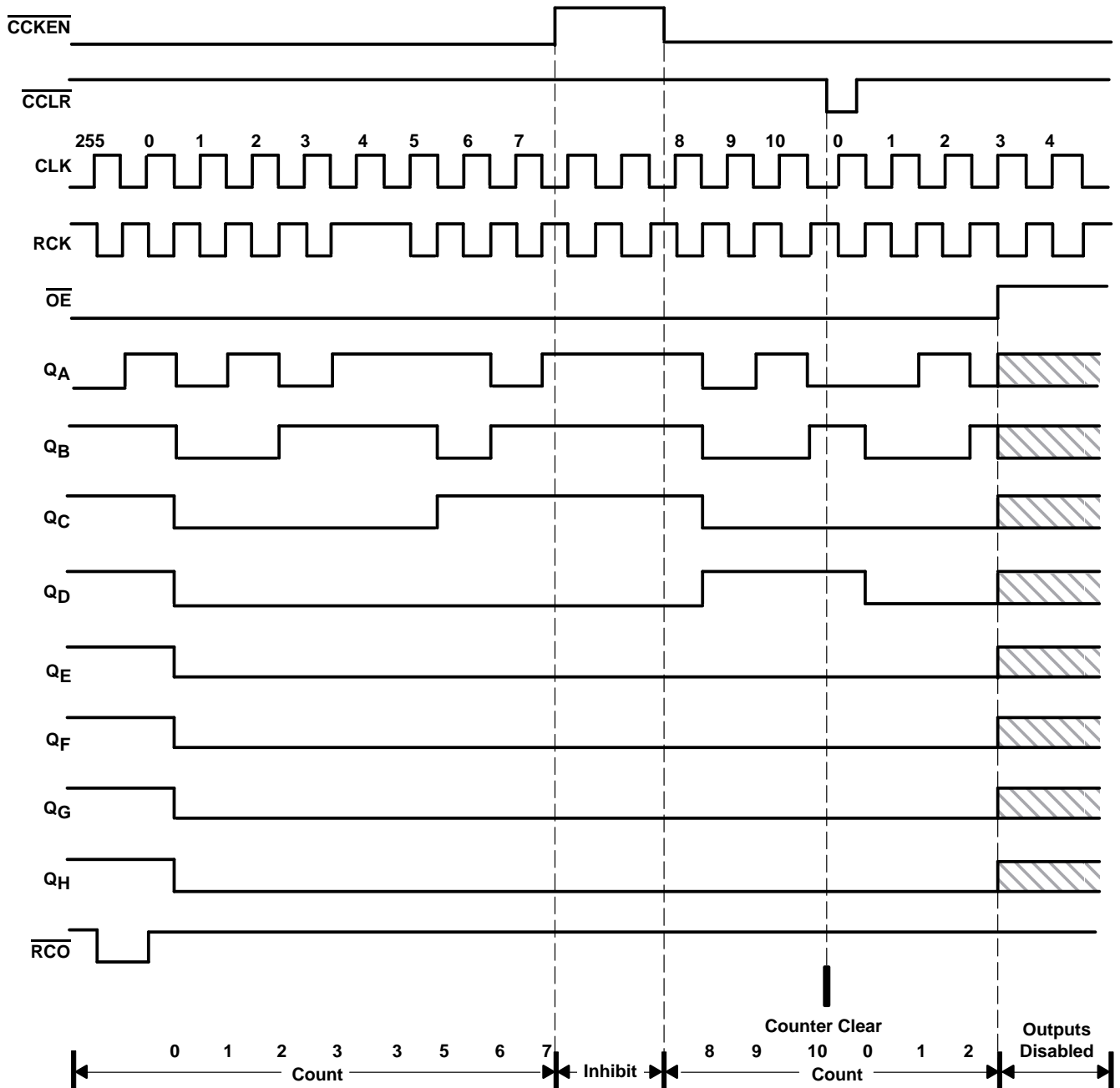
SCAS194 – D3988, MARCH 1992 – REVISED APRIL 1993

logic diagram (positive logic)



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

typical operating sequence



74AC11590
8-BIT BINARY COUNTER
WITH REGISTERED 3-STATE OUTPUTS

SCAS194 – D3988, MARCH 1992 – REVISED APRIL 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±225 mA
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 3$ V	2.1		V
		$V_{CC} = 4.5$ V	3.15		
		$V_{CC} = 5.5$ V	3.85		
V_{IL}	Low-level input voltage	$V_{CC} = 3$ V		0.9	V
		$V_{CC} = 4.5$ V		1.35	
		$V_{CC} = 5.5$ V		1.65	
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 3$ V		–4	mA
		$V_{CC} = 4.5$ V		–24	
		$V_{CC} = 5.5$ V		–24	
I_{OL}	Low-level output current	$V_{CC} = 3$ V		12	mA
		$V_{CC} = 4.5$ V		24	
		$V_{CC} = 5.5$ V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	–40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.



74AC11590
8-BIT BINARY COUNTER
WITH REGISTERED 3-STATE OUTPUTS
SCAS194 – D3988, MARCH 1992 – REVISED APRIL 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V _{OH}	I _{OH} = -50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		
		4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
I _{OH} = -75 mA [†]	5.5 V				3.85			
V _{OL}	I _{OL} = 50 μA	3 V	0.1			0.1		V
		4.5 V	0.1			0.1		
		5.5 V	0.1			0.1		
	I _{OL} = 12 mA	3 V	0.36			0.44		
		4.5 V	0.36			0.44		
		5.5 V	0.36			0.44		
I _{OL} = 75 mA [†]	5.5 V				1.65			
I _I	V _I = V _{CC} or GND	5.5 V	±0.1			±1		μA
I _{OZ}	V _O = V _{CC} or GND	5.5 V	±0.5			±5		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	8			80		μA
C _i	V _I = V _{CC} or GND	5 V	3					pF
C _o	V _O = V _{CC} or GND	5 V	11					pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
f _{clock}	Clock frequency, CCK or RCK	0	50	0	50	MHz
t _w	Pulse duration	CCK or RCK high or low		10		ns
		CCLR low		7.4		
t _{su}	Setup time	CCKEN low before CCK↑		5.2		ns
		CCLR high before CCK↑		3.4		
		CCK↑ before RCK↑ [‡]		8.1		
t _h	Hold time	CCKEN low after CCK↑		0		ns

[‡] This setup time ensures that the register will see stable data from the counter outputs. The clocks may be tied together, in which case the register will be one clock pulse behind the counter.



74AC11590
8-BIT BINARY COUNTER
WITH REGISTERED 3-STATE OUTPUTS

SCAS194 – D3988, MARCH 1992 – REVISED APRIL 1993

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5 V \pm 0.5 V$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ C$		MIN	MAX	UNIT
		MIN	MAX			
f_{clock}	Clock frequency, CCK or RCK	0	80	0	80	MHz
t_w	Pulse duration	CCK or RCK high or low	6.3	6.3		ns
		\overline{CCLR} low	4.9	4.9		
t_{su}	Setup time	\overline{CCKEN} low before CCK \uparrow	3.7	3.7		ns
		\overline{CCLR} high before CCK \uparrow	1.6	1.6		
		CCK \uparrow before RCK $\uparrow\uparrow$	5.5	5.5		
t_h	Hold time	\overline{CCKEN} low after CCK \uparrow	0.5	0.5		ns

† This setup time ensures that the register will see stable data from the counter outputs. The clocks may be tied together, in which case the register will be one clock pulse behind the counter.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3 V \pm 0.3 V$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ C$			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}	CCK or RCK		50			50		MHz
t_{PLH}	CCK	\overline{RCO}	7	13.5	15.9	7	18.3	ns
t_{PHL}			9	16.9	19.5	9	22.1	
t_{PLH}	\overline{CCLR}	\overline{RCO}	6.2	12.4	14.8	6.2	17.1	ns
t_{PLH}	RCK	Q	7.3	13.7	16.2	7.3	18.7	ns
t_{PHL}			7	13.6	15.9	7	17.9	
t_{PZH}	\overline{OE}	Q	7.8	15.5	18.5	7.8	21.1	ns
t_{PZL}			8.5	18.2	21.4	8.5	24.5	
t_{PHZ}	\overline{OE}	Q	6.3	10	11.9	6.3	13.2	ns
t_{PLZ}			6.8	10.8	12.8	6.8	14.1	
t_{PLH}	\overline{CCKEN}	\overline{RCO}	6	11.7	14	6	16.2	ns
t_{PHL}			6	11.6	13.7	6	15.4	

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5 V \pm 0.5 V$ (unless otherwise noted) (see Figure 1)

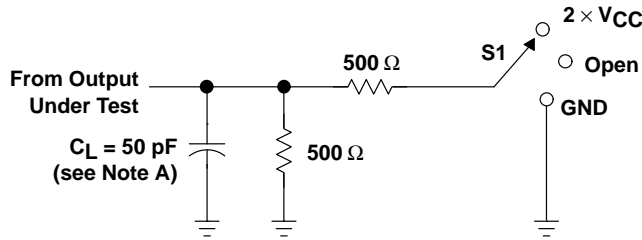
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ C$			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}	CCK or RCK		80			80		MHz
t_{PLH}	CCK	RCO	3.6	7.8	10.2	3.6	11.7	ns
t_{PHL}			4.7	9.8	12.7	4.7	14.4	
t_{PLH}	\overline{CCLR}	\overline{RCO}	3.2	7.2	9.5	3.2	10.9	ns
t_{PLH}	RCK	Q	3.7	8	10.4	3.7	12	ns
t_{PHL}			3.6	8.2	10.7	3.6	12.1	
t_{PZH}	OE	Q	3.8	8.9	11.9	3.8	13.6	ns
t_{PZL}			3.7	9.5	12.6	3.7	14.3	
t_{PHZ}	OE	Q	4.5	7.5	9.4	4.5	10.5	ns
t_{PLZ}			5.4	8.7	10.8	5.4	12	
t_{PLH}	\overline{CCKEN}	\overline{RCO}	3	6.9	9	3	10.4	ns
t_{PHL}			2.9	7	9.2	2.9	10.4	



operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

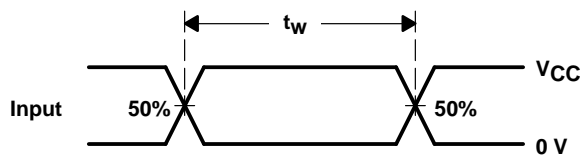
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	66	pF
			43	

PARAMETER MEASUREMENT INFORMATION

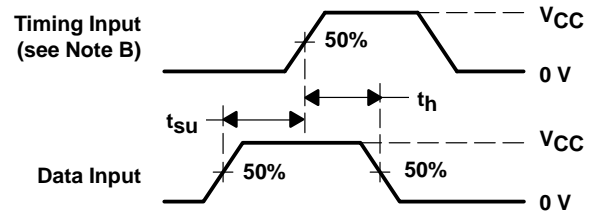


LOAD CIRCUIT

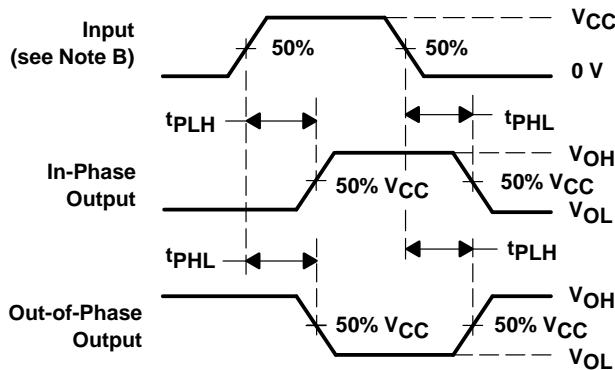
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



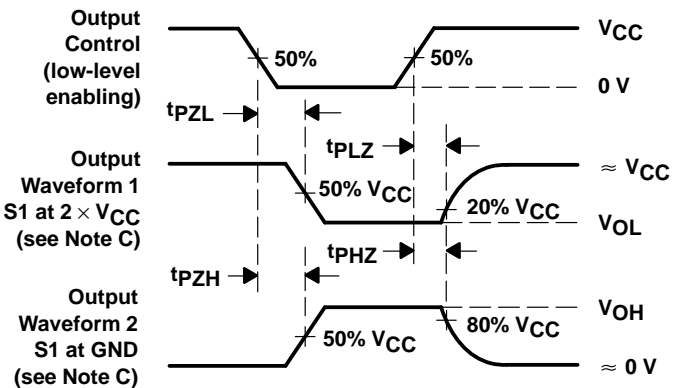
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.