National Semiconductor

April 1993

54AC/74AC169•54ACT/74ACT169
4-Stage Synchronous Bidirectional Counter

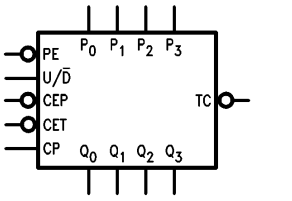
General Description

The 'AC/'ACT169 is fully synchronous 4-stage up/down counter. The 'AC/'ACT169 is a modulo-16 binary counter. It features a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the Clock.

Features

- I_{CC} reduced by 50%
- Synchronous counting and loading
- Built-In lookahead carry capability
- Presettable for programmable operation
- Outputs source/sink 24 mA
- 'ACT has TTL-compatible inputs
- Standard Military Drawing (SMD)
  — 'AC169: 5962-91603

Logic Symbols



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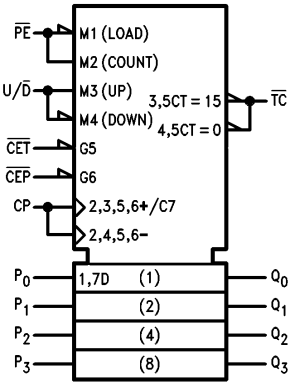
IEEE/IEC



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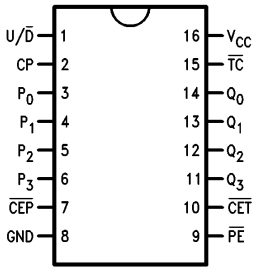
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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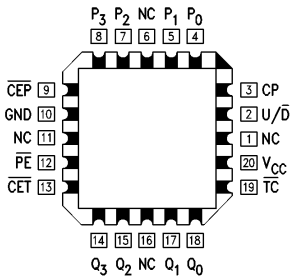
Pin Assignment for LCC



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Pin Names	Description
$\overline{CEP}$	Count Enable Parallel Input
$\overline{CET}$	Count Enable Trickle Input
CP	Clock Pulse Input
P_0–P_3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input
U/$\overline{D}$	Up-Down Count Control Input
Q_0–Q_3	Flip-Flop Outputs
$\overline{TC}$	Terminal Count Output

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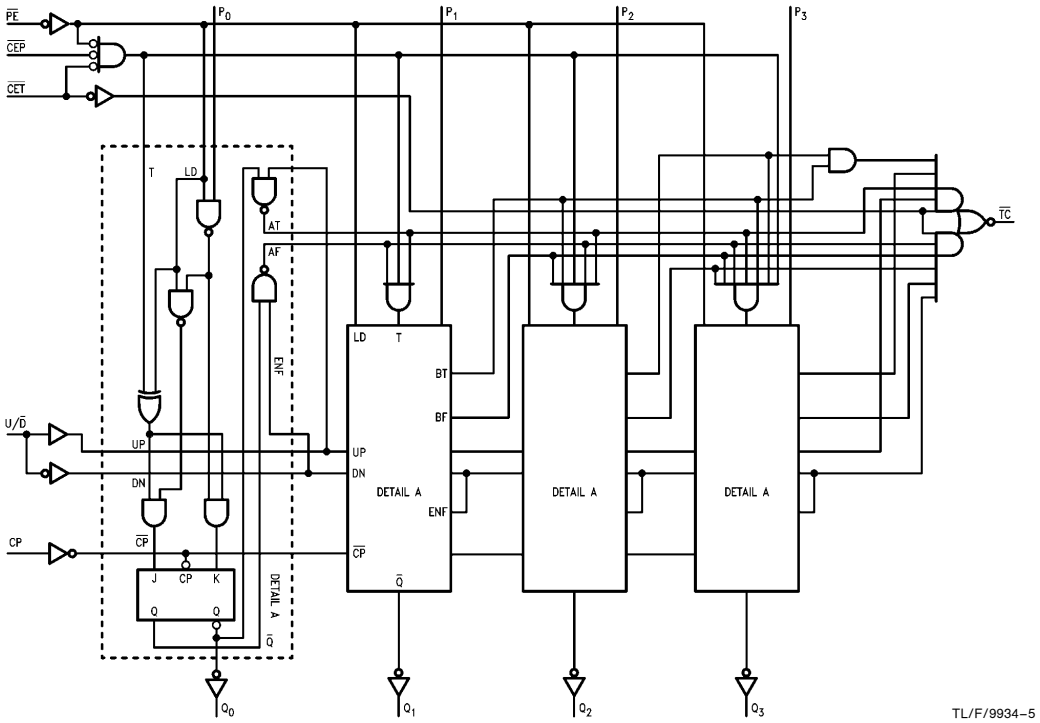
Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

The 'AC/'ACT169 uses edge-triggered J-K-type flip-flops and have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is LOW, the data on the P_0–P_3 inputs enters the flip-flops on the next rising edge of the Clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be LOW and $\overline{PE}$ must be HIGH; the U/$\overline{D}$ input then determines the direction of counting. The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW, provided that $\overline{CET}$ is LOW, when a counter reaches zero in the Count Down mode or reaches 15 in the Count Up mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. If an illegal state occurs, the 'AC169 will return to the legitimate sequence within two counts. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended (see logic equations below).

1) Count Enable = $\overline{CEP}$•$\overline{CET}$•$\overline{PE}$

2) Up: $\overline{TC}$ = Q_0•Q_1•$Q_2$$Q_3$•(Up)•$\overline{CET}$

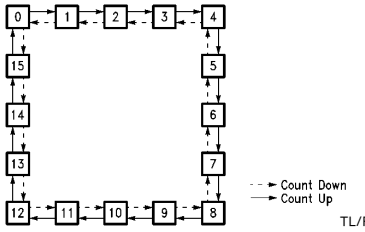
3) Down: $\overline{TC}$ = $\overline{Q}_0$•$\overline{Q}_1$•$\overline{Q}_2$•$\overline{Q}_3$•(Down)•$\overline{CET}$

Mode Select Table

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	Action on Rising Clock Edge
L	X	X	X	Load (P_n to Q_n)
H	L	L	H	Count Up (Increment)
H	L	L	L	Count Down (Decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagrams



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$	74AC $T_A = -55°C$ to $+125°C$	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	$I_{OUT} = -50\ \mu A$
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	$I_{OUT} = 50\ \mu A$
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
I_{OLD}	†Minimum Dynamic Output Current	5.5		50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5		−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	0.8	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4		
		4.5		3.86	3.70	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −24 mA
		5.5		4.86	4.70		
					3.76		
					4.76		
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1		
		4.5		0.36	0.50	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA
		5.5		0.36	0.50		
					0.44		
					0.44		
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	$V_I = V_{CC}$, GND
					±1.0		
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	mA	$V_I = V_{CC}$ − 2.1V
					1.5		
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	mA	V_{OLD} = 1.65V Max
					75		
I_{OHD}		5.5			−50	mA	V_{OHD} = 3.85V Min
					−75		
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	μA	$V_{IN} = V_{CC}$ or GND
					40.0		

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	3.3 5.0	75 100	118 154		55 75		65 90		MHz
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ HIGH or LOW)	3.3 5.0	2.5 1.5	9.5 7.0	13.0 10.0	1.0 1.5	15.0 12.0	2.0 1.5	14.5 11.0	ns
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ HIGH or LOW)	3.3 5.0	2.5 1.5	10.5 7.5	14.5 11.0	1.0 1.5	16.5 13.0	2.0 1.5	16.0 12.0	ns
t_{PLH}	Propagation Delay CP to $\overline{TC}$	3.3 5.0	4.5 3.0	13.5 9.5	18.0 13.0	3.0 3.0	22.0 16.0	3.5 2.0	22.0 14.0	ns
t_{PHL}	Propagation Delay CP to $\overline{TC}$	3.3 5.0	3.5 2.5	13.5 9.5	18.0 13.0	3.0 3.0	22.0 16.0	3.0 2.0	20.5 14.5	ns
t_{PLH}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.3 5.0	3.5 3.0	11.0 8.0	15.0 10.5	1.0 1.5	18.5 13.0	3.0 2.5	16.5 12.0	ns
t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.3 5.0	3.0 2.0	9.5 7.0	12.5 9.0	1.0 1.5	16.0 11.0	2.5 1.5	14.5 10.0	ns
t_{PLH}	Propagation Delay $U/\overline{D}$ to $\overline{TC}$	3.3 5.0	3.5 2.5	11.0 8.0	15.0 10.5	1.0 1.5	18.5 13.0	3.0 2.0	17.0 12.0	ns
t_{PHL}	Propagation Delay $U/\overline{D}$ to $\overline{TC}$	3.3 5.0	2.5 1.5	10.0 7.0	13.5 9.5	1.0 1.5	16.5 12.0	2.0 1.5	15.5 10.5	ns

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	3.0 1.5	4.5 2.5	7.0 4.5	5.0 2.5	ns
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	−1.5 −0.5	0.5 1.5	2.0 2.5	0.5 1.5	ns
t_s	Setup Time, HIGH or LOW $\overline{CEP}$ to CP	3.3 5.0	7.5 4.5	10.5 7.0	13.5 9.0	12.5 8.0	ns
t_h	Hold Time, HIGH or LOW $\overline{CEP}$ to CP	3.3 5.0	−4.5 −2.0	0 0.5	0.5 2.5	0 1.0	ns
t_s	Setup Time, HIGH or LOW $\overline{CET}$ to CP	3.3 5.0	7.0 4.0	10.0 6.5	13.5 9.0	12.0 8.0	ns
t_h	Hold Time, HIGH or LOW $\overline{CET}$ to CP	3.3 5.0	−6.0 −4.0	0 0.5	0.5 2.5	0 1.0	ns
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	3.5 2.0	5.5 3.5	8.5 6.5	6.5 4.0	ns
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	−3.5 −1.5	0 0.5	0.5 2.0	0 0.5	ns
t_s	Setup Time, HIGH or LOW U/$\overline{D}$ to CP	3.3 5.0	7.0 4.5	10.0 6.5	13.0 9.0	11.5 7.5	ns
t_h	Hold Time, HIGH or LOW U/$\overline{D}$ to $\overline{CP}$	3.3 5.0	−7.0 −4.0	0 0.5	0.5 2.0	0 0.5	ns
t_w	CP Pulse Width, HIGH or LOW	3.3 5.0	2.0 2.0	3.0 3.0	5.0 5.0	4.0 3.0	ns

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	5.0	90			75		90		MHz
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ HIGH or LOW)	5.0	2.0	6.5	9.0	1.5	12.5	2.0	10.5	ns
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ HIGH or LOW)	5.0	2.0	6.5	9.0	1.5	12.5	2.0	10.5	ns
t_{PLH}	Propagation Delay CP to $\overline{TC}$	5.0	3.0	9.0	11.5	1.5	16.5	3.0	14.0	ns
t_{PHL}	Propagation Delay CP to $\overline{TC}$	5.0	3.0	9.0	11.5	1.5	16.5	3.0	14.0	ns
t_{PLH}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	5.0	2.5	7.5	10.0	1.5	13.5	2.5	11.5	ns
t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	5.0	2.5	7.5	10.0	1.5	13.5	2.5	11.5	ns
t_{PLH}	Propagation Delay $U/\overline{D}$ to $\overline{TC}$	5.0	2.5	8.0	10.5	1.5	14.5	2.5	12.0	ns
t_{PHL}	Propagation Delay $U/\overline{D}$ to $\overline{TC}$	5.0	2.5	8.0	10.5	1.5	14.5	2.5	12.0	ns

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACT		54ACT	74ACT	Units
			$T_A = +25°C$, $C_L = 50$ pF		$T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to CP	5.0		2.5	4.5	2.5	ns
t_h	Hold Time, HIGH or LOW P_n to CP	5.0		1.5	2.5	1.5	ns
t_s	Setup Time, HIGH or LOW $\overline{CEP}$ to CP	5.0		7.0	9.0	7.0	ns
t_h	Hold Time, HIGH or LOW $\overline{CEP}$ to CP	5.0		0	2.5	0	ns
t_s	Setup Time, HIGH or LOW $\overline{CET}$ to CP	5.0		7.0	9.0	7.0	ns
t_h	Hold Time, HIGH or LOW $\overline{CET}$ to CP	5.0		0	2.5	0	ns
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	5.0		6.0	6.5	6.0	ns
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	5.0		0.5	2.0	0.5	ns
t_s	Setup Time, HIGH or LOW $U/\overline{D}$ to CP	5.0		7.0	9.0	7.0	ns
t_h	Hold Time, HIGH or LOW $U/\overline{D}$ to $\overline{CP}$	5.0		0.5	2.0	0.5	ns
t_w	CP Pulse Width, HIGH or LOW	5.0		4.0	5.0	4.0	ns

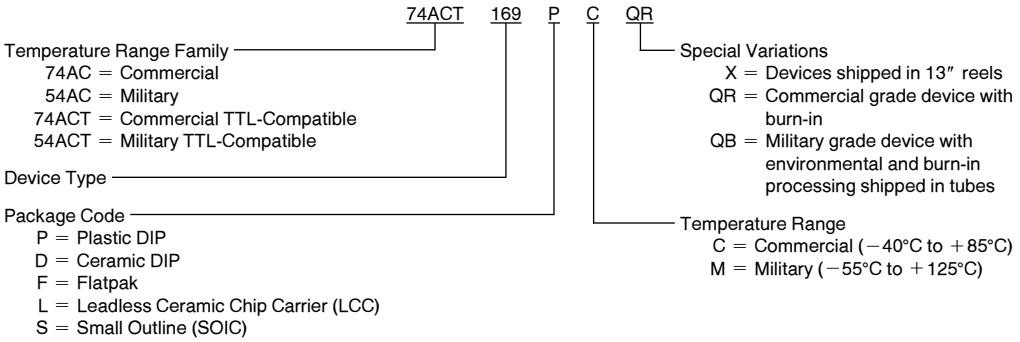
*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

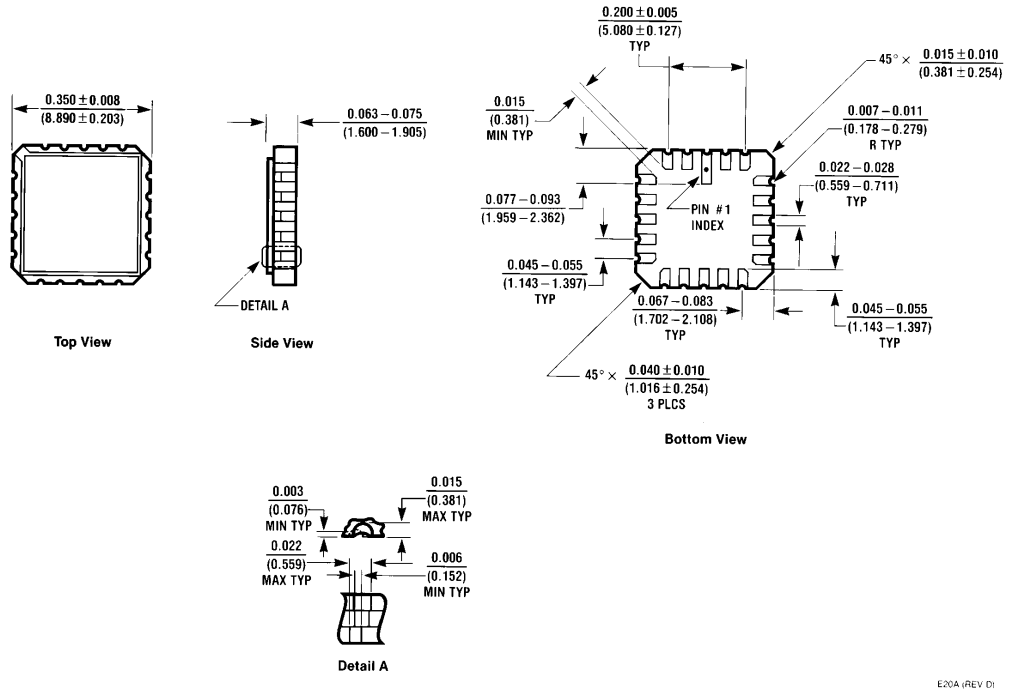
Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD}	Power Dissipation Capacitance	60.0	pF	V_{CC} = 5.0V

Ordering Information

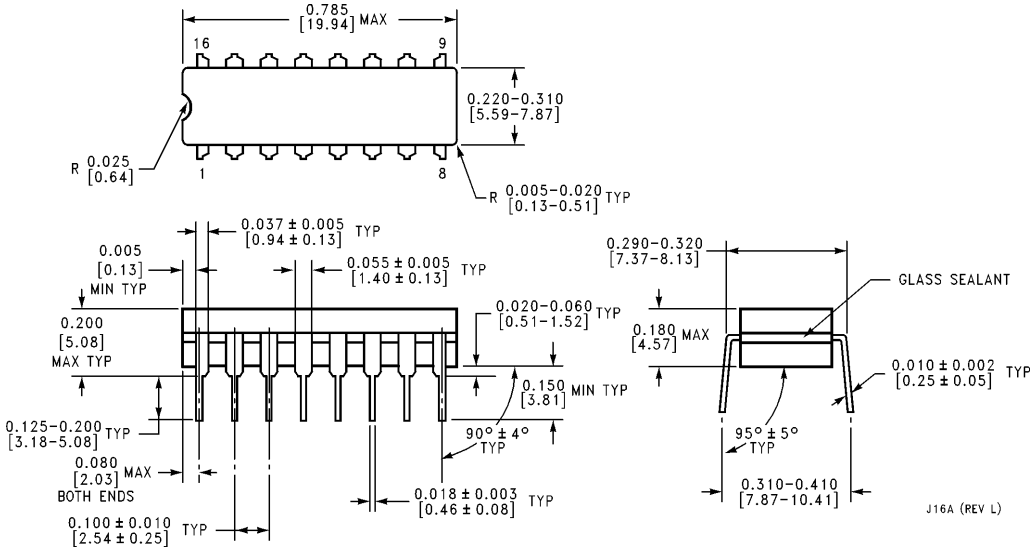
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



Physical Dimensions inches (millimeters)

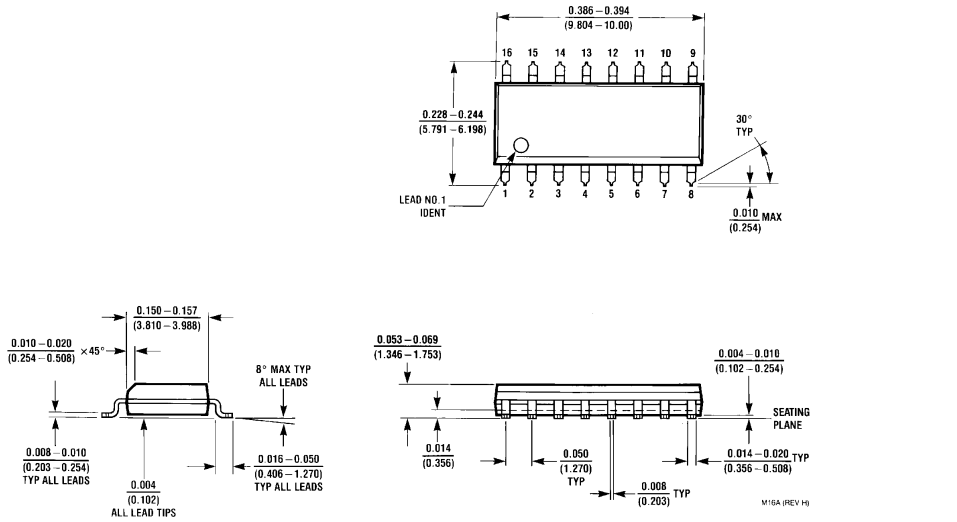


20-Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

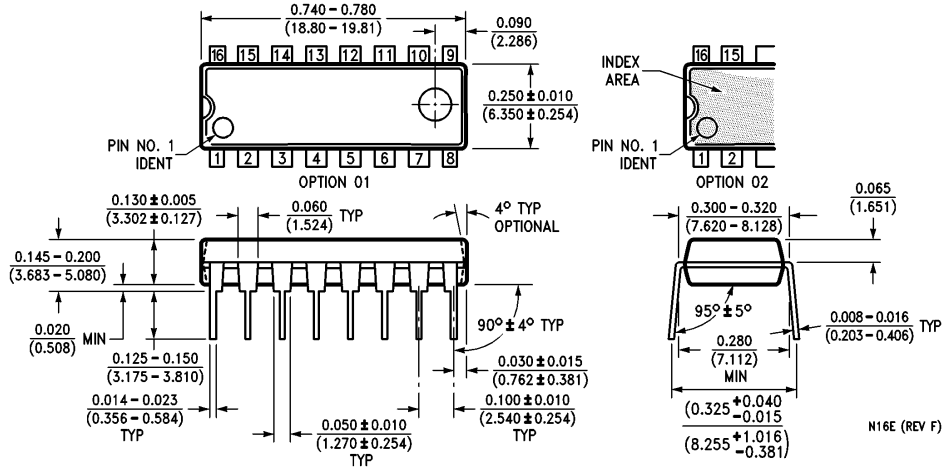


16-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)

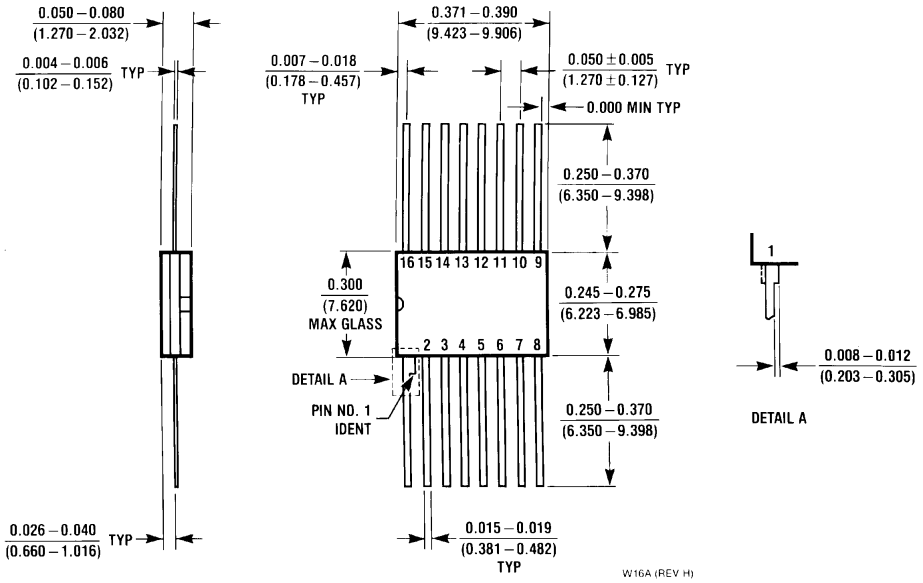


16-Lead Small Outline Integrated Circuit (S)
NS Package Number M16A



16-Lead Plastic Dual-In-Line Package (P)
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flatpak (F)
NS Package Number W16A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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