

# 54ACT11109, 74ACT11109 DUAL J- $\bar{K}$ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SCAS451 – FEBRUARY 1987 – REVISED APRIL 1993

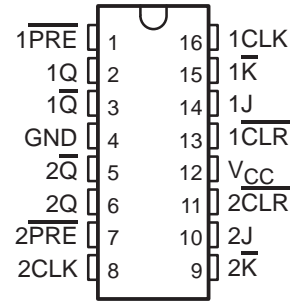
- Inputs Are TTL-Voltage Compatible
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin  $V_{CC}$  and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

## description

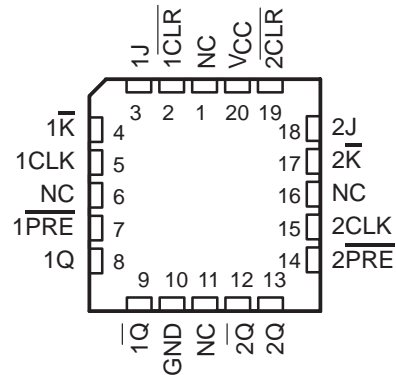
These devices contain two independent J- $\bar{K}$  positive-edge-triggered flip-flops. A low level at the preset ( $1\bar{PRE}$  or  $2\bar{PRE}$ ) or clear ( $1\bar{CLR}$  or  $2\bar{CLR}$ ) input sets or resets the outputs regardless of the levels of the other inputs. When  $\bar{PRE}$  and  $\bar{CLR}$  are inactive (high), data at the J and  $\bar{K}$  inputs meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the J and  $\bar{K}$  inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding  $\bar{K}$  and tying J high. They also can perform as D-type flip-flops if J and  $\bar{K}$  are tied together.

The 54ACT11109 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The 74ACT11109 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

54ACT11109 . . . J PACKAGE  
74ACT11109 . . . D OR N PACKAGE  
(TOP VIEW)



54ACT11109 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUTS					OUTPUTS	
$\bar{PRE}$	$\bar{CLR}$	CLK	J	$\bar{K}$	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H <sup>†</sup>	H <sup>†</sup>
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q <sub>0</sub>	$\bar{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q <sub>0</sub>	$\bar{Q}_0$

<sup>†</sup> This configuration is nonstable; that is, it will not persist when either  $\bar{PRE}$  or  $\bar{CLR}$  returns to the inactive (high) level.

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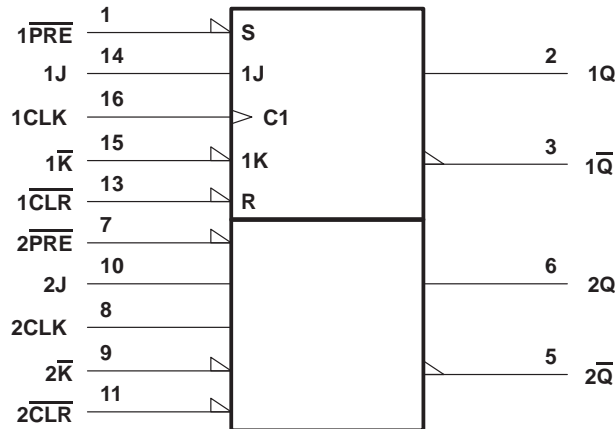
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the D, J, and N packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	–0.5 V to 6 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through $V_{CC}$ or GND	±100 mA
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

## recommended operating conditions

	54ACT11109		74ACT11109		UNIT
	MIN	MAX	MIN	MAX	
$V_{CC}$ Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$ High-level input voltage	2		2		V
$V_{IL}$ Low-level input voltage		0.8		0.8	V
$V_I$ Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$V_O$ Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$ High-level output current		–24		–24	mA
$I_{OL}$ Low-level output current		24		24	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	0	10	0	10	ns/V
$T_A$ Operating free-air temperature	–55	125	–40	85	°C

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**DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS**  
**WITH CLEAR AND PRESET**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			54ACT11109		74ACT11109		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I <sub>OH</sub> = -24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I <sub>OH</sub> = -50 mA <sup>†</sup>	5.5 V				3.85				
I <sub>OH</sub> = -75 mA <sup>†</sup>	5.5 V						3.85			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V				0.1		0.1		V
		5.5 V				0.1		0.1		
	I <sub>OL</sub> = 24 mA	4.5 V				0.36		0.44		
		5.5 V				0.36		0.44		
	I <sub>OL</sub> = 50 mA <sup>†</sup>	5.5 V				1.65				
I <sub>OL</sub> = 75 mA <sup>†</sup>	5.5 V						1.65			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V	±0.1			±1		±1		μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V	4			80		40		μA
ΔI <sub>CC</sub> <sup>‡</sup>	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V	0.9			1		1		mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V	3.5							pF

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

<sup>‡</sup> This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

**timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

		T <sub>A</sub> = 25°C		54ACT11109		74ACT11109		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	0	100	0	100	0	100	MHz
t <sub>w</sub>	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low		5.5		5.5		ns
		CLK high or low		5		5		
t <sub>su</sub>	Setup time before CLK <sup>↑</sup>	Data high or low		5.5		5.5		ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive		2		2		
t <sub>h</sub>	Hold time, data after CLK <sup>↑</sup>	0		0		0		ns

**switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			54ACT11109		74ACT11109		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			100	125		100		100	MHz	
t <sub>PLH</sub>	PRE or CLR	Q or $\overline{Q}$	1.5	5.5	8.6	1.5	9.8	1.5	9.2	ns
t <sub>PHL</sub>			1.5	6	10.8	1.5	12.6	1.5	11.8	
t <sub>PLH</sub>	CLK	Q or $\overline{Q}$	1.5	6	8.3	1.5	9.7	1.5	9.1	ns
t <sub>PHL</sub>			1.5	5.5	7.6	1.5	9	1.5	8.3	



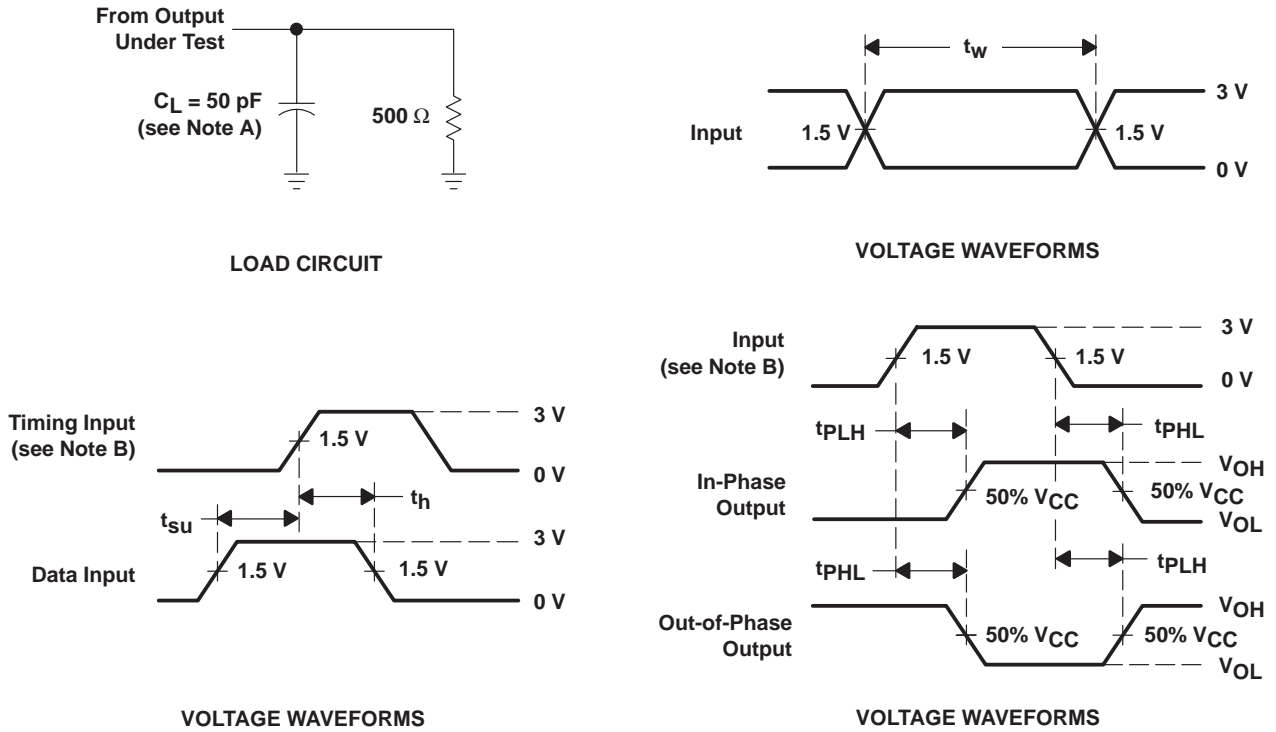
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operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance per flip-flop	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	31	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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