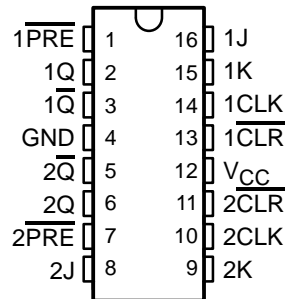


74ACT11112 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOP WITH CLEAR AND PRESET

SCAS064A – D3339, JUNE 1989 – REVISED APRIL 1993

- Inputs Are TTL-Voltage Compatible
- Fully Buffered to Offer Maximum Isolation From External Disturbance
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs

D OR N PACKAGE
(TOP VIEW)



description

This device contains two independent J-K negative-edge-triggered flip-flops. A low level at the \overline{PRE} or \overline{CLR} input sets or resets the outputs regardless of the levels of the other inputs. When \overline{PRE} and \overline{CLR} are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold-time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The 74ACT11112 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

INPUTS					OUTPUTS	
\overline{PRE}	\overline{CLR}	CLK	J	K	Q	\overline{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H [†]	H [†]
H	H	↓	L	L	Q ₀	\overline{Q}_0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	TOGGLE
H	H	H	X	X	Q ₀	\overline{Q}_0

† This configuration is nonstable; that is, it will not persist when either \overline{PRE} or \overline{CLR} returns to the inactive (high) level.

EPIC is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



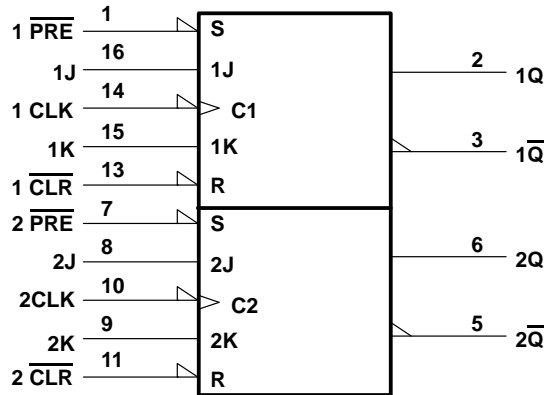
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1993, Texas Instruments Incorporated

74ACT11112 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOP WITH CLEAR AND PRESET

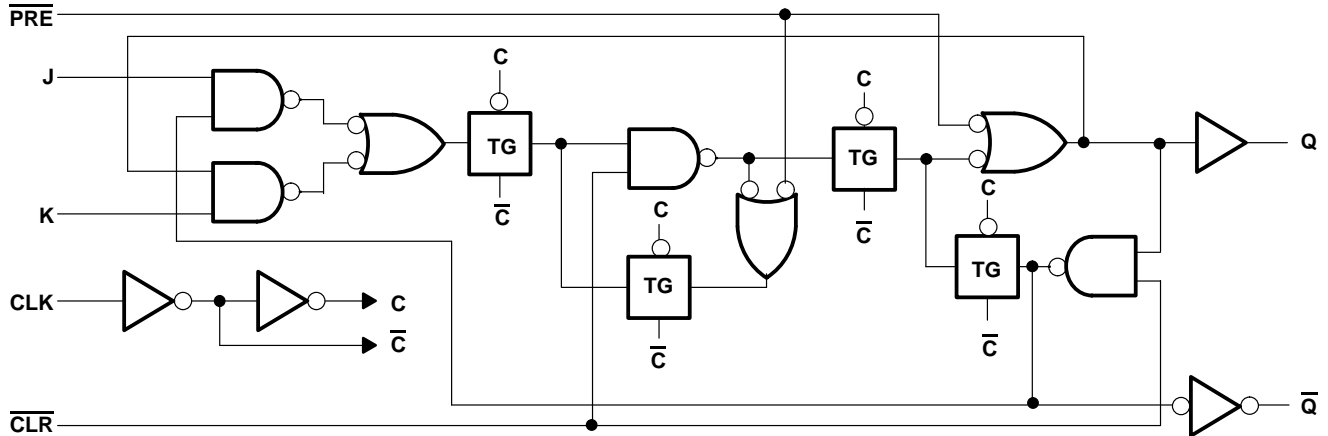
SCAS064A – D3339, JUNE 1989 – REVISED APRIL 1993

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-42.

logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 100 mA
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

74ACT11112
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOP
WITH CLEAR AND PRESET

SCAS064A – D3339, JUNE 1989 – REVISED APRIL 1993

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		-24	mA
I_{OL}	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4			4.4	V	
		5.5 V	5.4			5.4		
	$I_{OH} = -24 \text{ mA}$	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	$I_{OH} = -75 \text{ mA}^\dagger$	5.5 V				3.85		
V_{OL}	$I_{OL} = 50 \mu\text{A}$	4.5 V				0.1	V	
		5.5 V				0.1		
	$I_{OL} = 24 \text{ mA}$	4.5 V				0.36		
		5.5 V				0.36		
	$I_{OL} = 75 \text{ mA}^\dagger$	5.5 V				1.65		
I_I	$V_I = V_{CC}$ or GND	5.5 V				± 0.1	± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V				4	40	μA
ΔI_{CC}^\ddagger	$V_I = V_{CC}$ or GND	5.5 V				0.9	1	mA
C_i	$V_I = V_{CC}$ or GND	5 V	3.5					pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] This parameter is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
f_{clock}	Clock frequency	125		125		MHz
t_w	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	4	4		ns
		CLK high or low	4	4		
t_{su}	Setup time before CLK \downarrow	Data high or low	3.5	4.5		ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	2	2		
t_h	Hold time after CLK \downarrow	1.5	1.5	1.5		ns



74ACT11112 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOP WITH CLEAR AND PRESET

SCAS064A – D3339, JUNE 1989 – REVISED APRIL 1993

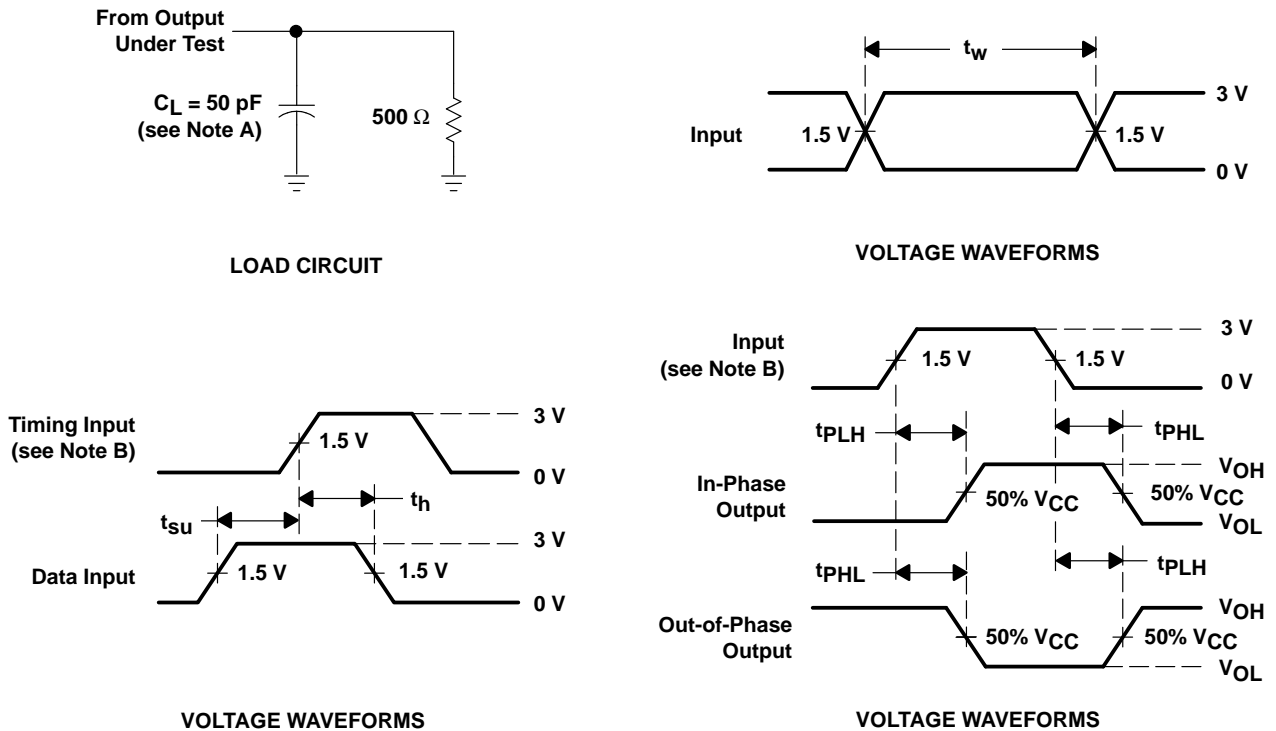
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f _{max}			125			125		MHz
t _{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	1.5	3.6	6.3	1.5	6.8	ns
t _{PHL}			1.5	4.6	7.4	1.5	8	
t _{PLH}	CLK	Q or $\overline{\text{Q}}$	1.5	4.2	7	1.5	7.7	ns
t _{PHL}			1.5	4.7	7.4	1.5	8.4	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per flip-flop	C _L = 50 pF, f = 1 MHz	39	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.

C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.