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ACL Products	

# 74AC/ACT11158

## Quad 2-input multiplexer, INV

### FEATURES

- Output capability:  $\pm 24$  mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- Center-pin  $V_{CC}$  and ground configuration to minimize high-speed switching noise
- $I_{CC}$  category: MSI

### DESCRIPTION

The 74AC/ACT11158 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11158 provides four 2-to-1 multiplexers with a common selector and a common enable. The state of the Select (S) input determines the particular register from which the data comes. The Enable ( $\bar{E}$ ) input is active-Low. When  $\bar{E}$  is High, all of the inverting outputs ( $\bar{Y}$ ) are forced High regardless of all other input conditions.

The device is the logic implementation of a 4-pole, 2 position switch where the position of the switch is determined by the logic levels supplied to the Select input.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}C$ ; GND = 0V; $V_{CC} = 5.0V$	TYPICAL		UNIT
			AC	ACT	
$t_{PLH}/t_{PHL}$	Propagation delay $nI_0, nI_1$ to $n\bar{Y}$	$C_L = 50pF$	3.8	5.5	ns
$C_{PD}$	Power dissipation capacitance per multiplexer <sup>1</sup>	$f = 1MHz$ ; $C_L = 50pF$	33	37	pF
$C_{IN}$	Input capacitance	$V_I = 0V$ or $V_{CC}$	3.5	3.5	pF
$I_{LATCH}$	Latch-up current	Per Jeduc JC40.2 Standard 17	500	500	mA

#### Note:

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_I + \sum (C_L \times V_{CC}^2 \times f_O) \text{ where:}$$

$f_I$  = input frequency in MHz,  $C_L$  = output load capacitance in pF,

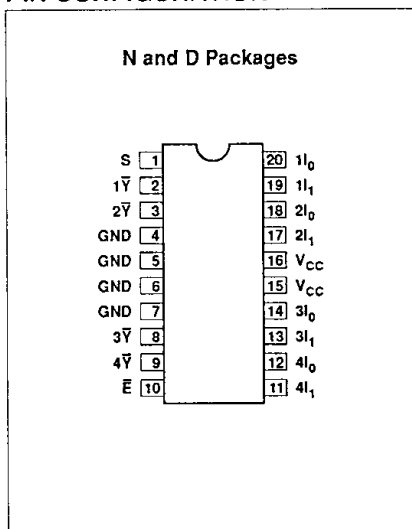
$f_O$  = output frequency in MHz,  $V_{CC}$  = supply voltage in V,

$\sum (C_L \times V_{CC}^2 \times f_O)$  = sum of outputs

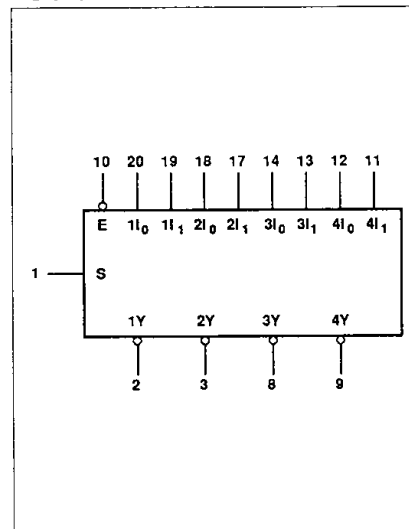
### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11158N 74ACT11158N
20-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11158D 74ACT11158D

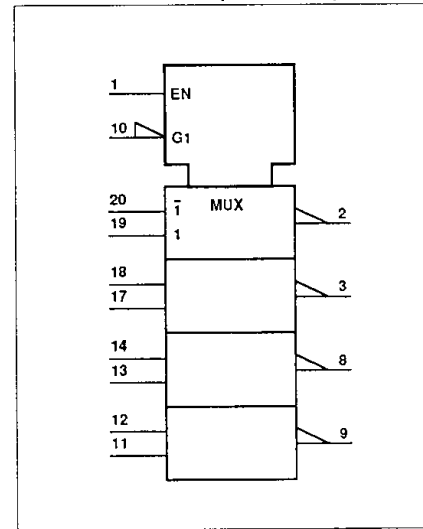
### PIN CONFIGURATION



### LOGIC SYMBOL



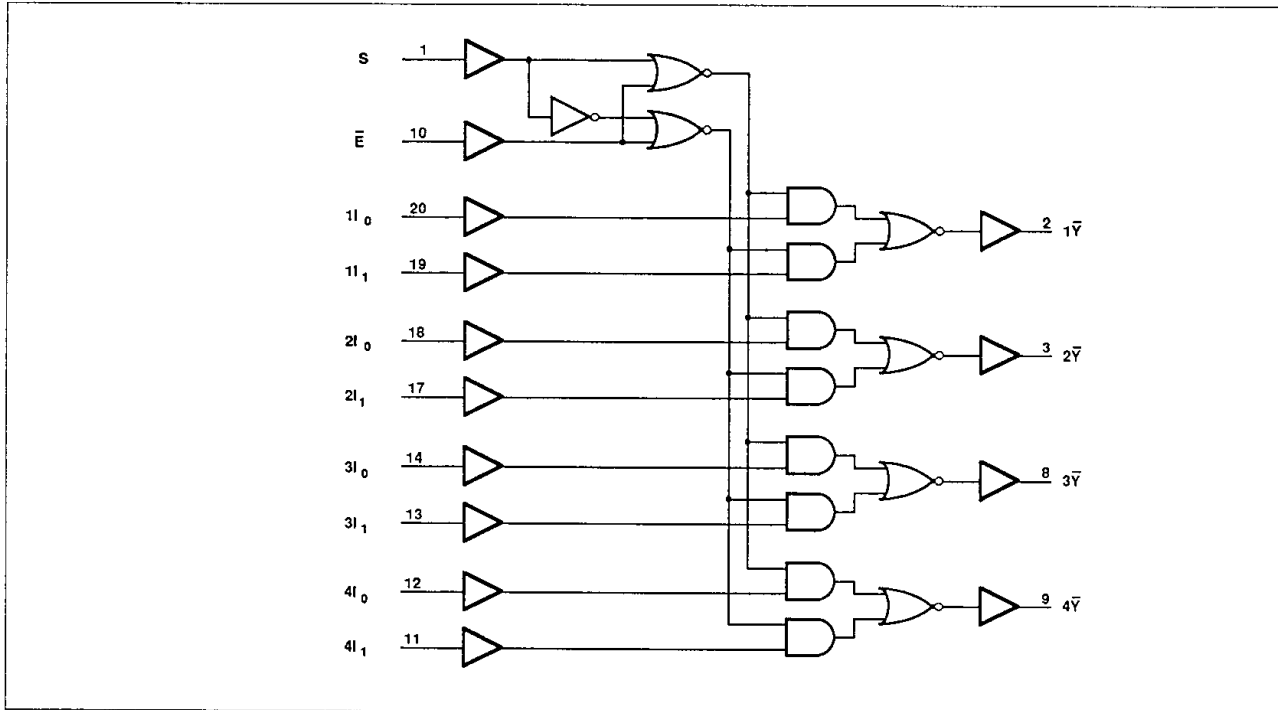
### LOGIC SYMBOL (IEEE/IEC)



# Quad 2-input multiplexer, INV

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## LOGIC DIAGRAM



## PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	S	Common select input
20, 18, 14, 12	nl <sub>0</sub> - nl <sub>0</sub>	Data inputs
19, 17, 13, 11	nl <sub>1</sub> - nl <sub>1</sub>	Data inputs
2, 3, 8, 9	1Y-bar - 4Y-bar	Data outputs
10	E-bar	Output enable input
4, 5, 6, 7	GND	Ground (0V)
15, 16	V <sub>CC</sub>	Positive supply voltage

## FUNCTION TABLE

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
		nl <sub>0</sub>	nl <sub>1</sub>	
E-bar	S	nl <sub>0</sub>	nl <sub>1</sub>	nY-bar
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

## Quad 2-input multiplexer, INV

## 74AC/ACT11158

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11158			74ACT11158			UNIT
		Min	Nom	Max	Min	Nom	Max	
$V_{CC}$	DC supply voltage	3.0 <sup>1</sup>	5.0	5.5	4.5	5.0	5.5	V
$V_I$	Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$\Delta t/\Delta v$	Input transition rise or fall rate	Data	0	10	0		10	ns/V
		Select and Enable	0	5	0		5	
$T_{amb}$	Operating free-air temperature range	-40		+85	-40		+85	°C

## NOTE:

- No electrical or switching characteristics are specified at  $V_{CC} < 3V$ . Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 TO +7.0	V
$I_{IK}$ or $V_I$	DC input diode current <sup>2</sup>	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to $V_{CC} + 0.5$	V
$I_{OK}$ or $V_O$	DC output diode current <sup>2</sup>	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to $V_{CC} + 0.5$	V
$I_O$	DC output source or sink current per output pin	$V_O = 0$ to $V_{CC}$	±50	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ current		±100	mA
	DC ground current		±100	
$T_{STG}$	Storage temperature		-65 to 150	°C
$P_{TOT}$	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

## NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	74AC11158				74ACT11158				UNIT	
				T <sub>amb</sub> = +25°C		T <sub>amb</sub> = -40°C to +85°C		T <sub>amb</sub> = +25°C		T <sub>amb</sub> = -40°C to +85°C			
				Min	Max	Min	Max	Min	Max	Min	Max		
V <sub>IH</sub>	High-level input voltage		3.0	2.10		2.10						V	
			4.5	3.15		3.15		2.0		2.0			
			5.5	3.85		3.85		2.0		2.0			
V <sub>IL</sub>	Low-level input voltage		3.0		0.90		0.90					V	
			4.5		1.35		1.35		0.8		0.8		
			5.5		1.65		1.65		0.8		0.8		
V <sub>OH</sub>	High-level output voltage	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OH</sub> = -50μA	3.0	2.9		2.9					V	
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I <sub>OH</sub> = -4mA	3.0	2.58		2.48						
				4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
				5.5			3.85				3.85		
V <sub>OL</sub>	Low-level output voltage	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OL</sub> = 50μA	3.0		0.1		0.1				V	
				4.5		0.1		0.1		0.1			0.1
				5.5		0.1		0.1		0.1			0.1
			I <sub>OL</sub> = 12mA	3.0		0.36		0.44					
				4.5		0.36		0.44		0.36			0.44
			I <sub>OL</sub> = 24mA	3.0		0.36		0.44		0.36			0.44
				5.5		0.36		0.44		0.36			0.44
I <sub>OL</sub> = 75mA <sup>1</sup>	5.5				1.65				1.65				
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5		±0.1		±1.0		±0.1		±1.0	μA	
I <sub>CC</sub>	Quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0mA	5.5		8.0		80		8.0		80	μA	
ΔI <sub>CC</sub>	Supply current, TTL inputs High <sup>2</sup>	One input at 3.4V, other inputs at V <sub>CC</sub> or GND	5.5						0.9		1.0	mA	

## NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V<sub>CC</sub>.

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## AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11158					UNIT
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay nI <sub>0</sub> , nI <sub>1</sub> to n $\bar{Y}$	1	1.5 1.5	5.8 5.9	7.3 7.6	1.5 1.5	8.0 8.4	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay S to n $\bar{Y}$	1	1.5 1.5	6.5 6.8	8.0 8.4	1.5 1.5	8.8 9.3	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay $\bar{E}$ to n $\bar{Y}$	2	1.5 1.5	5.7 6.3	7.1 7.8	1.5 1.5	8.0 8.7	ns

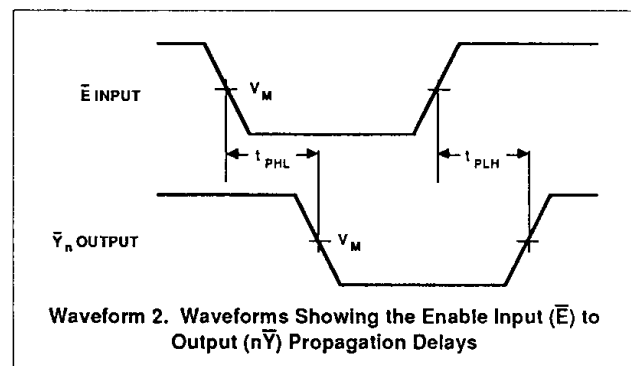
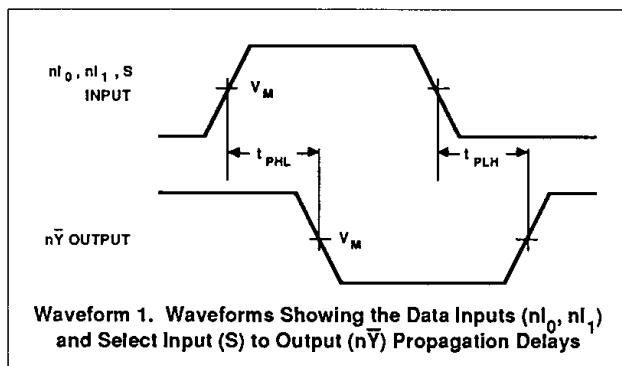
## AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11158					UNIT
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay nI <sub>0</sub> , nI <sub>1</sub> to n $\bar{Y}$	1	1.5 1.5	3.6 3.9	5.4 5.6	1.5 1.5	5.8 6.4	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay S to n $\bar{Y}$	1	1.5 1.5	4.1 4.4	5.9 6.2	1.5 1.5	6.4 6.9	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay $\bar{E}$ to n $\bar{Y}$	2	1.5 1.5	3.7 4.2	5.4 5.9	1.5 1.5	5.9 6.5	ns

## AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11158					UNIT
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay nI <sub>0</sub> , nI <sub>1</sub> to n $\bar{Y}$	1	2.0 2.7	5.1 5.9	7.6 8.3	2.0 2.7	8.4 9.4	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay S to n $\bar{Y}$	1	2.3 2.9	5.3 6.7	7.7 9.8	2.3 2.9	8.5 10.8	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay $\bar{E}$ to n $\bar{Y}$	2	2.5 2.5	5.1 6.1	6.8 8.9	2.5 2.5	7.5 10.0	ns

## AC WAVEFORMS



**Quad 2-input multiplexer, INV**

**74AC/ACT11158**

**WAVEFORM CONDITIONS**

	INPUTS	OUTPUTS
AC	$V_{IN} = \text{GND to } V_{CC}$ , $V_M = 50\% V_{CC}$	$V_{OUT} = V_{OL} \text{ to } V_{OH}$
ACT	$V_{IN} = \text{GND to } 3.0V$ , $V_M = 1.5V$	$V_M = 50\% V_{CC}$

**TEST CIRCUIT**

