

# 54ACT11280, 74ACT11280 9-BIT PARITY GENERATORS/CHECKERS

SCAS046A – D3148, AUGUST 1988 – REVISED APRIL 1993

- Inputs Are TTL-Voltage Compatible
- Generates Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bits Parity
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin  $V_{CC}$  and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

## description

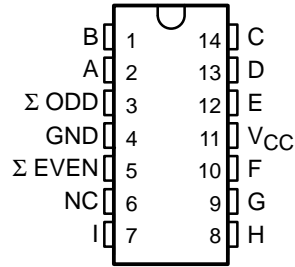
These universal, monolithic, 9-bit parity generators/checkers feature odd and even outputs to facilitate operation of either an odd or even parity application. The word-length capability is easily expanded by cascading.

The 54ACT11280 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The 74ACT11280 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

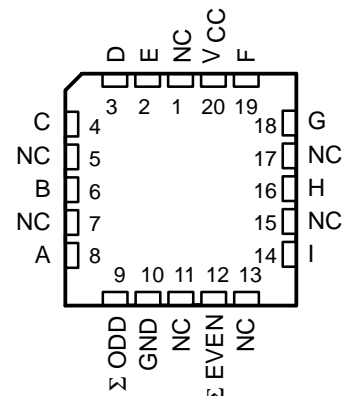
FUNCTION TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	$\Sigma$ EVEN	$\Sigma$ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

54ACT11280 . . . J PACKAGE  
74ACT11280 . . . D OR N PACKAGE  
(TOP VIEW)

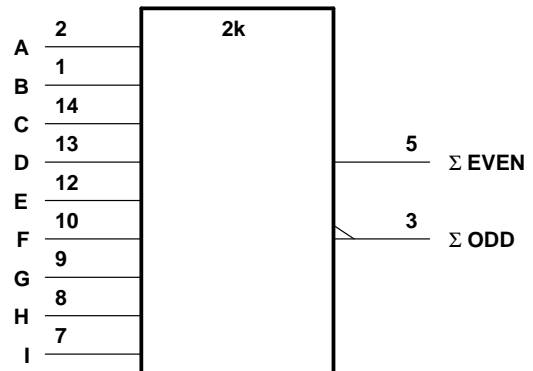


54ACT11280 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, J, and N packages.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

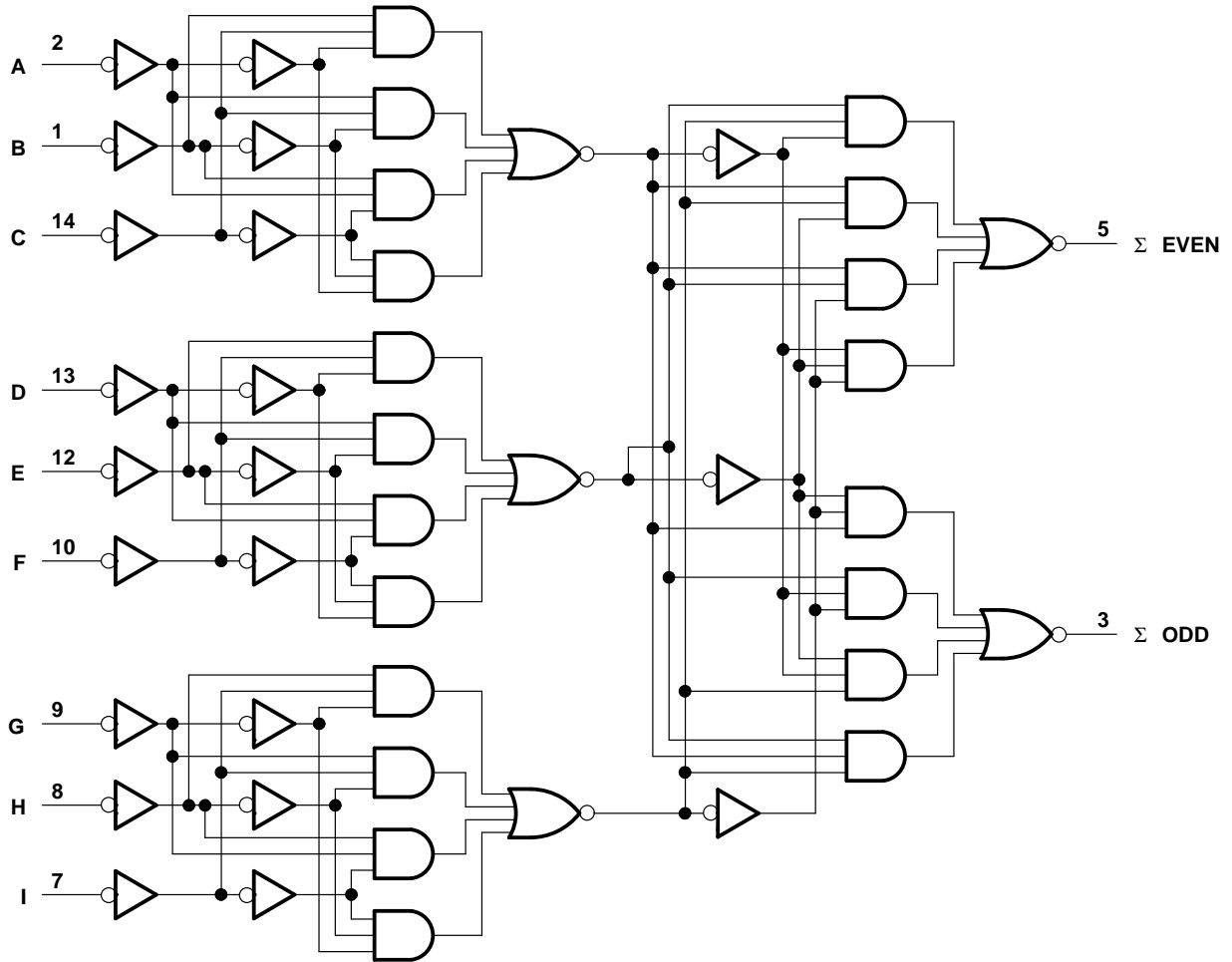
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## logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 00$ mA
Storage temperature range .....	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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## recommended operating conditions

		54ACT11280		74ACT11280		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		-24		-24	mA
$I_{OL}$	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
$T_A$	Operating free-air temperature	-55	125	-40	85	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			54ACT11280		74ACT11280		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$V_{OH}$	$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4		4.4		4.4		V	
		5.5 V	5.4		5.4		5.4			
	$I_{OH} = -24 \text{ mA}$	4.5 V	3.94		3.7		3.8			
		5.5 V	4.94		4.7		4.8			
	$I_{OH} = -50 \text{ mA}^\dagger$	5.5 V			3.85					
$I_{OH} = -75 \text{ mA}^\dagger$	5.5 V					3.85				
$V_{OL}$	$I_{OL} = 50 \mu\text{A}$	4.5 V			0.1		0.1		V	
		5.5 V			0.1		0.1			
	$I_{OL} = 24 \text{ mA}$	4.5 V			0.36		0.5	0.44		
		5.5 V			0.36		0.5	0.44		
	$I_{OL} = 50 \text{ mA}^\dagger$	5.5 V					1.60			
$I_{OL} = 75 \text{ mA}^\dagger$	5.5 V						1.65			
$I_I$	$V_I = V_{CC}$ or GND	5.5 V			$\pm 0.1$		$\pm 1$	$\pm 1$	$\mu\text{A}$	
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		160	80	$\mu\text{A}$	
$\Delta I_{CC}^\ddagger$	One input at 3.4 V, Other inputs at GND or $V_{CC}$	5.5 V			0.9		1	1	mA	
$C_i$	$V_I = V_{CC}$ or GND	5 V			3.5				pF	

$^\dagger$  Not more than one output should be tested at a time and the duration of the test should not exceed 10 ms.

$^\ddagger$  This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ .

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54ACT11280		74ACT11280		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	Any input	$\Sigma$ EVEN	1.5	7.3	10.8	1.5	13.1	1.5	12.2	ns
$t_{PHL}$			1.5	8.8	12.5	1.5	15.6	1.5	14.3	
$t_{PLH}$	Any input	$\Sigma$ ODD	1.5	7.3	10.8	1.5	12.9	1.5	12.1	ns
$t_{PHL}$			1.5	8.6	12.4	1.5	15.7	1.5	14.3	



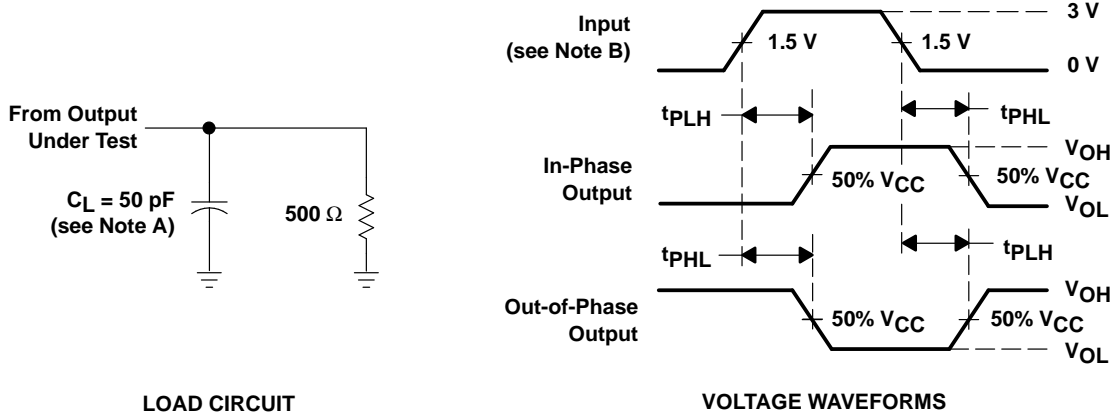
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operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	56	pF

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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