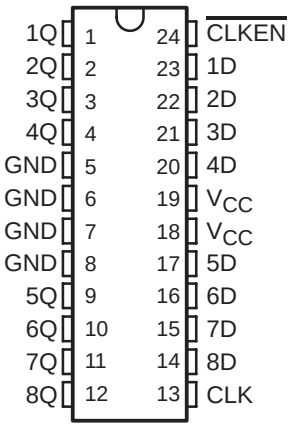
- **Inputs Are TTL-Voltage Compatible**
- **Contains Eight D-Type Flip-Flops**
- **Clock Enable Latched to Avoid False Clocking**
- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Plastic Shrink Small-Outline Packages and Standard Plastic 300-mil DIPs**

DB, DW OR NT PACKAGE
(TOP VIEW)



description

These circuits are positive-edge-triggered D-type flip-flops with a clock enable input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if $\overline{\text{CLKEN}}$ is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at the $\overline{\text{CLKEN}}$ input.

The 74ACT11377 is characterized for operation from − 40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{\text{CLKEN}}$	CLK	D	Q
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	L	X	Q_0

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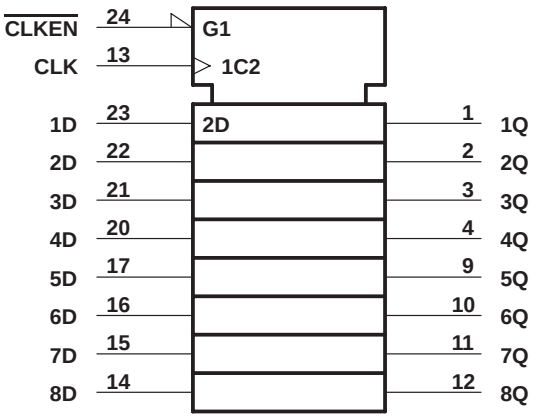
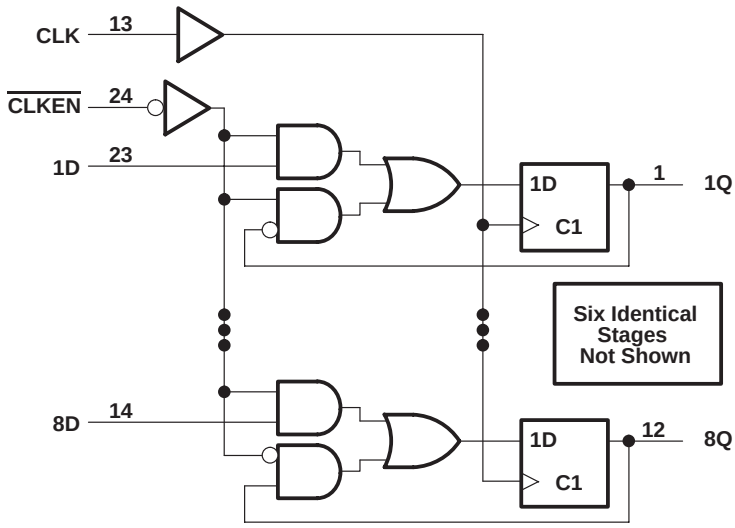
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Input voltage range, V_I (see Note 1) . . . . . − 0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . − 0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ± 50 mA
Continuous current through V_{CC} or GND . . . . . ± 200 mA
Storage temperature range . . . . . − 65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−24	mA
I_{OL}	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns /V
T_A	Operating free-air temperature	− 40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = − 50 μA		4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
	I_{OH} = − 24 mA		4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
	I_{OH} = − 75 mA†		5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA		4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
	I_{OL} = 24 mA		4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
V_{OL}	I_{OL} = 75 mA†		5.5 V					1.65	V
I_I	V_I = V_{CC} or GND		5.5 V			± 0.1		± 1	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	5.5 V			8		80	μA
ΔI_{CC}‡	One input at 3.4 V,	Other inputs at GND or V_{CC}	5.5 V			0.9		1	mA
C_i	V_I = V_{CC} or GND		5 V		4				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	100	0	100	MHz
t_w	Pulse duration	CLK high	5		5		ns
		CLK low	5		5		
t_{su}	Setup time before CLK↑	Data	4		4		ns
		$\overline{\text{CLKEN}}$ high	4		4		
		$\overline{\text{CLKEN}}$ low	5		5		
t_h	Hold time after CLK↑	$\overline{\text{CLKEN}}$ high or low	0		0		ns
		Data high	1		1		
		Data low	0		0		

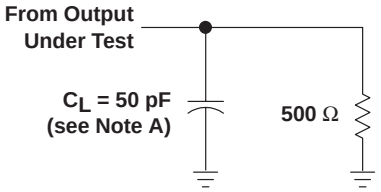
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			100			100		MHz
t_{PLH}	CLK	Any Q	4.5	9.1	12.2	4.5	13.8	ns
t_{PHL}			4.8	9.6	12.7	4.8	14.2	

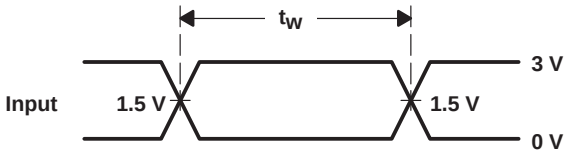
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 1 MHz	68	pF

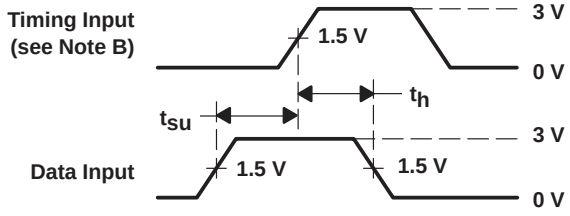
PARAMETER MEASUREMENT INFORMATION



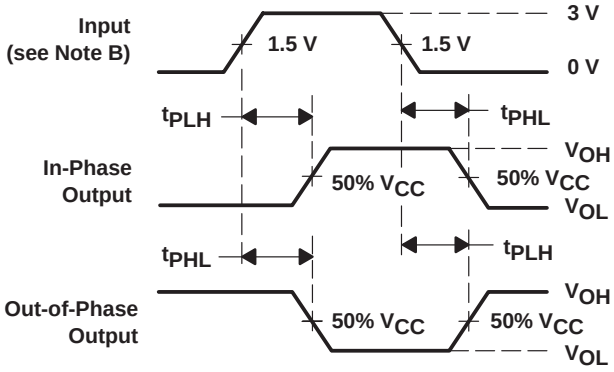
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
74ACT11377DBLE	OBSOLETE	SSOP	DB	24		TBD	Call TI	Call TI
74ACT11377DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
74ACT11377DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
74ACT11377DWR	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
74ACT11377DWR	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
74ACT11377NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI
74ACT11377NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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