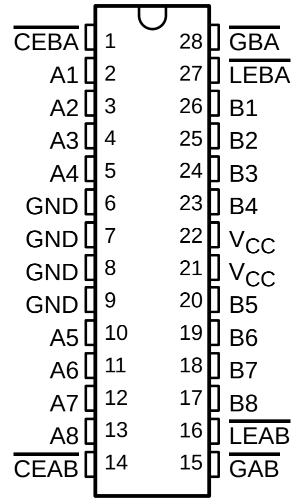
- **Inputs Are TTL-Voltage Compatible**
- **3-State Inverted Outputs**
- **Back-to-Back Registers for Storage**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DW PACKAGE
(TOP VIEW)



description

This 8-bit registered transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch enable ($\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$) and output enable ($\overline{\text{GAB}}$ or $\overline{\text{GBA}}$) inputs are provided for each register to permit independent control in either direction of data flow. The 74ACT11544 inverts data in both directions.

The A-to-B enable ($\overline{\text{CEAB}}$) input must be low in order to enter data from A or to output data to B. Having $\overline{\text{CEAB}}$ low and $\overline{\text{LEAB}}$ low makes the A-to-B latches transparent; a subsequent low-to-high transition of $\overline{\text{LEAB}}$ puts the A latches in the storage mode. With $\overline{\text{CEAB}}$ and $\overline{\text{GAB}}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B-to-A is similar, but requires the use of $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{GBA}}$ inputs.

The 74ACT11544 is characterized for operation from –40°C to 85°C.

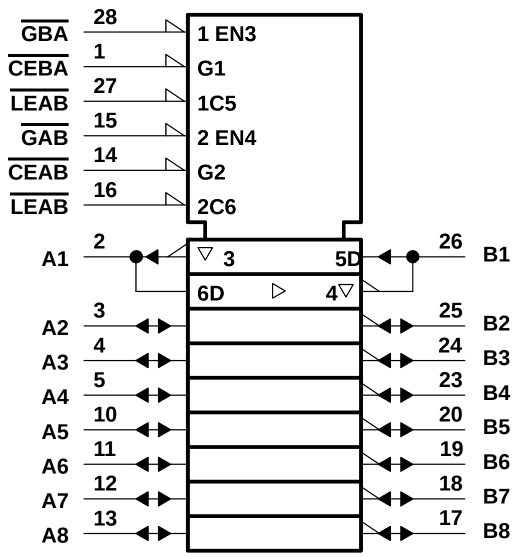
FUNCTION TABLE

INPUTS			LATCH STATUS A TO B†	OUTPUT BUFFERS B1 THRU B8
$\overline{\text{CEAB}}$	$\overline{\text{LEAB}}$	$\overline{\text{GAB}}$		
H	X	X	Storing	Z
X	H		Storing	
X		H		Z
L	L	L	Transparent	Current A Data
L	H	L	Storing	Previous‡ A Data

† A-to-B data flow is shown: B-to-A flow control is the same except uses $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{GBA}}$.
‡ Data present before low-to-high transition of $\overline{\text{LEAB}}$.

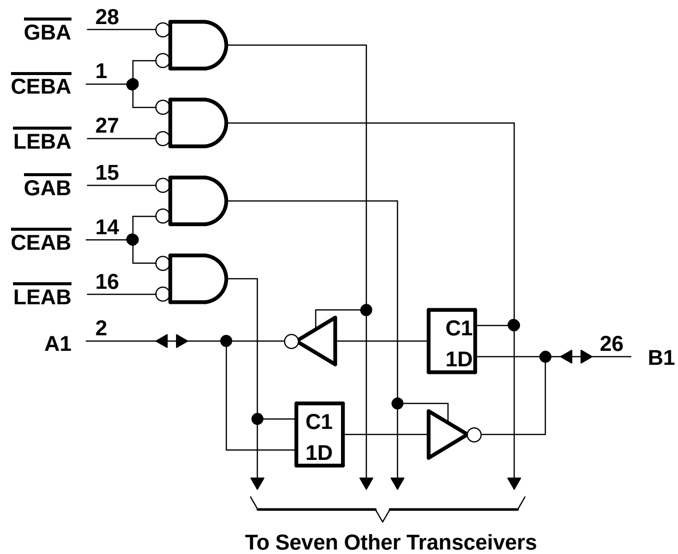
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . ± 50 mA
Continuous current through V_{CC} or GND . . . . ± 200 mA
Storage temperature range . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			–24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	– 40		85	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C MIN	TYP	MAX	MIN	MAX	UNIT
V_{OH}		I_{OH} = – 50 μA	4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
		I_{OH} = – 24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = – 75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1	μA
I_{OZ}	A or B ports‡	$V_O = V_{CC}$ or GND	5.5 V			± 0.5		± 5	μA
I_{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4.5				pF
C_o	A or B ports	$V_O = V_{CC}$ or GND	5 V		12				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			T_A = 25°C MIN	MAX	MIN	MAX	UNIT
t_w	Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low		4		4		ns
t_{su}	Setup time	Data before $\overline{LEAB}$ or $\overline{LEBA}$↑	2.5		2.5		ns
		Data before $\overline{CEAB}$ or $\overline{CEBA}$↑	3		3		
t_h	Hold time	Data after $\overline{LEAB}$ or $\overline{LEBA}$↑	2		2		ns
		Data after $\overline{CEAB}$ or $\overline{CEBA}$↑	1.5		1.5		

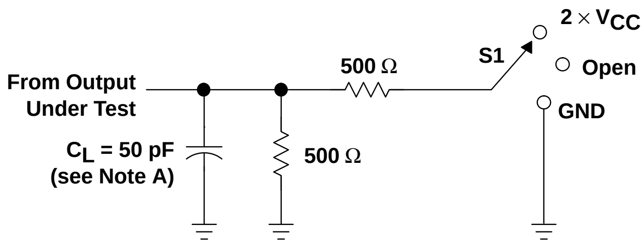
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	MIN	MAX	UNIT
t_{PLH}	A or B	B or A	2.4	5.7	8.2	2.4	8.9	ns
t_{PHL}			4.1	7.3	9.3	4.1	10.3	
t_{PLH}	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	2.6	6	8.7	2.6	9.5	ns
t_{PHL}			3.4	7.1	10.1	3.4	11	
t_{PZH}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	3.3	6.7	9.5	3.3	10.4	ns
t_{PZL}			3.6	8.2	11.2	3.6	13	
t_{PHZ}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	4.8	7.6	9.7	4.8	10.4	ns
t_{PLZ}			4.7	7.6	9.5	4.7	10.2	
t_{PZH}	$\overline{GBA}$ or $\overline{GAB}$	A or B	3	6.4	9	3	9.9	ns
t_{PZL}			3.5	7.8	10.8	3.5	12.5	
t_{PHZ}	$\overline{GBA}$ or $\overline{GAB}$	A or B	4.6	7.3	9.3	4.6	9.9	ns
t_{PLZ}			4.6	7.2	9.2	4.6	9.7	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

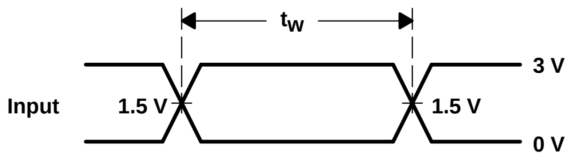
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	47	pF
		Outputs disabled		14	

PARAMETER MEASUREMENT INFORMATION

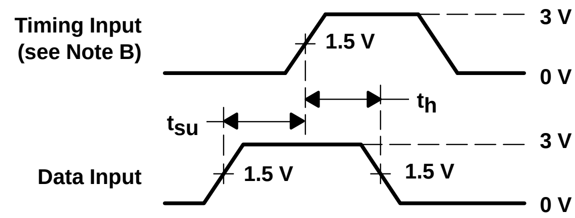


LOAD CIRCUIT

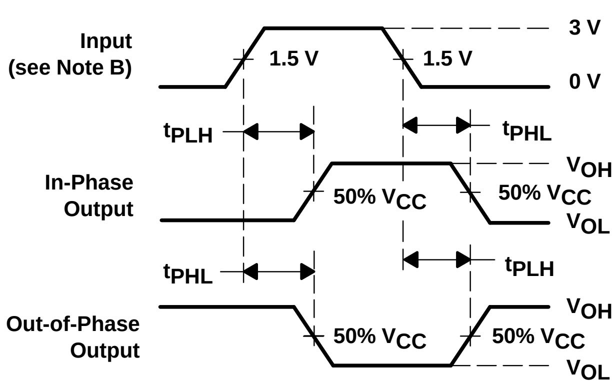
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



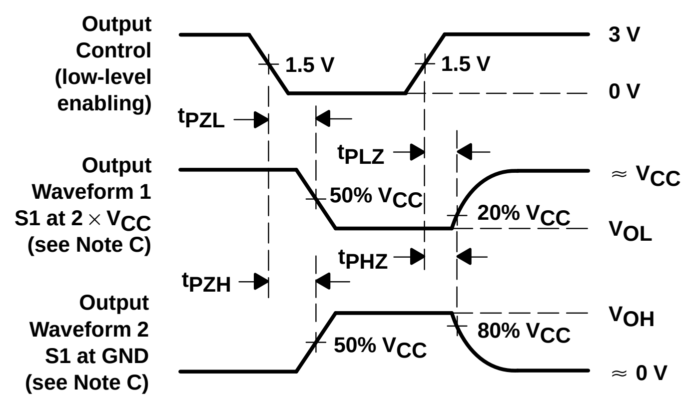
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms