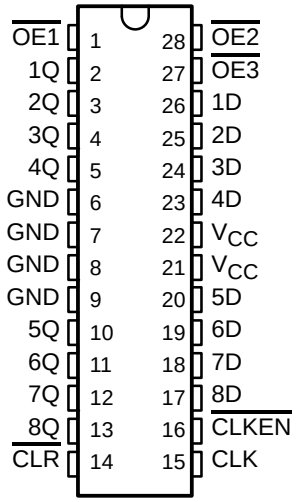
- **Inputs Are TTL-Voltage Compatible**
- **Multiple Output Enables Allow Multiuser Control of the Interface**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DW PACKAGE
(TOP VIEW)



description

This device contains eight flip-flops that feature 3-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing multiuser registers, I/O ports, bidirectional bus drivers, and working registers.

With the clock-enable ($\overline{CLKEN}$) input low, the eight edge-triggered D-type flip-flops enter data on the low-to-high transition of the clock. Taking $\overline{CLKEN}$ high disables the clock buffer, thus latching the outputs. The 74ACT11825 has noninverting data (D) inputs. Taking the clear ($\overline{CLR}$) input low causes the eight Q outputs to go low independently of the clock.

Multiuser buffered output-enable ($\overline{OE1}$, $\overline{OE2}$, and $\overline{OE3}$) inputs can be used to place the eight outputs in either a normal logic state (high or low logic level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components. The output enable ($\overline{OE}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74ACT11825 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS					OUTPUT
$\overline{OE}$†	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

† $\overline{OE}$ = H if any of $\overline{OE1}$, $\overline{OE2}$, or $\overline{OE3}$ are high.
$\overline{OE}$ = L if all of $\overline{OE1}$, $\overline{OE2}$, or $\overline{OE3}$ are low.

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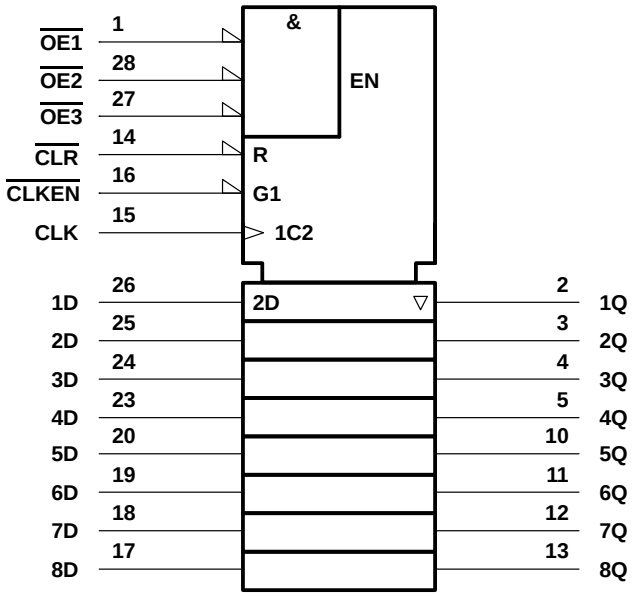
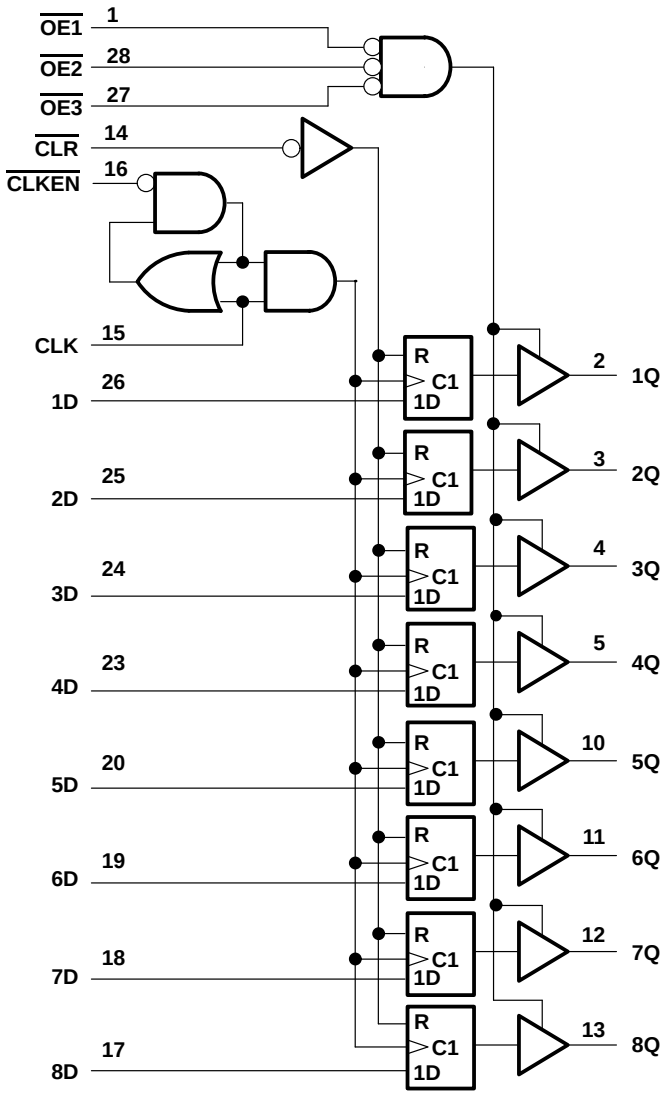
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±200 mA
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			–24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	–40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = –50 µA		4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
	I_{OH} = –24 mA		4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
	I_{OH} = –75 mA†		5.5 V				3.85		
V_{OL}	I_{OL} = 50 µA		4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
	I_{OL} = 24 mA		4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
	I_{OL} = 75 mA†		5.5 V					1.65	
I_I	$V_I = V_{CC}$ or GND		5.5 V			±0.1		±1	µA
I_{OZ}	$V_O = V_{CC}$ or GND		5.5 V			±0.5		±5	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V			8		80	µA
ΔI_{CC}‡	One input at 3.4 V,	Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	$V_I = V_{CC}$ or GND		5 V		4.5				pF
C_o	$V_O = V_{CC}$ or GND		5 V		12				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	122	0	122	MHz
t_w	Pulse duration	$\overline{CLR}$ low	4		4		ns
		CLK high or low	4.5		4.5		
t_{su}	Setup time before CLK↑	$\overline{CLR}$ inactive	3		3		ns
		Data	3		3		
		$\overline{CLKEN}$ high or low	3		3		
t_h	Hold time after CLK↑	Data	1.5		1.5		ns
		$\overline{CLKEN}$ high or low	2		2		

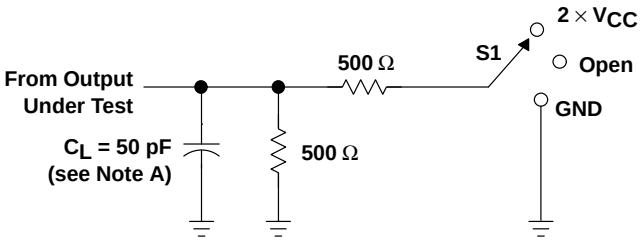
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			122			122		MHz
t_{PLH}	CLK	Q	4.6	7.7	10.2	4.6	11.6	ns
t_{PHL}			5.1	8.4	10.9	5.1	12.3	
t_{PHL}	$\overline{CLR}$	Q	4.5	8.5	11.9	4.5	13.2	ns
t_{PZH}	$\overline{OE}$	Q	3.3	6.4	9.2	3.3	10.4	ns
t_{PZL}			4.2	7.9	11.5	4.2	13	
t_{PHZ}	$\overline{OE}$	Q	6.1	8.5	10.7	6.1	12	ns
t_{PLZ}			5.5	7.9	10	5.5	11.2	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

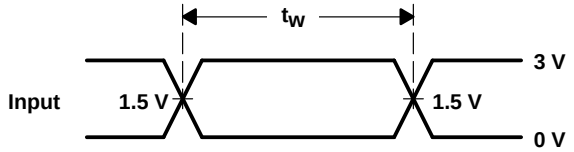
PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF,	f = 1 MHz	47	pF
		Outputs disabled			34	

PARAMETER MEASUREMENT INFORMATION

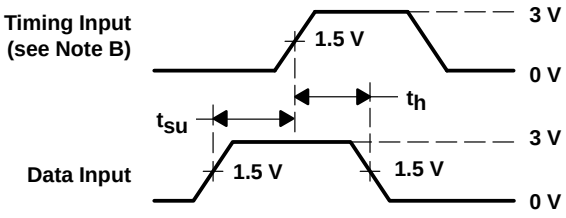


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS



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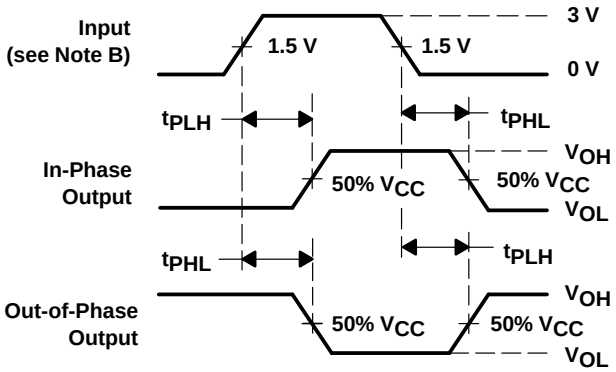
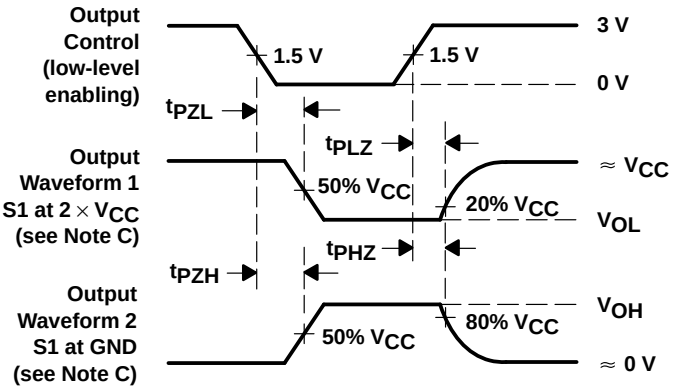


VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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