

74ACT11867

SYNCHRONOUS 8-BIT UP/DOWN BINARY COUNTER WITH ASYNCHRONOUS CLEAR

SCAS178 – D3990, DECEMBER 1991 – REVISED APRIL 1993

- Inputs Are TTL-Voltage Compatible
- Asynchronous Clear
- Fully Independent Clock Circuit Simplifies Use
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 74ACT11867 is a synchronous presettable binary counter featuring an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the eight flip-flops on the rising (positive-going) edge of the clock waveform.

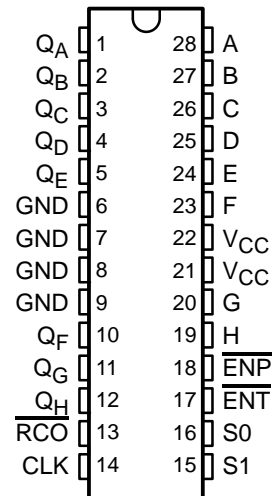
The counters are fully programmable; that is, the outputs may each be preset to either logic level. The load-mode circuitry allows parallel loading of the cascaded counters. As loading is synchronous, selecting the load mode disables the counter and causes the outputs to agree with the data inputs after the next clock rising edge.

The carry look-ahead circuitry is provided for cascading counters for n-bit synchronous applications without additional gating. This is done with two count-enable inputs and a carry output. Both count-enable (\overline{ENP} and \overline{ENT}) inputs must be low to count. The direction of the count is determined by the levels of the select (S_0 and S_1) inputs (see the function table). Input \overline{ENT} is fed forward to enable the ripple-carry (\overline{RCO}) output. \overline{RCO} then produces a low-level pulse while the count is zero (all outputs low) when counting down or 255 during counting up (all outputs high). This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at \overline{ENP} and \overline{ENT} are allowed regardless of the level of the clock input.

These counters feature a fully independent clock circuit. Whenever \overline{ENP} and/or \overline{ENT} is taken high, \overline{RCO} either goes high or remains high. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

The 74ACT11867 is characterized for operation from -40°C to 85°C .

DW PACKAGE
(TOP VIEW)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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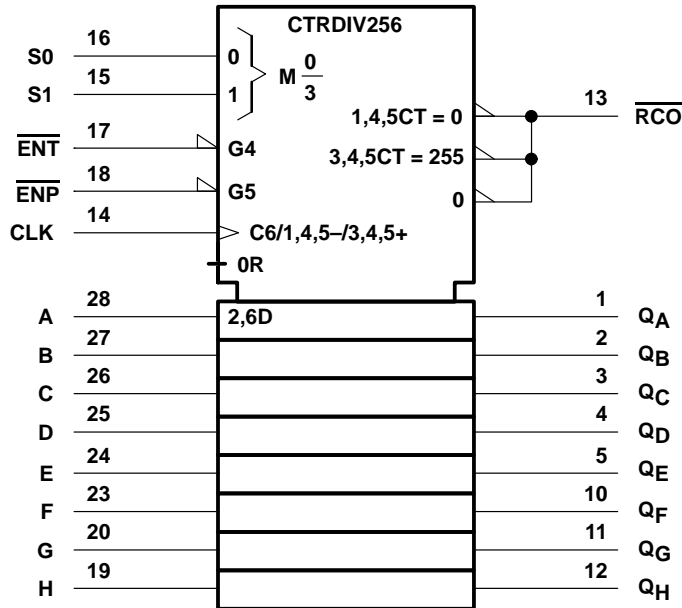
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MODE FUNCTION TABLE

S1	S0	FUNCTION
L	L	Clear
L	H	Count down
H	L	Load
H	H	Count up

logic symbol†

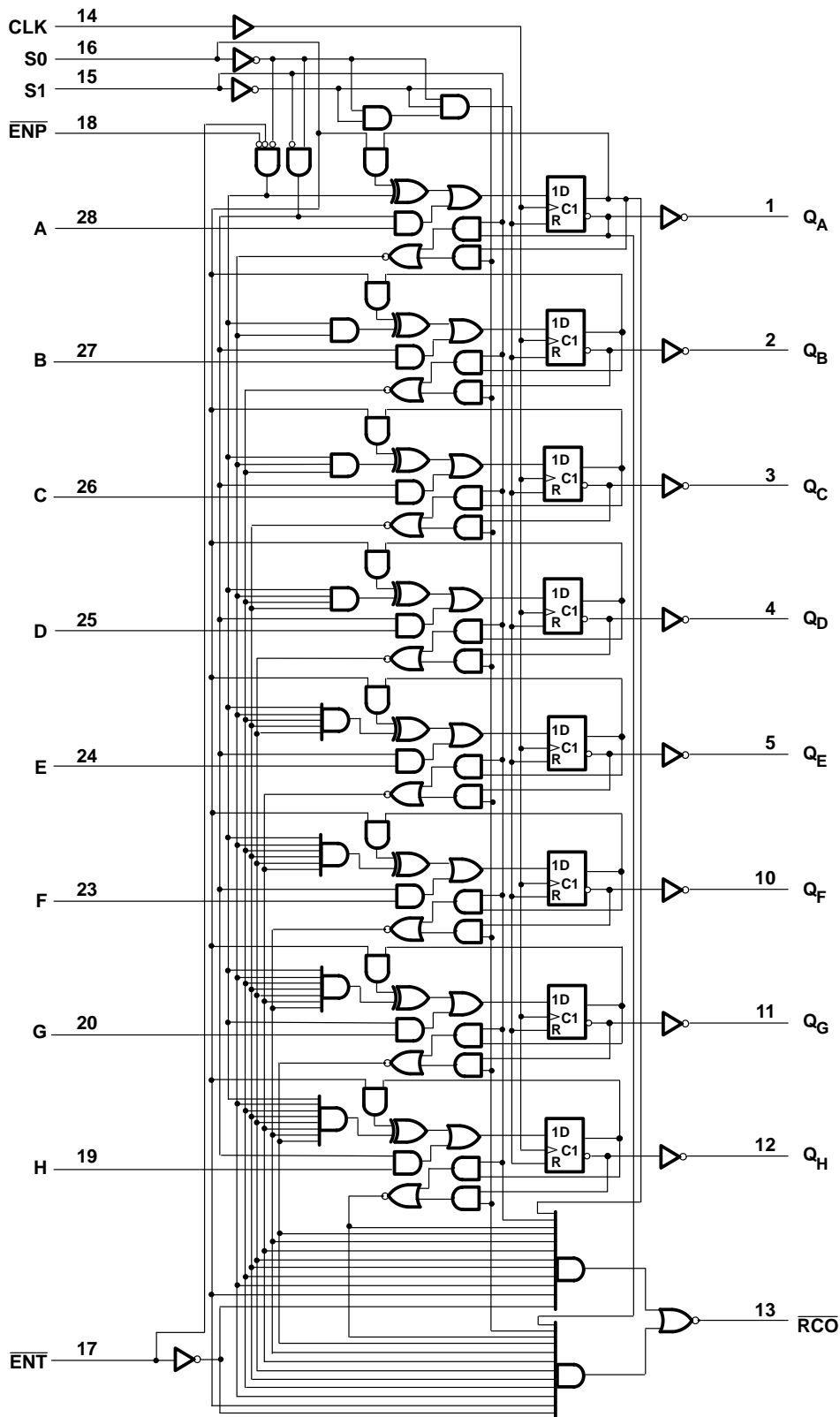


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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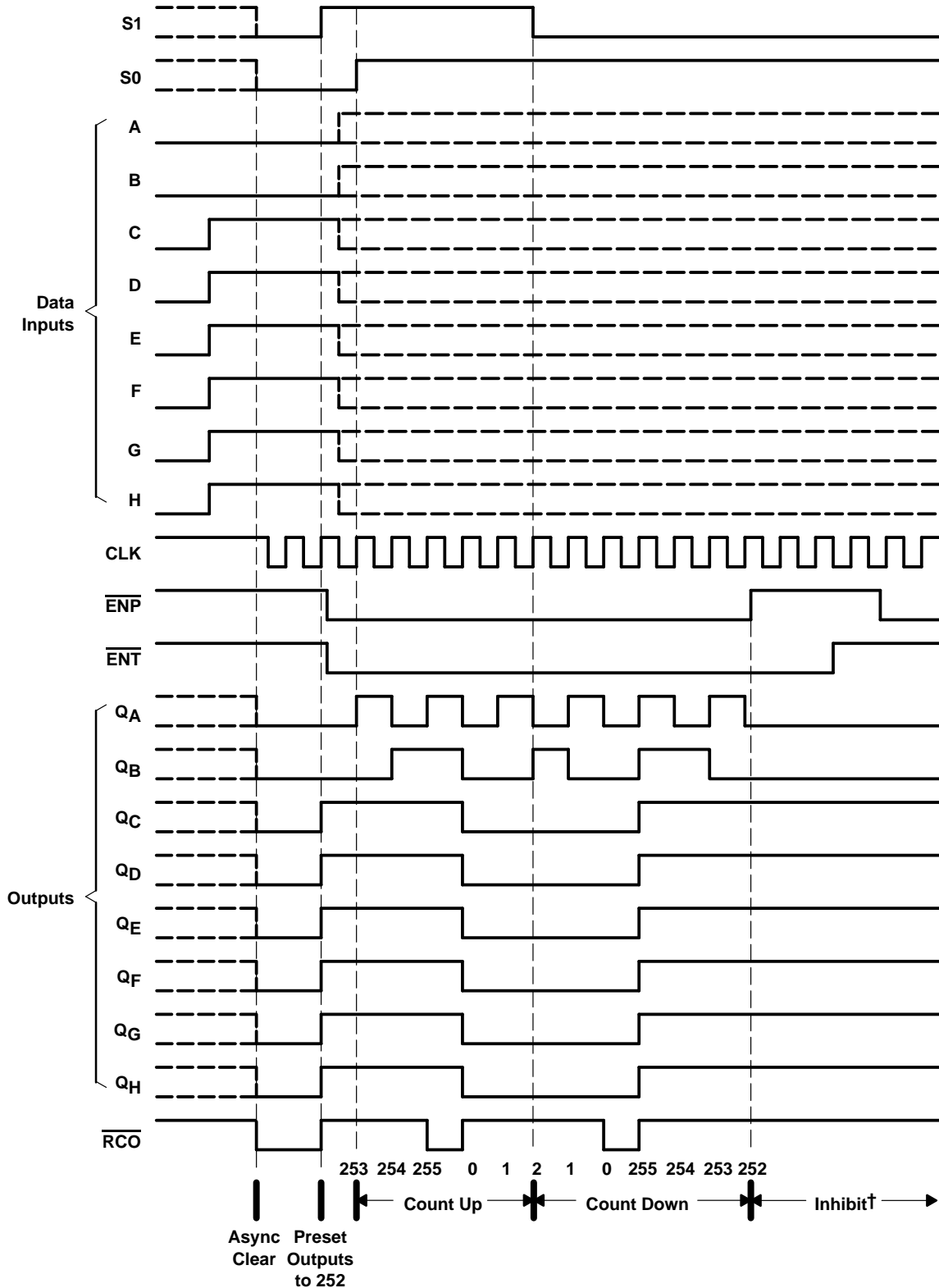
logic diagram (positive logic)



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output sequence



† ENT and ENP must both be low for counting to occur.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 225 mA
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0	V_{CC}		V
V_O	Output voltage	0	V_{CC}		V
I_{OH}	High-level output current			-24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	-40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4		4.4	V		
		5.5 V	5.4		5.4			
	$I_{OH} = -24 \text{ mA}$	4.5 V	3.94		3.8			
		5.5 V	4.94		4.8			
	$I_{OH} = -75 \text{ mA}^\ddagger$	5.5 V			3.85			
V_{OL}	$I_{OL} = 50 \mu\text{A}$	4.5 V			0.1	V		
		5.5 V			0.1			
	$I_{OL} = 24 \text{ mA}$	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	$I_{OL} = 75 \text{ mA}^\ddagger$	5.5 V			1.65			
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1	± 1	μA	
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8	80	μA	
ΔI_{CC}^\S	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9	1	mA	
C_i	$V_I = V_{CC}$ or GND	5 V		4.5			pF	

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .



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timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
f_{clock}	Clock frequency	0	70	0	70	MHz
t_w	Pulse duration	S0 and S1 low	12	12		ns
		CLK	6.5	6.5		
t_{su}^\dagger	Setup time before CLK \uparrow	Data	8	8		ns
		$\overline{\text{ENP}}, \overline{\text{ENT}}$	4	4		
		S0, S1 (load)	11	11		
		S0, S1 (count down)	11	11		
		S0, S1 (count up)	11	11		
t_h	Hold time after CLK \uparrow	Data	1	1		ns
t_{skew}	Skew time between S0 and S1 to avoid inadvertent clear \ddagger	S0 and S1 low	0	0		ns

\dagger This setup time is required to ensure stable data.

\ddagger This is the maximum time for which S0 and S1 may be low simultaneously when the device transitions between the load (S1 = H, S0 = L) and count-down (S1 = L, S0 = H) modes.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			70			70		MHz
t_{PLH}	CLK	$\overline{\text{RCO}}$	6	9.9	12.7	6	14.6	ns
t_{PHL}			6.4	10.9	14.2	6.4	16.3	
t_{PLH}	CLK	Q	5	8.9	11.9	5	13.6	ns
t_{PHL}			4.9	9	12.2	4.9	14	
t_{PLH}	$\overline{\text{ENT}}$	$\overline{\text{RCO}}$	3.9	6.8	9.1	3.9	10.5	ns
t_{PHL}			3.1	7	10.2	3.1	11.5	
t_{PHL}	Clear (S0, S1 low)	Q	6.3	11.9	16.6	6.3	19.1	ns
t_{PLH}	S0, S1 (count up/down)	$\overline{\text{RCO}}$	5.5	10.4	15.6	5.5	17.8	ns
t_{PHL}	S0, S1 (count up/down)	$\overline{\text{RCO}}$	5.6	10.1	14.8	5.6	17.2	ns
t_{PHL}	Clear (S0, S1 low)	$\overline{\text{RCO}}$	6.2	11.3	15.6	6.2	17.8	ns

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

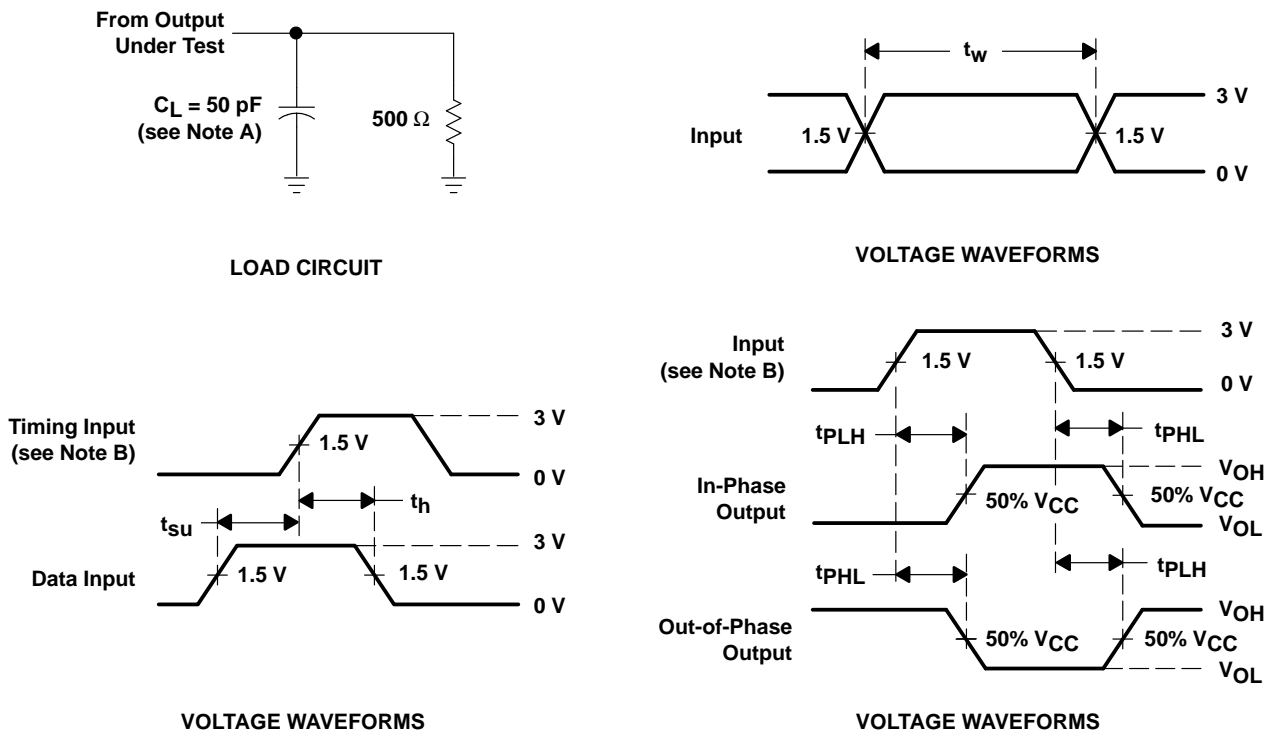
PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	62	pF



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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.

C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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