



74AC374, 74ACT374 Octal D-Type Flip-Flop with 3-STATE Outputs

Features

- I_{CC} and I_{OZ} reduced by 50%
- Buffered positive edge-triggered clock
- 3-STATE outputs for bus-oriented applications
- Outputs source/sink 24mA
- See 273 for reset version
- See 377 for clock enable version
- See 373 for transparent latch version
- See 574 for broadside pinout version
- See 564 for broadside pinout version with inverted outputs
- ACT374 has TTL-compatible inputs

General Description

The AC/ACT374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable (\overline{OE}) are common to all flip-flops.

Ordering Information

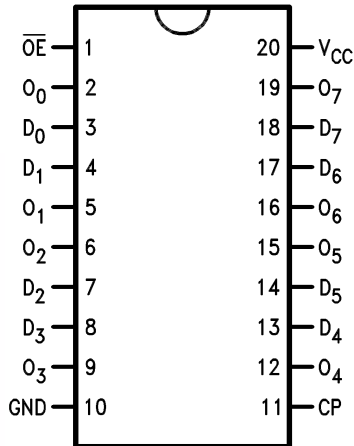
| Order Number | Package Number | Package Description |
|--------------|----------------|---|
| 74AC374SC | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74AC374SJ | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74AC374MTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74AC374PC | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |
| 74ACT374SC | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74ACT374SJ | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74ACT374MSA | MSA20 | 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide |
| 74ACT374MTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74ACT374PC | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

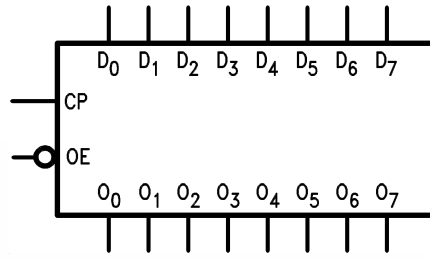


All packages are lead free per JEDEC: J-STD-020B standard.

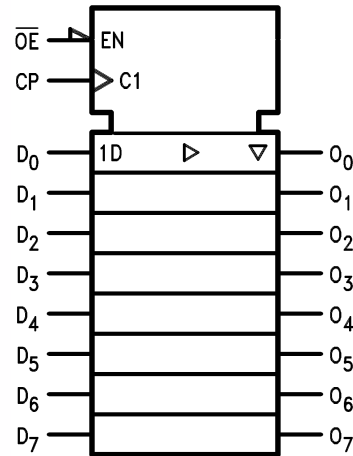
Connection Diagram



Logic Symbols



IEEE/IEC



Pin Description

| Pin Names | Description |
|--------------------------------|-----------------------------|
| D ₀ -D ₇ | Data Inputs |
| CP | Clock Pulse Input |
| \overline{OE} | 3-STATE Output Enable Input |
| O ₀ -O ₇ | 3-STATE Outputs |

Functional Description

The AC/ACT374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable (\overline{OE}) LOW, the contents of the eight flip-flops are available at the outputs. When the \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

Truth Table

| Inputs | | | Outputs |
|----------------|----|-----------------|----------------|
| D _n | CP | \overline{OE} | O _n |
| H | ↗ | L | H |
| L | ↗ | L | L |
| X | X | H | Z |

H = HIGH Voltage Level

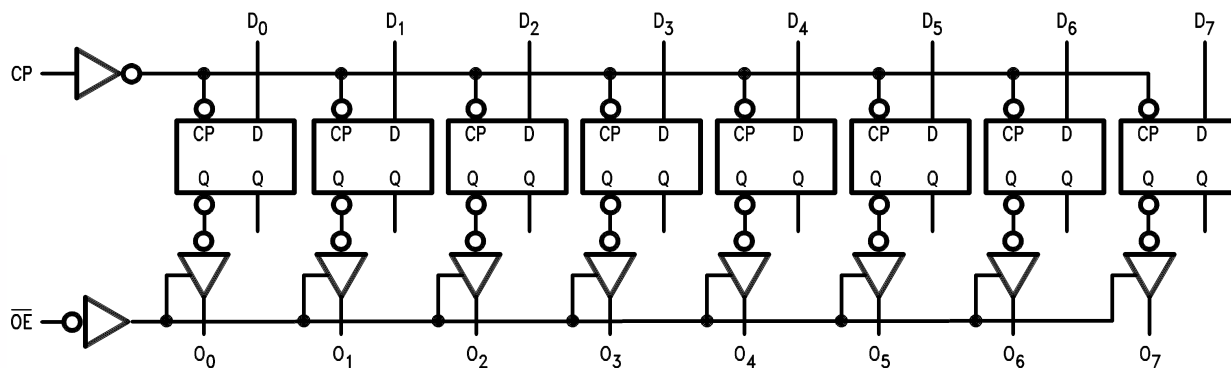
L = LOW Voltage Level

X = Immaterial

Z = High Impedance

↗ = LOW-to-HIGH Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Rating |
|-----------------------|--|--------------------------|
| V_{CC} | Supply Voltage | -0.5V to +7.0V |
| I_{IK} | DC Input Diode Current $V_I = -0.5V$ | -20mA |
| | $V_I = V_{CC} + 0.5$ | +20mA |
| V_I | DC Input Voltage | -0.5V to $V_{CC} + 0.5V$ |
| I_{OK} | DC Output Diode Current $V_O = -0.5V$ | -20mA |
| | $V_O = V_{CC} + 0.5V$ | +20mA |
| V_O | DC Output Voltage | -0.5V to $V_{CC} + 0.5V$ |
| I_O | DC Output Source or Sink Current | $\pm 50mA$ |
| I_{CC} or I_{GND} | DC V_{CC} or Ground Current per Output Pin | $\pm 50mA$ |
| T_{STG} | Storage Temperature | -65°C to +150°C |
| T_J | Junction Temperature | 140°C |

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Rating |
|-----------------------|--|----------------|
| V_{CC} | Supply Voltage AC | 2.0V to 6.0V |
| | ACT | 4.5V to 5.5V |
| V_I | Input Voltage | 0V to V_{CC} |
| V_O | Output Voltage | 0V to V_{CC} |
| T_A | Operating Temperature | -40°C to +85°C |
| $\Delta V / \Delta t$ | Minimum Input Edge Rate, AC Devices: V_{IN} from 30% to 70% of V_{CC} , V_{CC} @ 3.3V, 4.5V, 5.5V | 125mV/ns |
| $\Delta V / \Delta t$ | Minimum Input Edge Rate, ACT Devices: V_{IN} from 0.8V to 2.0V, V_{CC} @ 4.5V, 5.5V | 125mV/ns |

DC Electrical Characteristics for AC

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = +25°C | | T _A = -40°C to +85°C | | Units | |
|--------------------------------|---|---------------------|--|---|--|---------------------------------|------|-------|------|
| | | | | Typ. | Guaranteed Limits | | | | |
| V _{IH} | Minimum HIGH Level Input Voltage | 3.0 | V _{OUT} = 0.1V or V _{CC} - 0.1V | 1.5 | 2.1 | 2.1 | | V | |
| | | 4.5 | | 2.25 | 3.15 | 3.15 | | | |
| | | 5.5 | | 2.75 | 3.85 | 3.85 | | | |
| V _{IL} | Maximum LOW Level Input Voltage | 3.0 | V _{OUT} = 0.1V or V _{CC} - 0.1V | 1.5 | 0.9 | 0.9 | | V | |
| | | 4.5 | | 2.25 | 1.35 | 1.35 | | | |
| | | 5.5 | | 2.75 | 1.65 | 1.65 | | | |
| V _{OH} | Minimum HIGH Level Output Voltage | 3.0 | I _{OUT} = -50μA | 2.99 | 2.9 | 2.9 | | V | |
| | | 4.5 | | 4.49 | 4.4 | 4.4 | | | |
| | | 5.5 | | 5.49 | 5.4 | 5.4 | | | |
| | | 3.0 | V _{IN} = V _{IL} or V _{IH} , I _{OH} = -12mA | | 2.56 | 2.46 | | | |
| | | 4.5 | | V _{IN} = V _{IL} or V _{IH} , I _{OH} = -24mA | | 3.86 | 3.76 | | |
| | | 5.5 | | | V _{IN} = V _{IL} or V _{IH} , I _{OH} = -24mA ⁽¹⁾ | | 4.86 | | 4.76 |
| V _{OL} | Maximum LOW Level Output Voltage | 3.0 | I _{OUT} = 50μA | 0.002 | | 0.1 | 0.1 | | V |
| | | 4.5 | | 0.001 | 0.1 | 0.1 | | | |
| | | 5.5 | | 0.001 | 0.1 | 0.1 | | | |
| | | 3.0 | V _{IN} = V _{IL} or V _{IH} , I _{OL} = 12mA | | 0.36 | 0.44 | | | |
| | | 4.5 | | V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA | | 0.36 | 0.44 | | |
| | | 5.5 | | | V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA ⁽¹⁾ | | 0.36 | 0.44 | |
| I _{IN} ⁽²⁾ | Maximum Input Leakage Current | 5.5 | V _I = V _{CC} , GND | | | ±0.1 | ±1.0 | μA | |
| I _{OZ} | Maximum 3-STATE Leakage Current | 5.5 | V _I (OE) = V _{IL} , V _{IH} ; V _I = V _{CC} , GND; V _O = V _{CC} , GND | | ±0.25 | ±2.5 | | μA | |
| I _{OLD} | Minimum Dynamic Output Current ⁽³⁾ | 5.5 | V _{OLD} = 1.65V Max. | | | 75 | | mA | |
| I _{OHD} | | 5.5 | V _{OHD} = 3.85V Min. | | | -75 | | mA | |
| I _{CC} ⁽²⁾ | Maximum Quiescent Supply Current | 5.5 | V _{IN} = V _{CC} or GND | | 4.0 | 40.0 | | μA | |

Notes:

1. All outputs loaded; thresholds on input associated with output under test.
2. I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
3. Maximum test duration 2.0ms, one output loaded at a time.

DC Electrical Characteristics for ACT

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = +25°C | | T _A = -40°C to +85°C | | Units |
|------------------|---|---------------------|---|------------------------|-------------------|---------------------------------|--|-------|
| | | | | Typ. | Guaranteed Limits | | | |
| V _{IH} | Minimum HIGH Level Input Voltage | 4.5 | V _{OUT} = 0.1V or V _{CC} - 0.1V | 1.5 | 2.0 | 2.0 | | V |
| | | 5.5 | | 1.5 | 2.0 | 2.0 | | |
| V _{IL} | Maximum LOW Level Input Voltage | 4.5 | V _{OUT} = 0.1V or V _{CC} - 0.1V | 1.5 | 0.8 | 0.8 | | V |
| | | 5.5 | | 1.5 | 0.8 | 0.8 | | |
| V _{OH} | Minimum HIGH Level Output Voltage | 4.5 | I _{OUT} = -50μA | 4.49 | 4.4 | 4.4 | | V |
| | | 5.5 | | 5.49 | 5.4 | 5.4 | | |
| | | 4.5 | V _{IN} = V _{IL} or V _{IH} , I _{OH} = -24mA | | 3.86 | 3.76 | | |
| | | 5.5 | V _{IN} = V _{IL} or V _{IH} , I _{OH} = -24mA ⁽⁴⁾ | | 4.86 | 4.76 | | |
| V _{OL} | Maximum LOW Level Output Voltage | 4.5 | I _{OUT} = 50μA | 0.001 | 0.1 | 0.1 | | V |
| | | 5.5 | | 0.001 | 0.1 | 0.1 | | |
| | | 4.5 | V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA | | 0.36 | 0.44 | | |
| | | 5.5 | V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA ⁽⁴⁾ | | 0.36 | 0.44 | | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | V _I = V _{CC} , GND | | ±0.1 | ±1.0 | | μA |
| I _{OZ} | Maximum 3-STATE Leakage Current | 5.5 | V _I = V _{IL} , V _{IH} ; V _O = V _{CC} , GND | | ±0.25 | ±2.5 | | μA |
| I _{CCT} | Maximum I _{CC} /Input | 5.5 | V _I = V _{CC} - 2.1V | 0.6 | | 1.5 | | mA |
| I _{OLD} | Minimum Dynamic Output Current ⁽⁵⁾ | 5.5 | V _{OLD} = 1.65V Max. | | | 75 | | mA |
| I _{OHD} | | 5.5 | V _{OHD} = 3.85V Min. | | | -75 | | mA |
| I _{CC} | Maximum Quiescent Supply Current | 5.5 | V _{IN} = V _{CC} or GND | | 4.0 | 40.0 | | μA |

Notes:

- All outputs loaded; thresholds on input associated with output under test.
- Maximum test duration 2.0ms, one output loaded at a time.

AC Electrical Characteristics for AC

| Symbol | Parameter | V _{CC} (V) ⁽⁶⁾ | T _A = +25°C, C _L = 50pF | | | T _A = -40°C to +85°C, C _L = 50pF | | Units |
|------------------|--|------------------------------------|--|------|------|---|------|-------|
| | | | Min. | Typ. | Max. | Min. | Max. | |
| f _{MAX} | Maximum Clock Frequency | 3.3 | 60 | 110 | | 60 | | MHz |
| | | 5.0 | 100 | 155 | | 100 | | |
| t _{PLH} | Propagation Delay, CP to O _n | 3.3 | 3.0 | 11.0 | 13.5 | 1.5 | 15.5 | ns |
| | | 5.0 | 2.5 | 8.0 | 9.5 | 1.5 | 10.5 | |
| t _{PHL} | Propagation Delay, CP to O _n | 3.3 | 2.5 | 10.0 | 12.5 | 2.0 | 14.0 | ns |
| | | 5.0 | 2.0 | 7.0 | 9.0 | 1.5 | 10.0 | |
| t _{PZH} | Output Enable Time | 3.3 | 3.0 | 9.5 | 11.5 | 1.5 | 13.0 | ns |
| | | 5.0 | 2.0 | 7.0 | 8.5 | 1.0 | 9.5 | |
| t _{PZL} | Output Enable Time | 3.3 | 2.5 | 9.0 | 11.5 | 1.5 | 13.0 | ns |
| | | 5.0 | 2.0 | 6.5 | 8.5 | 1.0 | 9.5 | |
| t _{PHZ} | Output Disable Time | 3.3 | 3.0 | 10.5 | 12.5 | 2.0 | 14.5 | ns |
| | | 5.0 | 2.0 | 8.0 | 11.0 | 2.0 | 12.5 | |
| t _{PLZ} | Output Disable Time | 3.3 | 2.0 | 8.0 | 11.5 | 1.0 | 12.5 | ns |
| | | 5.0 | 1.5 | 6.5 | 8.5 | 1.0 | 10.0 | |

Note:

6. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V.

AC Operating Requirements for AC

| Symbol | Parameter | V _{CC} (V) ⁽⁷⁾ | T _A = +25°C, C _L = 50pF | | T _A = -40°C to +85°C, C _L = 50pF | | Units |
|----------------|--|------------------------------------|--|--------------------|---|--|-------|
| | | | Typ. | Guaranteed Minimum | | | |
| t _S | Setup Time, HIGH or LOW, D _n to CP | 3.3 | 2.0 | 5.5 | 6.0 | | ns |
| | | 5.0 | 1.0 | 4.0 | 4.5 | | |
| t _H | Hold Time, HIGH or LOW, D _n to CP | 3.3 | -1.0 | 1.0 | 1.0 | | ns |
| | | 5.0 | 0 | 1.5 | 1.5 | | |
| t _W | CP Pulse Width, HIGH or LOW | 3.3 | 4.0 | 5.5 | 6.0 | | ns |
| | | 5.0 | 2.5 | 4.0 | 4.5 | | |

Note:

7. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V.

AC Electrical Characteristics for ACT

| Symbol | Parameter | V _{CC} (V) ⁽⁸⁾ | T _A = +25°C, C _L = 50pF | | | T _A = -40°C to +85°C, C _L = 50pF | | Units |
|------------------|---|------------------------------------|--|------|------|---|------|-------|
| | | | Min. | Typ. | Max. | Min. | Max. | |
| f _{MAX} | Maximum Clock Frequency | 5.0 | 100 | 160 | | 90 | | MHz |
| t _{PLH} | Propagation Delay, CP to O _n | 5.0 | 2.0 | 8.5 | 10.0 | 2.0 | 11.5 | ns |
| t _{PHL} | Propagation Delay, CP to O _n | 5.0 | 2.0 | 8.0 | 9.5 | 1.5 | 11.0 | ns |
| t _{PZH} | Output Enable Time | 5.0 | 2.0 | 8.0 | 9.5 | 1.5 | 10.5 | ns |
| t _{PZL} | Output Enable Time | 5.0 | 1.5 | 8.0 | 9.0 | 1.5 | 10.5 | ns |
| t _{PHZ} | Output Disable Time | 5.0 | 1.5 | 8.5 | 11.5 | 1.0 | 12.5 | ns |
| t _{PLZ} | Output Disable Time | 5.0 | 1.5 | 7.0 | 8.5 | 1.0 | 10.0 | ns |

Note:

8. Voltage range 5.0 is 5.0V ± 0.5V.

AC Operating Requirements for ACT

| Symbol | Parameter | V _{CC} (V) ⁽⁹⁾ | T _A = +25°C, C _L = 50pF | | T _A = -40°C to +85°C, C _L = 50pF | | Units |
|----------------|---|------------------------------------|--|--------------------|---|--|-------|
| | | | Typ. | Guaranteed Minimum | | | |
| t _S | Setup Time, HIGH or LOW, D _n to CP | 5.0 | 1.0 | 5.5 | 5.5 | | ns |
| t _H | Hold Time, HIGH or LOW, D _n to CP | 5.0 | 0 | 1.5 | 1.5 | | ns |
| t _W | CP Pulse Width, HIGH or LOW | 5.0 | 2.5 | 5.0 | 5.0 | | ns |

Note:

9. Voltage range 5.0 is 5.0V ± 0.5V.

Capacitance

| Symbol | Parameter | Conditions | Typ. | Units |
|-----------------|-------------------|------------------------|------|-------|
| C _{IN} | Input Capacitance | V _{CC} = OPEN | 4.5 | pF |

Physical Dimensions

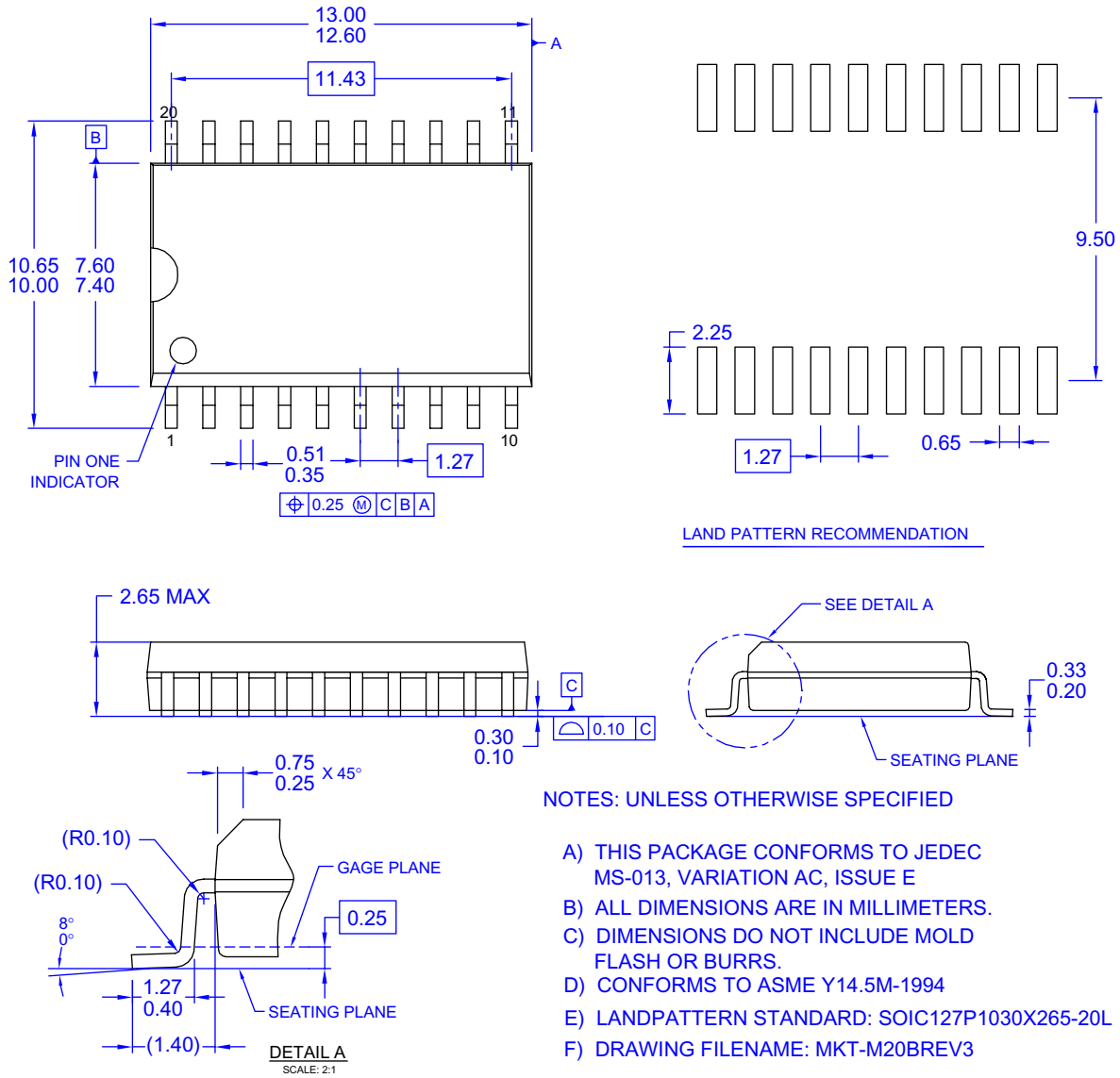


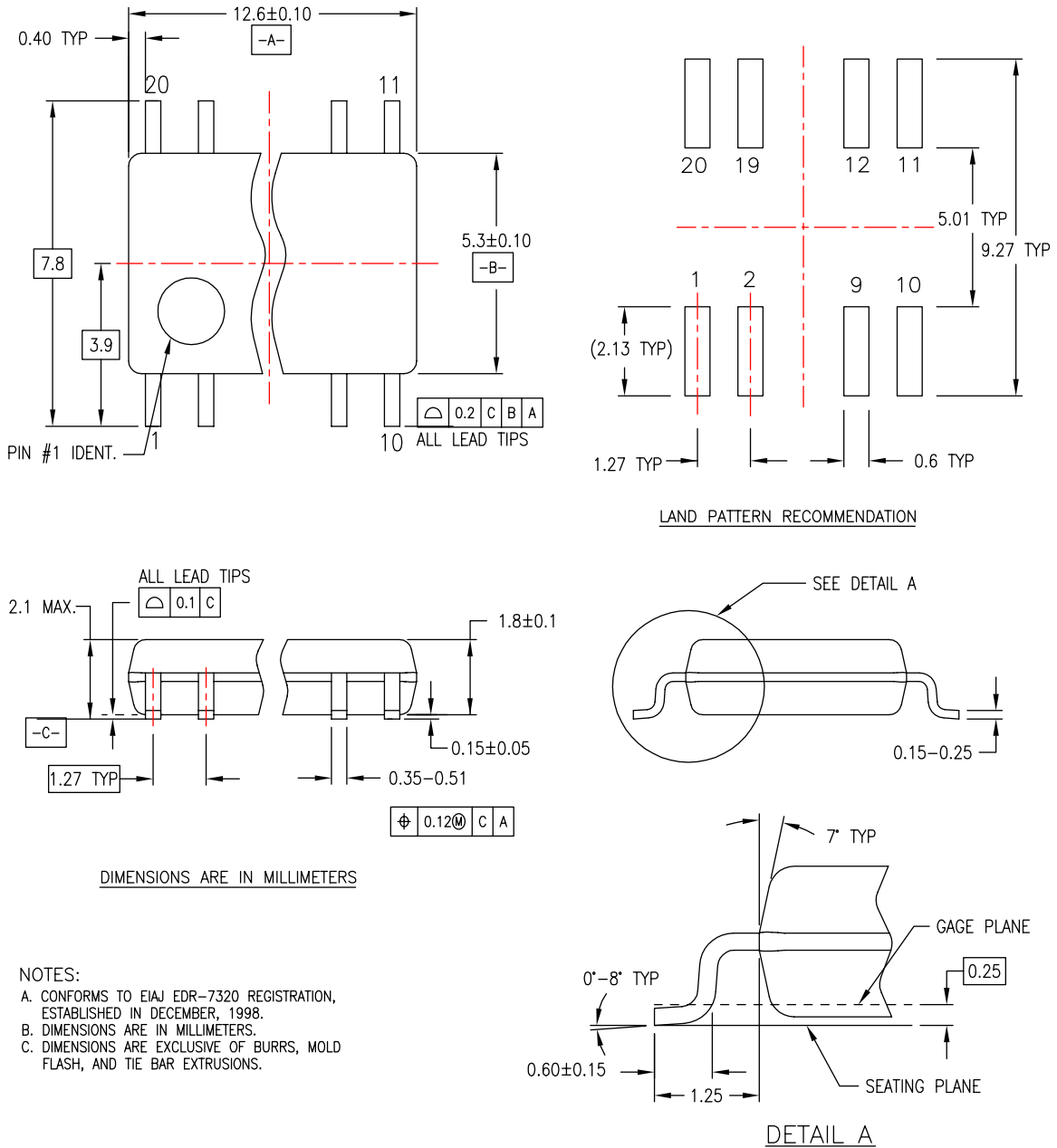
Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

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Physical Dimensions (Continued)



M20DREVC

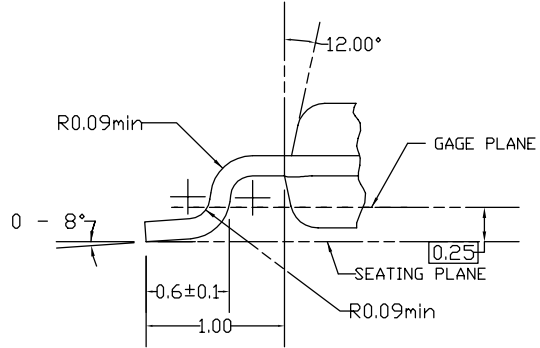
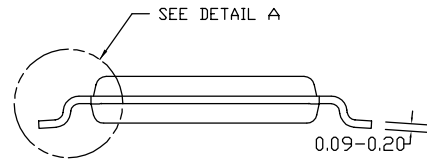
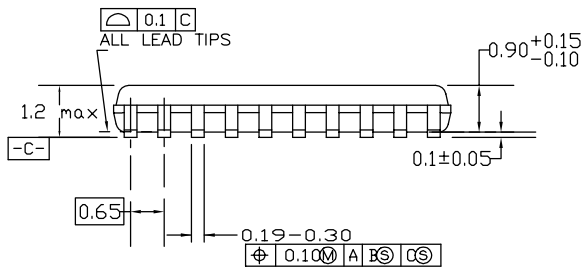
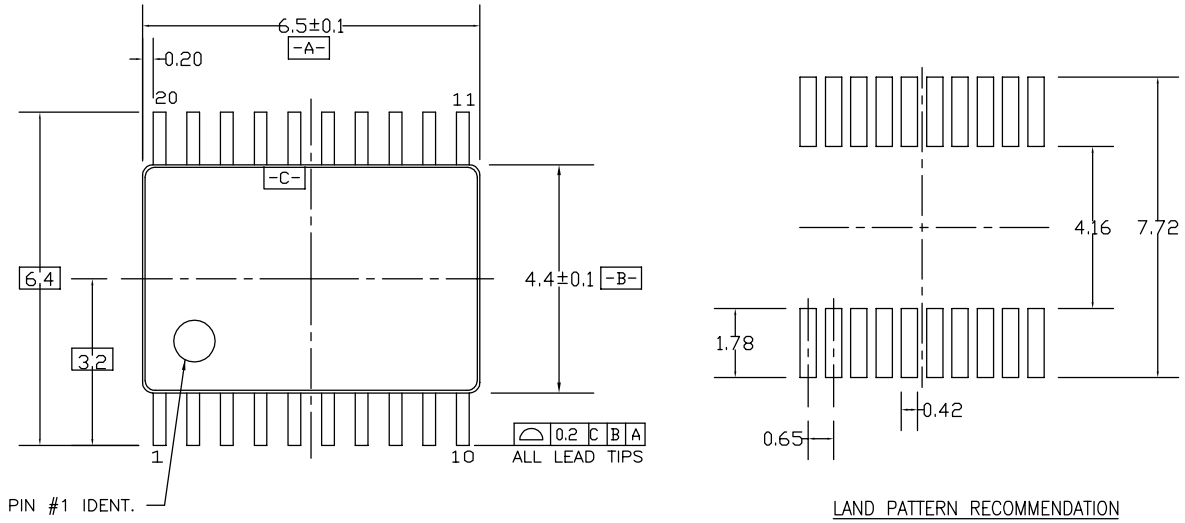
Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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Physical Dimensions (Continued)



DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MD-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REV D1

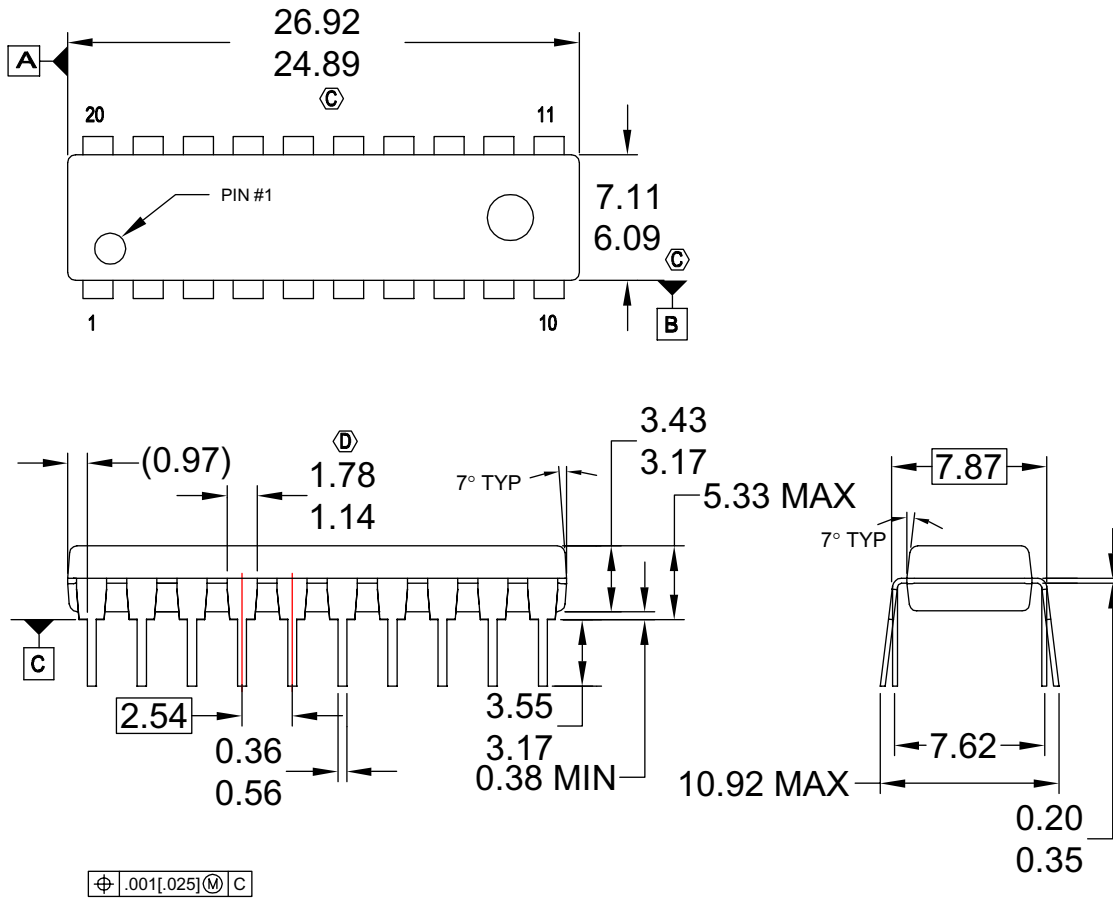
Figure 3. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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Physical Dimensions (Continued)



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MS-001, VARIATIONS AD.
- B. ALL DIMENSIONS ARE IN MILLIMETERS
- \textcircled{C} . DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25MM.
- \textcircled{D} . DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED 0.25MM.
- E. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- F. DRAWING FILE NAME: N20AREV8

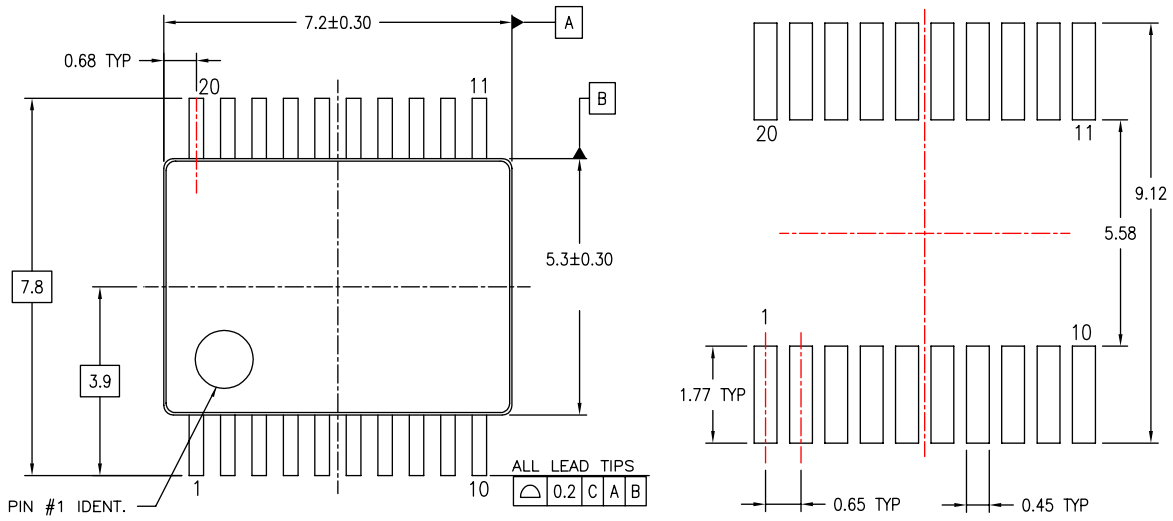
Figure 4. 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

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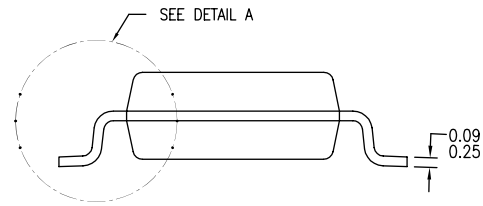
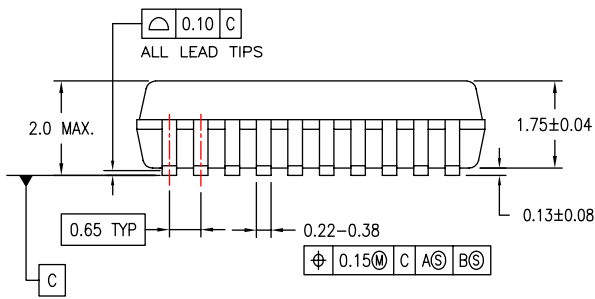
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Physical Dimensions (Continued)



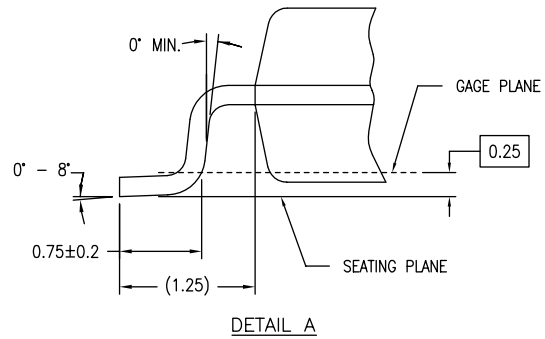
LAND PATTERN RECOMMENDATIONS



DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-150, VARIATION AE, DATE 1/94.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M - 1994.



MSA20REV B

Figure 5. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide

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

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| CorePLUS [™] | Global Power Resource SM | Power247 [®] | GENERAL [®] |
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| | | SuperSOT [™] -6 | VCX [™] |
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