

54ACTQ/74ACTQ16373 16-Bit Transparent Latch with TRI-STATE® Outputs

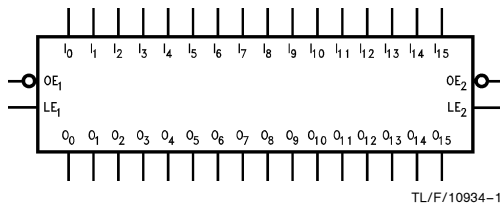
General Description

The 'ACTQ16373 contains sixteen non-inverting latches with TRI-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is low, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the outputs are in high Z state. The 'ACTQ16373 utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control for superior performance.

Features

- Utilizes NSC FACT Quiet Series technology
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin output skew
- Separate control logic for each byte
- 16-bit version of the 'ACTQ373
- Outputs source/sink 24 mA
- Additional specs for Multiple Output Switching
- Output Loading specs for both 50 pF and 250 pF loads

Logic Symbol

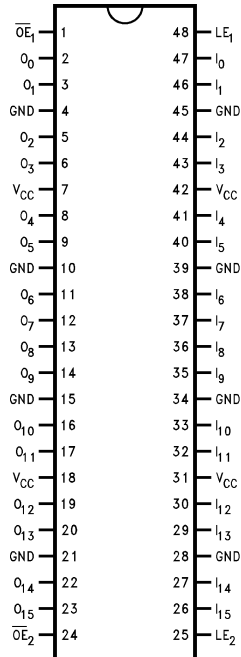


Pin Description

Pin Names	Description
\overline{OE}_n	Output Enable Input (Active Low)
LE_n	Latch Enable Input
I_0-I_{15}	Inputs
O_0-O_{15}	Outputs

Connection Diagram

Pin Assignment for SSOP and CERPAK



TL/F/10934-2

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Functional Description

The 'ACTQ16373 contains sixteen D-type latches with TRI-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable (LE_n) input is HIGH, data on the D_n enters the latches. In this condition the latches are transparent, i.e., a latch output will change states each time its D input changes. When LE_n is LOW, the latches store information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE_n . The TRI-STATE standard outputs are controlled by the Output Enable (\overline{OE}_n) input. When \overline{OE}_n is LOW, the standard outputs are in the 2-state mode. When \overline{OE}_n is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

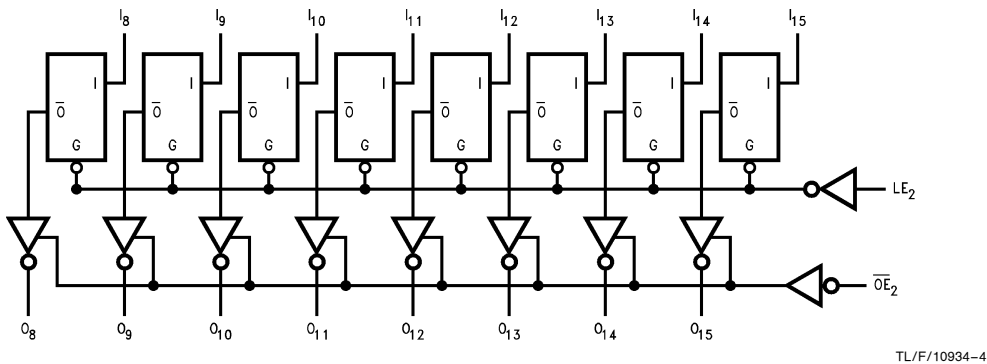
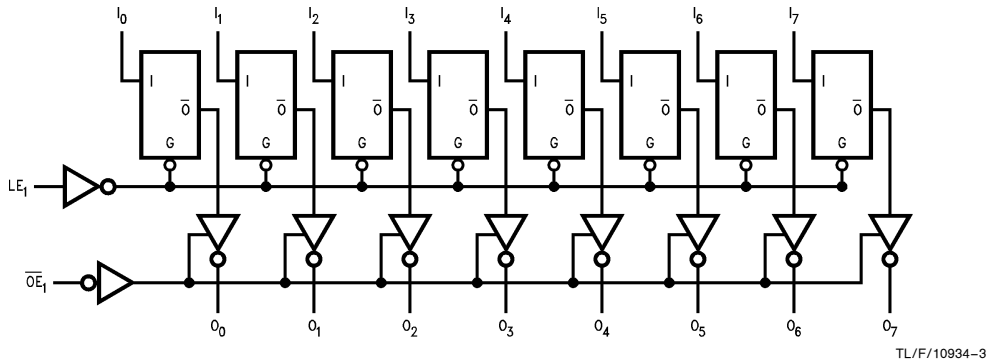
Truth Tables

Inputs			Outputs
LE_1	\overline{OE}_1	I_0-I_7	O_0-O_7
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	(Previous)

Inputs			Outputs
LE_2	\overline{OE}_2	I_8-I_{15}	O_8-O_{15}
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	(Previous)

H = High Voltage Level
 L = Low Voltage Level
 X = Immaterial
 Z = High Impedance
 Previous = previous output prior to HIGH to LOW transition of LE

Logic Diagrams



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source/Sink Current (I_O)	+50 mA
DC V_{CC} or Ground Current per Output Pin	+50 mA
Junction Temperature	
CDIP	+175°C
PDIP/SOIC	+140°C
Storage Temperature	-65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
'ACTQ	
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACTQ	-40°C to +85°C
54ACTQ	-55°C to +125°C
Minimum Input Edge Rate (dV/dt)	
'ACTQ Devices	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

DC Electrical Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ			54ACTQ		74ACTQ		Units	Conditions
			$T_A = +25^\circ\text{C}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$			
			Typ	Guaranteed Limits							
V_{IH}	Minimum High Input Voltage	4.5	1.5	2.0	2.0	2.0	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		5.5	1.5	2.0	2.0	2.0	2.0	2.0			
V_{IL}	Maximum Low Input Voltage	4.5	1.5	0.8	0.8	0.8	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		5.5	1.5	0.8	0.8	0.8	0.8	0.8			
V_{OH}	Minimum High Output Voltage	4.5	4.49	4.4	4.4	4.4	4.4	4.4	V	$I_{OUT} = -50 \mu\text{A}$	
		5.5	5.49	5.4	5.4	5.4	5.4	5.4			
			4.5		3.86	3.70	3.76	3.76	V	$V_{IN}^* = V_{IL}$ or V_{IH} -24 mA I_{OH} -24 mA	
			5.5		4.86	4.70	4.76	4.76			
V_{OL}	Maximum Low Output Voltage	4.5	0.001	0.1	0.1	0.1	0.1	0.1	V	$I_{OUT} = 50 \mu\text{A}$	
		5.5	0.001	0.1	0.1	0.1	0.1	0.1			
			4.5		0.36	0.50	0.44	0.44	V	$V_{IN}^* = V_{IL}$ or V_{IH} 24 mA I_{OL} 24 mA	
			5.5		0.36	0.50	0.44	0.44			
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		± 0.5	± 10.0	± 5.0	± 5.0	μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, \text{GND}$		
I_{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	± 1.0	± 1.0	μA	$V_I = V_{CC}, \text{GND}$		
I_{CCT}	Maximum I_{CC} /Input	5.5	0.6		1.6	1.5	1.5	mA	$V_I = V_{CC} - 2.1V$		
I_{CC}	Max Quiescent Supply Current	5.5		8.0	160.0	80.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 5)		
I_{OLD}	† Minimum Dynamic Output Current	5.5			50	75	75	mA	$V_{OLD} = 1.65V \text{ Max}$		
I_{OHD}					50	-75	-75	mA	$V_{OHD} = 3.85V \text{ Min}$		

*All outputs loaded; thresholds associated with output unders test.

†Maximum test duration 2.0 ms; one output loaded at a time.

DC Electrical Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V _{CC} (V)	74ACTQ		54ACTQ	74ACTQ	Units	Conditions
			T _A = +25°C		T _A = -55°C to +125°C	T _A = -40°C to +85°C		
			TYP	Guaranteed Limits				
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	5.0	0.5	0.8			V	Figures 2-12, 13 (Notes 2, 3)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	5.0	-0.5	-1.0			V	Figures 2-12, 13 (Notes 2, 3)
V _{OHP}	Maximum Overshoot	5.0	V _{OH} + 1.0	V _{OH} + 1.5			V	Figures 2-12, 13 (Notes 1, 3)
V _{OHV}	Minimum V _{CC} Droop	5.0	V _{OH} - 1.0	V _{OH} - 1.8			V	Figures 2-12, 13 (Notes 1, 3)
V _{IHD}	Minimum High Dynamic Input Voltage Level	5.0	1.7	2.0			V	(Notes 1,4)
V _{ILD}	Maximum Low Dynamic Input Voltage Level	5.0	1.2	0.8			V	(Notes 1,4)

Note 1: Worst case package

Note 2: Maximum number of outputs that can switch simultaneously is n. (n - 1) outputs are switched LOW and one output held LOW.

Note 3: Maximum number of outputs that can switch simultaneously is n. (n - 1) outputs are switched HIGH and one output held HIGH.

Note 4: Max number of data inputs (n) switching, (n - 1) input switching 0V to 3V ('ACTQ). Input under test switching 3V to threshold (V_{ILD})

Note 5: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

AC Electrical Characteristics:

Symbol	Parameter	V _{CC} * (V)	74ACTQ			54ACTQ		74ACTQ		Units
			T _A = +25°C C _L = 50 pF			T _A = -55°C to +125°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay D _n to O _n	5.0	3.1 2.6	5.3 4.6	7.9 7.3	3.0 3.0	10.5 10.0	3.1 2.6	8.4 7.8	ns
t _{PLH} t _{PHL}	Propagation Delay LE to O _n	5.0	3.1 2.8	5.4 4.9	7.9 7.3	3.0 3.0	11.0 10.0	3.2 2.8	8.4 7.8	ns
t _{PZH} t _{PZL}	Output Enable Delay	5.0	2.5 2.7	4.7 4.8	7.4 7.5	2.5 2.5	10.0 11.0	2.5 2.7	7.9 8.0	ns
t _{PHZ} t _{PLZ}	Output Disable Delay	5.0	2.1 2.0	5.1 4.5	7.9 7.4	2.0 2.0	9.0 9.0	2.1 2.0	8.2 7.9	ns

*Voltage Range 5.0 is 5.0V ± 0.5V.

Extended AC Electrical Characteristics

Symbol	Parameter	74ACTQ			54ACTQ		74ACTQ		54ACTQ		Units
		T _A = -40°C to +85°C V _{CC} = Com C _L = 50 pF 16 Outputs Switching (Note 2)			T _A = Mil V _{CC} = Mil C _L = 50 pF 16 Outputs Switching (Note 2)		T _A = -40°C to +85°C V _{CC} = Com C _L = 250 pF (Note 3)		T _A = Mil V _{CC} = Mil C _L = 250 pF (Note 3)		
		Min	Typ	Max	Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay Data to Output	4.7 4.6		12.7 10.6	4.7 4.6	13.4 11.3	6.6 6.4	15.7 14.5	6.6 6.4	16.5 15.3	ns
t _{PLH} t _{PHL}	Propagation Delay Latch Enable to Output	4.6 4.1		13.3 10.4	4.6 4.1	14.1 11.0	6.3 5.8	15.3 13.6	6.3 5.8	16.3 14.4	ns
t _{PZH} t _{PZL}	Output Enable Time	3.5 3.6		10.4 10.9	3.5 3.6	11.0 11.6	(Note 4)		(Note 4)		ns
t _{PHZ} t _{PLZ}	Output Disable Time	3.4 3.1		8.5 8.1	3.4 3.1	9.0 8.6	(Note 5)		(Note 5)		ns
t _{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output			1.3							ns
t _{OSLH} (Note 1)	Pin to Pin Skew LH Data to Output			2.1							ns
t _{OST} (Note 1)	Pin to Pin Skew LH/HL Data to Output			4.0							ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}).

Note 2: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 3: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 4: TRI-STATE delays are load dominated and have been excluded from the datasheet.

Note 5: The Output Disable Time is dominated by the RC Network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

AC Operating Requirements:

Symbol	Parameter	V _{CC} * (V)	74ACTQ		54ACTQ		74ACTQ		Units
			+25°C 50 pF		-55°C to +125°C 50 pF		-40°C to +85°C 50 pF		
			Typ	Guaranteed Minimum					
t _S	Setup Time, HIGH or LOW, Input to Clock	5.0		3.0	3.0	3.0	3.0	ns	
t _H	Hold time, High or LOW, Input to Clock	5.0		1.5	1.5	1.5	1.5	ns	
t _w	CS Pulse Width, HIGH or LOW	5.0		4.0	4.0	4.0	4.0	ns	

*Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions	
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$	
C_{PD}	Power Dissipation Capacitance	74ACTQ	30	pF	$V_{CC} = 5.0V$
		54ACTQ	95	pF	$V_{CC} = 5.0V$

FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

Hewlett Packard Model 8180A Word Generator
 PC-163A Test Fixture
 Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the word generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. Swap out the channels that have more than 150 ps of skew until all channels being used are within 150 ps. It is important to deskew the word generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set V_{CC} to 5.0V.
5. Set the word generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.

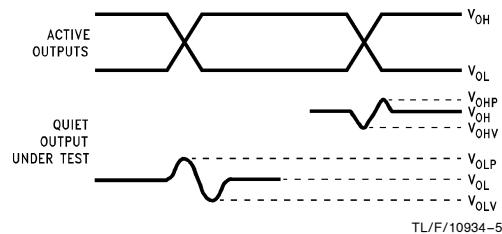


FIGURE 1. Quiet Output Noise Voltage Waveforms

Note A: V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note B: Input pulses have the following characteristics: $f = 1$ MHz, $t_r = 3$ ns, $t_f = 3$ ns, skew < 150 ps.

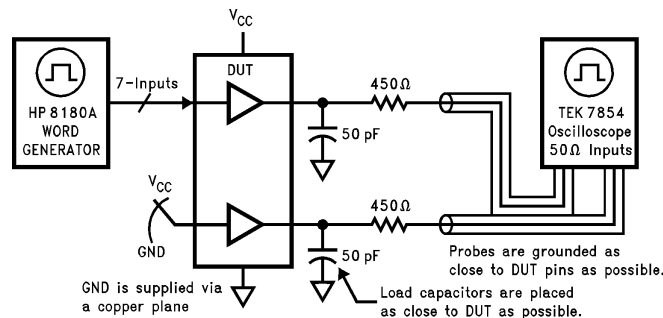


FIGURE 2. Simultaneous Switching Test Circuit

6. Set the word generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with a digital volt meter.

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV} :

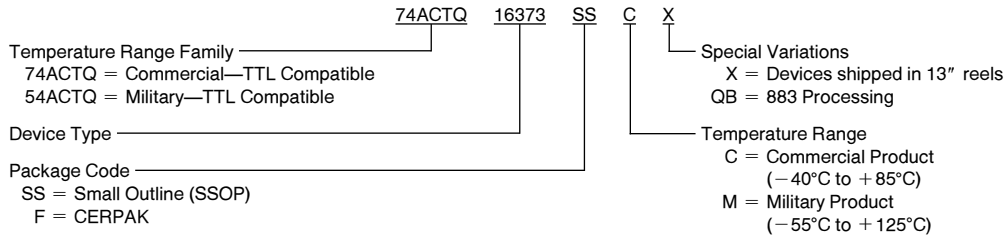
- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output during the HL transition. Measure V_{OHP} and V_{OHV} on the quiet output during the LH transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD} :

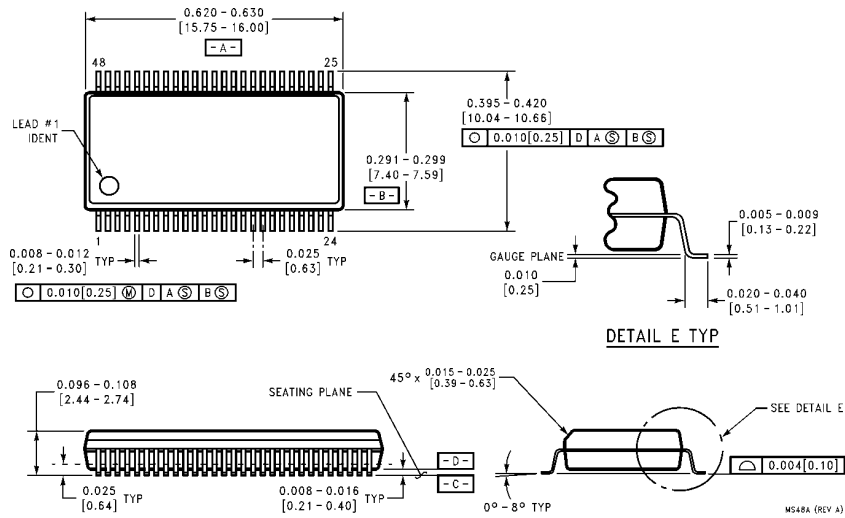
- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL} , until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD} .
- Next increase the input HIGH voltage level on the word generator, V_{IH} until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD} .
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

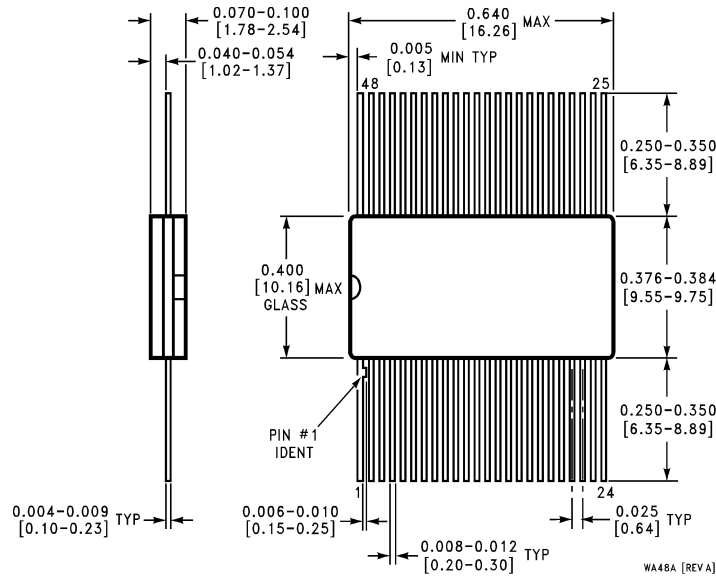


Physical Dimensions inches (millimeters)



**48-Lead SSOP (0.300" Wide) (SS)
NS Package Number MS48A**

Physical Dimensions inches (millimeters) (Continued)



**48-Lead CERPAK (F)
 NS Package Number WA48A**

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