# 74AHC2G00-Q100; 74AHCT2G00-Q100

## Dual 2-input NAND gate

Rev. 1 — 21 March 2013 Product data sheet

## 1. General description

The 74AHC2G00-Q100; 74AHCT2G00-Q100 are high-speed Si-gate CMOS devices. They provide two 2-input NAND gates.

The AHC device has CMOS input switching levels and supply voltage range 2 V to 5.5 V.

The AHCT device has TTL input switching levels and supply voltage range 4.5 V to 5.5 V.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from –40 °C to +85 °C and from –40 °C to +125 °C
- Symmetrical output impedance
- High noise immunity
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Low power dissipation
- Balanced propagation delays
- Multiple package options

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74AHC2G00DP-Q100 | –40 °C to +125 °C | TSSOP8 | plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm | SOT505-2 |
| 74AHCT2G00DP-Q100 | | | | |
| 74AHC2G00DC-Q100 | –40 °C to +125 °C | VSSOP8 | plastic very thin shrink small outline package; 8 leads; body width 2.3 mm | SOT765-1 |
| 74AHCT2G00DC-Q100 | | | | |

## 4. Marking

**Table 2. Marking**

| Type number | Marking code[1] |
|---|---|
| 74AHC2G00DP-Q100 | A00 |
| 74AHCT2G00DP-Q100 | C00 |
| 74AHC2G00DC-Q100 | A00 |
| 74AHCT2G00DC-Q100 | C00 |

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

## 5. Functional diagram

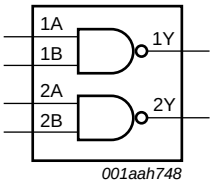



**Fig 1. Logic symbol**

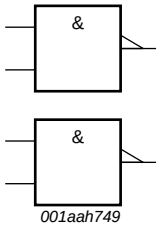



**Fig 2. IEC logic symbol**

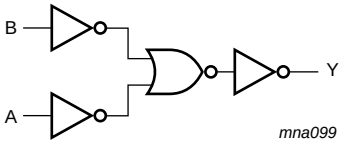



**Fig 3. Logic diagram (one gate)**

# 6. Pinning information

## 6.1 Pinning

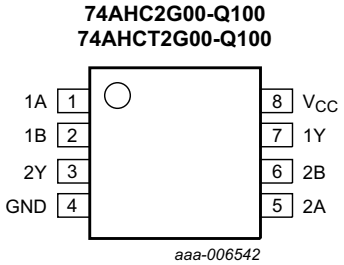



**Fig 4. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)**

## 6.2 Pin description

**Table 3. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| 1A, 2A | 1, 5 | data input |
| 1B, 2B | 2, 6 | data input |
| GND | 4 | ground (0 V) |
| 1Y, 2Y | 7, 3 | data output |
| $V_{CC}$ | 8 | supply voltage |

# 7. Functional description

**Table 4. Function table[1]**

| Input | | Output |
|---|---|---|
| **nA** | **nB** | **nY** |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

[1] H = HIGH voltage level; L = LOW voltage level.

# 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | –0.5 | +7.0 | V |
| $V_I$ | input voltage | | | –0.5 | +7.0 | V |
| $I_{IK}$ | input clamping current | $V_I < –0.5$ V | [1] | –20 | - | mA |
| $I_{OK}$ | output clamping current | $V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V | [1] | - | ±20 | mA |
| $I_O$ | output current | $–0.5$ V $< V_O < V_{CC} + 0.5$ V | | - | ±25 | mA |
| $I_{CC}$ | supply current | | | - | 75 | mA |
| $I_{GND}$ | ground current | | | –75 | - | mA |
| $T_{stg}$ | storage temperature | | | –65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = –40 °C to +125 °C | [2] | - | 250 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 package: above 55 °C the value of $P_{tot}$ derates linearly with 2.5 mW/K.
For VSSOP8 package: above 110 °C the value of $P_{tot}$ derates linearly with 8 mW/K.

# 9. Recommended operating conditions

**Table 6. Recommended operating conditions**

*Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | 74AHC2G00-Q100 | | | 74AHCT2G00-Q100 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{CC}$ | supply voltage | | 2.0 | 5.0 | 5.5 | 4.5 | 5.0 | 5.5 | V |
| $V_I$ | input voltage | | 0 | - | 5.5 | 0 | - | 5.5 | V |
| $V_O$ | output voltage | | 0 | - | $V_{CC}$ | 0 | - | $V_{CC}$ | V |
| $T_{amb}$ | ambient temperature | | –40 | +25 | +125 | –40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | - | - | 100 | - | - | - | ns/V |
| | | $V_{CC}$ = 5.0 V ± 0.5 V | - | - | 20 | - | - | 20 | ns/V |

# 10. Static characteristics

**Table 7. Static characteristics**

*Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| **74AHC2G00-Q100** | | | | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 2.0 V | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | $V_{CC}$ = 3.0 V | 2.1 | - | - | 2.1 | - | 2.1 | - | V |
| | | $V_{CC}$ = 5.5 V | 3.85 | - | - | 3.85 | - | 3.85 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 2.0 V | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | $V_{CC}$ = 3.0 V | - | - | 0.9 | - | 0.9 | - | 0.9 | V |
| | | $V_{CC}$ = 5.5 V | - | - | 1.65 | - | 1.65 | - | 1.65 | V |

**Table 7. Static characteristics** *...continued*

*Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| $V_{OH}$ | HIGH-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | $I_O$ = –50 μA; $V_{CC}$ = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | $I_O$ = –50 μA; $V_{CC}$ = 3.0 V | 2.9 | 3.0 | - | 2.9 | - | 2.9 | - | V |
| | | $I_O$ = –50 μA; $V_{CC}$ = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O$ = –4.0 mA; $V_{CC}$ = 3.0 V | 2.58 | - | - | 2.48 | - | 2.40 | - | V |
| | | $I_O$ = –8.0 mA; $V_{CC}$ = 4.5 V | 3.94 | - | - | 3.8 | - | 3.70 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | $I_O$ = 50 μA; $V_{CC}$ = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 50 μA; $V_{CC}$ = 3.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 50 μA; $V_{CC}$ = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 4.0 mA; $V_{CC}$ = 3.0 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| | | $I_O$ = 8.0 mA; $V_{CC}$ = 4.5 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| $I_I$ | input leakage current | $V_I$ = 5.5 V or GND; $V_{CC}$ = 0 V to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | μA |
| $I_{CC}$ | supply current | $V_I = V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 5.5 V | - | - | 10 | - | 10 | - | 40 | μA |
| $C_I$ | input capacitance | | - | 1.5 | 10 | - | 10 | - | 10 | pF |
| **74AHCT2G00-Q100** | | | | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | 2.0 | - | - | 2.0 | - | 2.0 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I = V_{IH}$ or $V_{IL}$; $V_{CC}$ = 4.5 V | | | | | | | | |
| | | $I_O$ = –50 μA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O$ = –8.0 mA | 3.94 | - | - | 3.8 | - | 3.70 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{IH}$ or $V_{IL}$; $V_{CC}$ = 4.5 V | | | | | | | | |
| | | $I_O$ = 50 μA | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 8.0 mA | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| $I_I$ | input leakage current | $V_I$ = 5.5 V or GND; $V_{CC}$ = 0 V to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | μA |
| $I_{CC}$ | supply current | $V_I = V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 5.5 V | - | - | 1.0 | - | 10 | - | 40 | μA |
| $\Delta I_{CC}$ | additional supply current | per input pin; $V_I$ = 3.4 V; other inputs at $V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 5.5 V | - | - | 1.35 | - | 1.5 | - | 1.5 | mA |
| $C_I$ | input capacitance | | - | 1.5 | 10 | - | 10 | - | 10 | pF |

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

*GND = 0 V; for test circuit see Figure 6.*

| Symbol | Parameter | Conditions | | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| **74AHC2G00-Q100** | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | nA, nB to nY; see Figure 5 | [1] | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [2] | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 4.5 | 7.9 | 1.0 | 9.5 | 1.0 | 10.5 | ns |
| | | $C_L$ = 50 pF | | - | 6.5 | 11.4 | 1.0 | 13.0 | 1.0 | 14.5 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | [3] | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 3.5 | 5.5 | 1.0 | 6.5 | 1.0 | 7.0 | ns |
| | | $C_L$ = 50 pF | | - | 4.9 | 7.5 | 1.0 | 8.5 | 1.0 | 9.5 | ns |
| $C_{PD}$ | power dissipation capacitance | per buffer; $C_L$ = 50 pF; $f_i$ = 1 MHz; $V_I$ = GND to $V_{CC}$ | [4] | - | 17 | - | - | - | - | - | pF |
| **74AHCT2G00-Q100** | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | nA, nB to nY; see Figure 5 | [1] | | | | | | | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | [3] | | | | | | | | |
| | | $C_L$ = 15 pF | | 1.0 | 3.6 | 6.2 | 1.0 | 7.1 | 1.0 | 8.0 | ns |
| | | $C_L$ = 50 pF | | 1.0 | 5.0 | 7.9 | 1.0 | 9.0 | 1.0 | 10.0 | ns |
| $C_{PD}$ | power dissipation capacitance | per buffer; $C_L$ = 50 pF; $f_i$ = 1 MHz; $V_I$ = GND to $V_{CC}$ | [4] | - | 18 | - | - | - | - | - | pF |

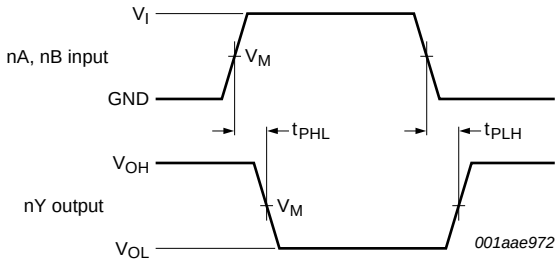
[1] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$.

[2] Typical values are measured at $V_{CC}$ = 3.3 V.

[3] Typical values are measured at $V_{CC}$ = 5.0 V.

[4] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz;
$f_o$ = output frequency in MHz;
$C_L$ = output load capacitance in pF;
$V_{CC}$ = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

## 12. Waveforms



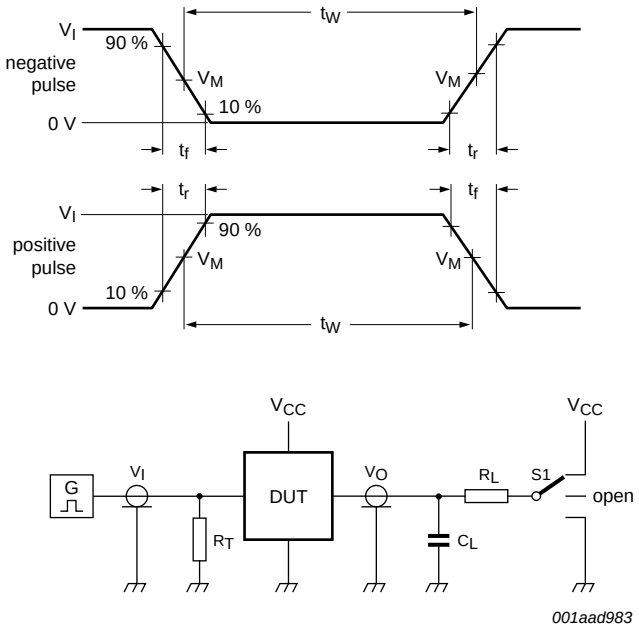

Measurement points are given in Table 9.

Logic levels: $V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Fig 5. The input (nA and nB) to output (nY) propagation delays.**

**Table 9. Measurement points**

| Type | Input | Output |
|---|---|---|
| | $V_M$ | $V_M$ |
| 74AHC2G00-Q100 | $0.5V_{CC}$ | $0.5V_{CC}$ |
| 74AHCT2G00-Q100 | 1.5 V | $0.5V_{CC}$ |




Test data is given in Table 10.

Definitions test circuit:

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_L$ = Load resistance.

S1 = Test selection switch.

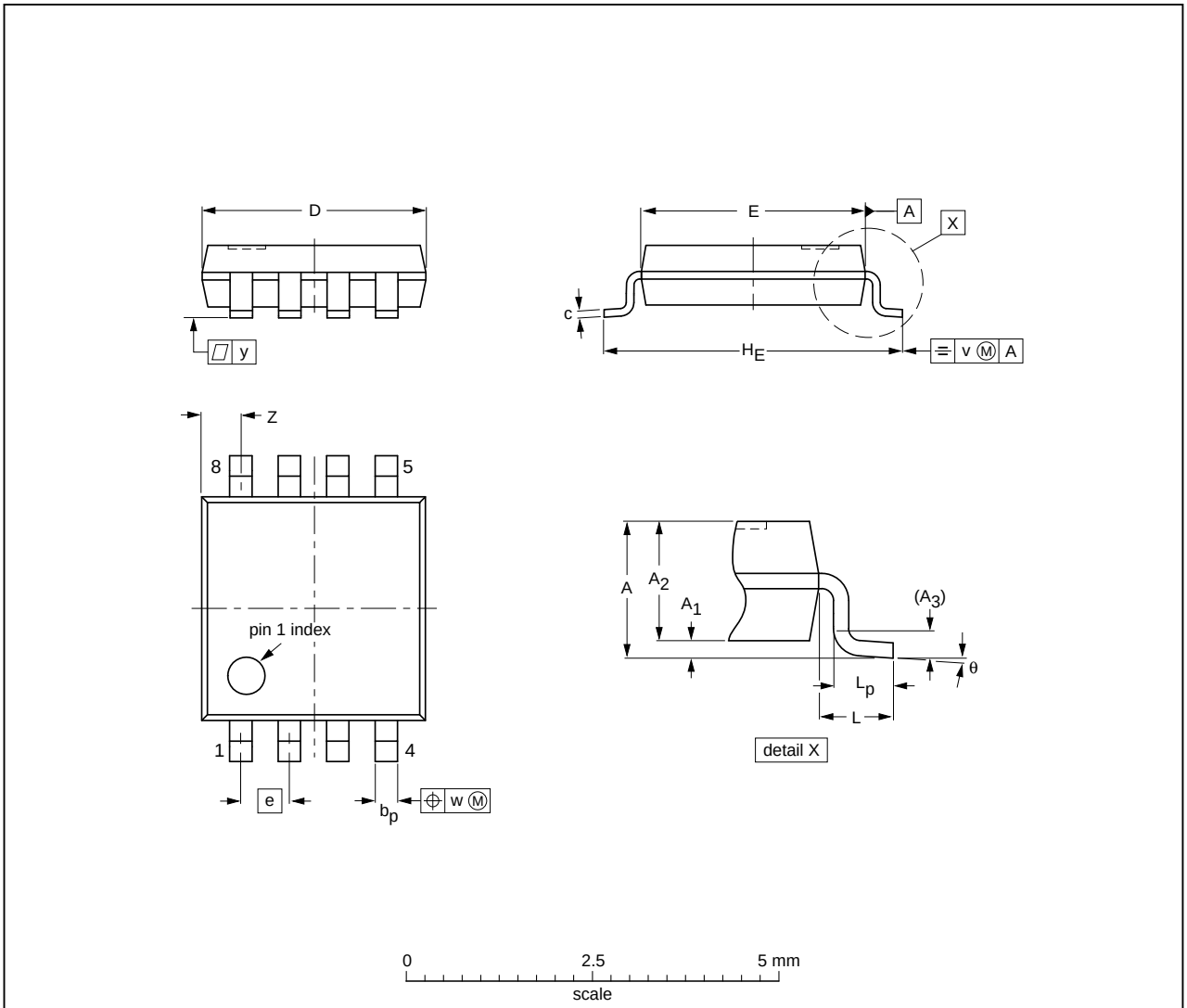
**Fig 6. Test circuit for measuring switching times**

**Table 10. Test data**

| Type | Input | | Load | | S1 position |
|---|---|---|---|---|---|
| | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PHL}$, $t_{PLH}$ |
| 74AHC2G00-Q100 | $V_{CC}$ | ≤ 3 ns | 15 pF, 50 pF | 1 kΩ | open |
| 74AHCT2G00-Q100 | 3 V | ≤ 3 ns | 15 pF, 50 pF | 1 kΩ | open |

## 13. Package outline

**TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.00 | 0.95<br>0.75 | 0.25 | 0.38<br>0.22 | 0.18<br>0.08 | 3.1<br>2.9 | 3.1<br>2.9 | 0.65 | 4.1<br>3.9 | 0.5 | 0.47<br>0.33 | 0.2 | 0.13 | 0.1 | 0.70<br>0.35 | 8°<br>0° |

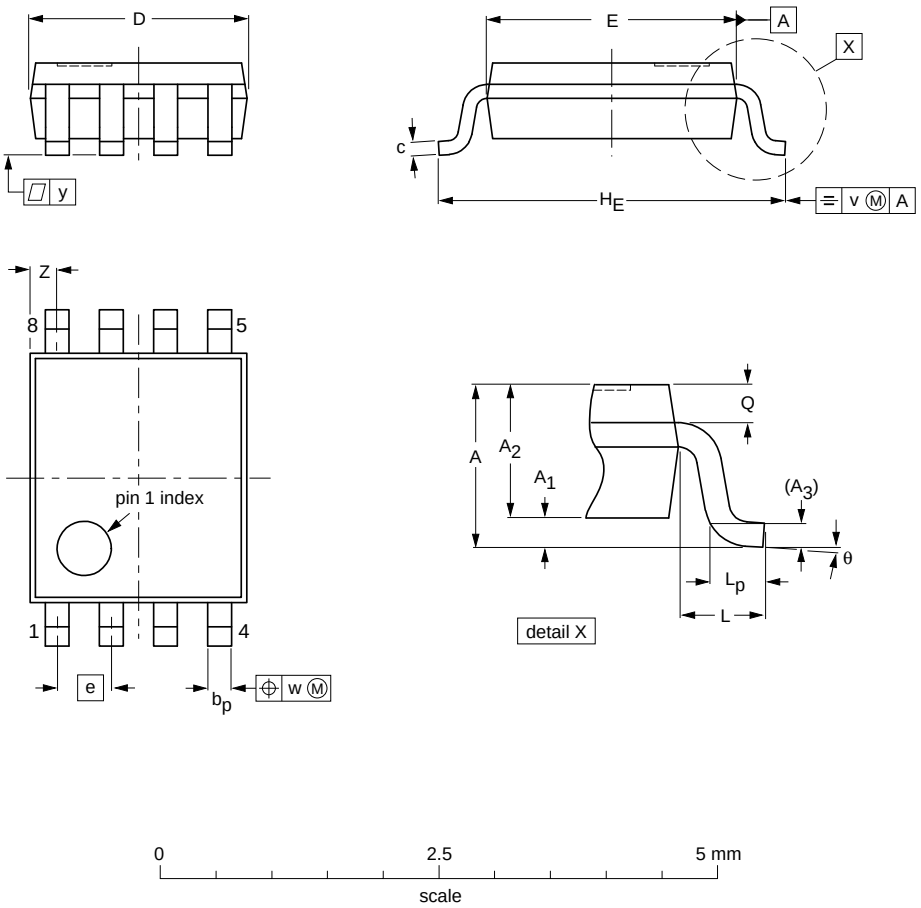
**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT505-2 | | - - - | | | | 02-01-16 |

**Fig 7. Package outline SOT505-2 (TSSOP8)**

**VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm** **SOT765-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1 | 0.15<br>0.00 | 0.85<br>0.60 | 0.12 | 0.27<br>0.17 | 0.23<br>0.08 | 2.1<br>1.9 | 2.4<br>2.2 | 0.5 | 3.2<br>3.0 | 0.4 | 0.40<br>0.15 | 0.21<br>0.19 | 0.2 | 0.13 | 0.1 | 0.4<br>0.1 | 8°<br>0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT765-1 | | MO-187 | | | | 02-06-07 |

**Fig 8. Package outline SOT765-1 (VSSOP8)**

## 14. Abbreviations

**Table 11. Abbreviations**

| Acronym | Description |
|---|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |
| MIL | Military |

## 15. Revision history

**Table 12. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74AHC_AHCT2G00_Q100 v.1 | 20130321 | Product data sheet | - | - |

# 16. Legal information

## 16.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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